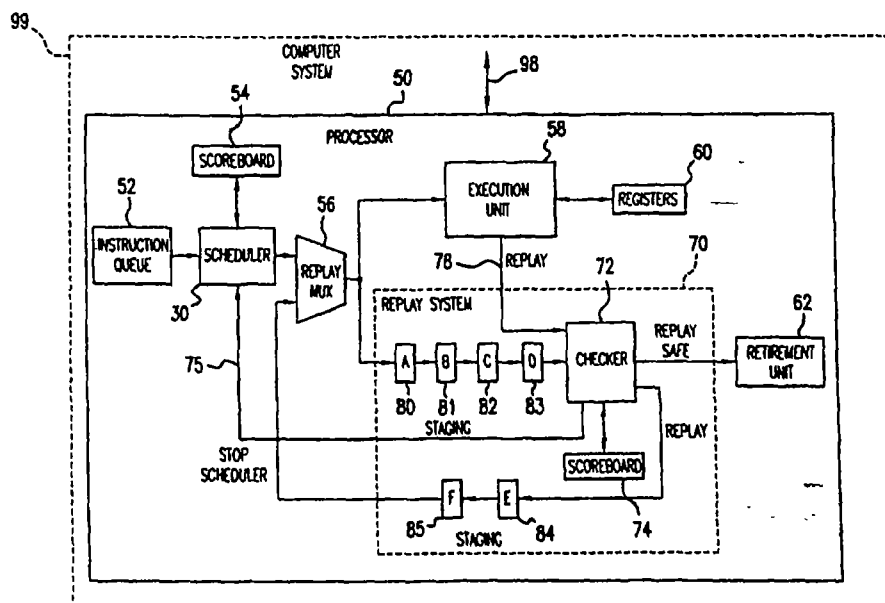


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(54) Title: COMPUTER PROCESSOR WITH A REPLAY SYSTEM



(57) Abstract

A computer processor (50) includes a multiplexer (56) having a first input, a second input, and an output, and a scheduler (30) coupled to the multiplexer first input. The processor further includes an execution unit (58) coupled to the multiplexer output. The execution unit is adapted to receive a plurality of instructions from the multiplexer. The processor further includes a replay system (70) coupled to the second multiplexer input and the scheduler. The replay system replays an instruction that has not correctly executed by sending a stop scheduler signal (75) to the scheduler and sending the instruction to the multiplexer.