~~What is claimed is:~~

CLAIMS

1. ~~——~~ A memory device fabrication method, comprising:

~~———~~forming a hole in a stack of alternating insulator layers and memory cell layers, wherein the insulator layers comprise a second oxide material layer disposed between a plurality of first oxide material layers;

~~———~~removing a first portion of each memory cell layer adjacent the hole to form a plurality of first cavities~~;~~ and expose an intermediate portion of the memory cell layers;

~~———~~performing a radical oxidation process on the intermediate portion of each memory cell layer to form blocking oxides;

depositing a charge trap material in the plurality of first cavities~~;~~ and in contact with the blocking oxides;

~~———~~removing a second portion of each memory cell on a surface opposite the first portion of the memory cell layers to form a plurality of second cavities~~;~~ and expose the blocking oxide;

~~———~~forming a control gate within each of the second cavities; and

~~———~~removing the second oxide material layer after forming the control gate to form an air gap.

2. ~~——~~ The method of claim 1, wherein depositing the charge trap material comprises:

~~———~~depositing the charge trap material on surfaces of the first cavities and on edge surfaces of the insulator layers; and

~~———~~removing a portion of the charge trap material from the edge surfaces of the insulator layers to electrically separate ~~the~~remaining charge trap material in each of the first cavities from the remaining charge trap material in adjacent first cavities.

3. ~~——~~ The method of claim 2, wherein the removing the second oxide material layer comprises performing an isotropic etch process to expose surfaces of ~~a gate~~the first oxide ~~layer deposited on the edge surface of the insulator layers and the charge trap~~ material ~~disposed in the first cavities.~~

layers.

4. The method of claim 1, wherein the memory cell layers comprise a sacrificial layer.

5. The method of claim 4, wherein the sacrificial layer is selected from the group consisting of a polysilicon material, a silicon nitride material, and an oxide material.

6. The method of claim 5, wherein the sacrificial layer comprises an arsenic doped polysilicon material.

7. The method of claim 1, wherein the plurality of first oxide material layers comprise silicon dioxide.

8. The method of claim 7, wherein the second oxide material layer comprises a high wet etch rate oxide material.

9. The method of claim 8, wherein the high wet etch rate oxide material is selected from the group consisting of a tensile oxide material, a boron doped oxide material, a phosphorous doped oxide material, and a borophosphosilicate glass material.

10. The method of claim 1, wherein a thickness of each of the plurality of first oxide material layers and a thickness of the second oxide material layer is about 10 nm or less.

11. A memory device fabrication method, comprising:

forming a hole in a stack of alternating insulator layers and memory cell layers, wherein the insulator layers comprise a nitride material layer disposed between a plurality of oxide material layers;

removing a first portion of each memory cell layer adjacent the hole to form a plurality of first cavities~~;~~ and expose an intermediate portion of the memory cell layers;

performing a radical oxidation process on the intermediate portion of each memory cell layer to form blocking oxides;

depositing a charge trap material in the plurality of first cavities~~;~~ and in contact with the blocking oxides;

———removing a second portion of each memory cell on a surface opposite the first portion of the memory cell layers to form a plurality of second cavities~~;~~ and expose the blocking oxide;

———forming a control gate within each of the second cavities; and

———removing the nitride material layer after forming the control gate to form an air gap between the plurality of oxide material layers.

12.—~~-~~ The method of claim 11, wherein depositing the charge trap material comprises:

———depositing the charge trap material on surfaces of the first cavities and on edge surfaces of the insulator layers; and

———removing a portion of the charge trap material from the edge surfaces of the insulator layers to electrically separate ~~the~~remaining charge trap material in each of the first cavities from the remaining charge trap material in adjacent first cavities.

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13.—~~-~~ The method of claim 12, wherein the removing the nitride material layer comprises performing an isotropic etch process to expose surfaces of ~~a gate oxide layer deposited on the edge surface of the insulator layers and the charge trap material disposed in the first cavities.~~

~~14. A three-dimensional NAND device, comprising:~~
~~a first memory cell coupled to a gate~~ the oxide ~~layer;~~
~~a second memory cell coupled to the gate oxide layer;~~
~~an air gap disposed between the first memory cell and the second~~material layers.

14. The method of claim 11, wherein the memory cell~~; and~~
———layers comprise a sacrificial layer.

15. The method of claim 14, wherein the sacrificial layer is selected from the group consisting of a polysilicon material, a silicon nitride material, and an oxide material.

16. The method of claim 15, wherein the sacrificial layer ~~disposed on surfaces of the first memory cell and the second memory cell adjacent to the air gap.~~

~~15. The device of claim 14, wherein~~ comprises an arsenic doped polysilicon material.

17. The method of claim 11, wherein the plurality of oxide material layers comprise silicon dioxide.

18. The method of claim 17, wherein the nitride material layer comprises silicon

nitride.

19. The method of claim 11, wherein a thickness of ~~the air gap~~each oxide material layer of the plurality of oxide material layers and a thickness of the nitride material layer is about 10 nm or less.

20. The method of claim 11, wherein each of the nitride material layers are in contact with a pair of oxide material layers.