## Claims

What is claimed:

1. A semiconductor device, comprising:

a substrate;

an insulating layer formed over the substrate;

a first conductive layer formed ~~over the insulating layer and~~ into an opening of the insulating layer; and

an interconnect structure extending from the substrate through the opening in the insulating layer covering the first conductive layer, wherein a portion ~~width~~ of the interconnect structure includes a width ~~extending from the substrate is~~ less than ~~a width of~~ the opening in the insulating layer.

2. The semiconductor device of claim 1, further including a second conductive layer formed over the substrate.

3. The semiconductor device of claim 1, wherein the interconnect structure includes a conductive pillar.

4. The semiconductor device of claim 1, wherein the interconnect structure includes a first conductive pad.

5. The semiconductor device of claim 4, wherein the interconnect structure further includes a second conductive pad formed over the first conductive pad.

6. The semiconductor device of claim 4, wherein the interconnect structure further includes a bump material deposited over the first conductive pad.

7. A semiconductor device, comprising:

a substrate including an insulating layer disposed over the substrate;

a first conductive layer formed in an opening of the insulating layer; and

an interconnect structure including a first width within the opening and below a surface of the insulating layer and a second width less than the first width outside the opening of the insulating layer.

8. The semiconductor device of claim 7, further including a second conductive layer formed over the substrate.

9. The semiconductor device of claim 7, wherein the interconnect structure includes a conductive pillar.

10. The semiconductor device of claim 7, wherein the interconnect structure includes a first conductive pad.

11. The semiconductor device of claim 10, wherein the interconnect structure further includes a bump material deposited over the first conductive pad.

12. The semiconductor device of claim 10, wherein the interconnect structure further includes a second conductive pad formed over the first conductive pad.

13. The semiconductor device of claim 12, wherein the second conductive pad is disposed around a perimeter of the first conductive pad or in an interior region of the first conductive pad.

14. A semiconductor device, comprising:

a substrate including an insulating layer disposed over the substrate; and

an interconnect structure including a first width within an opening in the insulating layer and a second width less than the ~~first width outside the~~ opening of the insulating layer.

15. The semiconductor device of claim 14, further including a conductive layer formed in the opening of the insulating layer.

16. The semiconductor device of claim 14, wherein the interconnect structure includes a conductive pillar.

17. The semiconductor device of claim 14, wherein the interconnect structure includes a first conductive pad.

18. The semiconductor device of claim 17, wherein the interconnect structure further includes a second conductive pad formed over the first conductive pad.

19. The semiconductor device of claim 17, wherein the interconnect structure further includes a bump material deposited over the first conductive pad.

20. A semiconductor device, comprising:

a substrate including an insulating layer disposed over the substrate; and

an interconnect structure extending from the substrate through an opening in the insulating layer, wherein the interconnect structure includes a ~~first width within the opening~~

~~in the insulating layer and a second~~ width less than the ~~first width outside the~~ opening of the insulating layer.

21. The semiconductor device of claim 20, further including a conductive layer formed in the opening of the insulating layer.

22. The semiconductor device of claim 20, wherein the interconnect structure includes a conductive pillar.

23. The semiconductor device of claim 20, wherein the interconnect structure includes a first conductive pad.

24. The semiconductor device of claim 23, wherein the interconnect structure further includes a second conductive pad formed over the first conductive pad.

25. The semiconductor device of claim 23, wherein the interconnect structure further includes a bump material deposited over the first conductive pad.