## Description

This invention relates to a deflection circuit with switched mode modulator circuit usable with cathode ray tubes such as television kinescopes.

Active side pincushion correction circuits are known which vary the amplitude of the line scanning current at a vertical rate in a parabolic manner to provide side pincushion correction. In one form of a diode modulator type side pincushion correction circuit, the modulation voltage is developed across a modulator capacitor and applied to the modulator inductor to generate a line repetitive, sawtooth current in the modulator inductor during the entire trace interval. To provide side pincushion correction, a transistor coupled in shunt with the modulator capacitor is operated Class A to discharge the modulator capacitor at a vertical rate in a parabolic manner. Such an example of a diode modulator has several disadvantages. Since the modulating transistor is operated Class A, the transistor dissipates significant power. Additionally, a relatively expensive capacitor is used for developing the modulation voltage.

In another form of a diode modulator, a line rate, switched mode, modulator voltage is applied to a relatively large input choke coupled to the modulator inductor. The choke current is injected into the diode modulator circuit for controlling the amplitude of the line scanning current. The switched mode modulator voltage is varied at a vertical rate in a parabolic manner to modulate the amplitude of the current that is injected into the diode modulator circuit for providing side pincushion correction to the line scanning current. Such an example of a diode modulator also has several disadvantages. In addition to the modulator inductor, a relatively large input choke is used. Furthermore, in some versions of a choke supplied diode modulator, a modulator capacitor is also used as for example in the diode modulator circuit disclosed in US-A-4 140 949.

In accordance with a feature of the invention, a switched mode modulator circuit modulates the line scanning current without the need for either an input choke or a modulator capacitor. Also, by operating the modulator circuit in the switched mode rather than in Class A, resistive losses are kept relatively small.

A switched mode modulator circuit includes a line deflection winding and a trace capacitance. A trace switch is operated at a line rate for applying a trace voltage to the deflection winding to generate line scanning current in the line deflection winding. A deflection retrace capacitance forms a deflection retrace resonant circuit with the deflection winding during the retrace interval to generate a deflection retrace pulse voltage. A modulator inductance is coupled to the trace switch and to the deflection winding. A modulator retrace capacitance is coupled to the modulator inductance and forms a modulator retrace resonant circuit during the retrace interval. A modulator switch is coupled to a voltage supply and to the modulator inductance and is responsive to a line rate signal and to a modulator control signal for switching conductive states at a controllable instant within the line trace interval that varies in accordance with the modulator control signal to thereby modulate the line scanning current.

In the Drawing:

FIGURE 1 illustrates a live (horizontal) deflection circuit suitable for operating a television kinescope and having switched mode side pincushion correction in accordance with the invention and

FIGURE 2 illustrates waveforms associated with the operation of the circuit of FIGURE 1.

In the side pincushion corrected line deflection circuit 10 of FIGURE 1, a regulated direct current B+ supply voltage is applied to the primary winding W1 of a horizontal flyback transformer T1 at a terminal 21. Another terminal of primary winding W1, terminal 22, is coupled to a line trace switch $S_H$, comprising a horizontal output transistor Q1 coupled in parallel with series coupled damper diodes D1 and D2. Paralleling damper diode D1 is a deflection retrace capacitor $C_{RH}$ and a series coupled horizontal deflection winding $L_H$ and S-shaping or trace capacitor $C_t$.

A switched mode side pincushion correction circuit 60, embodying the invention, is coupled to horizontal deflection winding $L_H$ and to trace switch $S_H$ for providing side pincushion correction to line scanning current $i_H$. Side pincushion correction circuit 60 includes a modulator inductor $L_m$ that is coupled to the junction of damper diodes D1 and D2, at a terminal 24, and that is coupled to a modulator switch $S_m$ at a terminal 23. A modulator retrace capacitor $C_{Rm}$ parallels damper diode D2.

Modulator switch $S_m$ includes a transistor switch Q2 that is coupled to a source of DC supply voltage $+V_0$ and that is coupled to modulator inductor $L_m$ at terminal 23. A diode switch D3 parallels transistor switch Q2 and is poled to conduct current in a direction opposite that of transistor Q2. A switched mode control circuit 30 is coupled to the base of transistor Q2 to generate a line rate, switched mode modulator voltage $V_m$ at switch output terminal 23 that is directly applied to modulator inductor $L_m$. Modulator voltage $V_m$ controls the modulator current $i_m$ in modulator inductor $L_m$.

In operation, horizontal output transistor Q1 is switched at a line rate by a horizontal oscillator and driver circuit 20 to generate line scanning current $i_H$

in horizontal deflection winding $L_H$. During the line trace interval, $t_0$-$t_4$, of the waveforms of FIGURE 2, horizontal trace switch $S_H$ is conductive to apply across horizontal deflection winding $L_H$ the trace voltage $V_t$ developed by trace capacitor $C_t$. An upwardly ramping, line scanning current $i_H$, illustrated in solid-line in FIGURE 2b, is developed during the line trace interval.

During the first half of the line trace interval, prior to time $t_1$, the center of trace, line scanning current $L_H$ is negative and flows in damper diode D1. In the first half of trace, the current $i_1$ in flyback transformer primary winding W1 is also negative. Damper diode D2 is, therefore, conductive to provide a path for current $i_1$ from ground to the B+ supply terminal 21 via damper diodes D1 and D2. During the second half of the line trace interval, after time $t_1$, line scanning current $i_H$ is positive, with current flowing out of terminal 22 to horizontal output transistor Q1 and returning to terminal 24 via conducting damper diode D2. Thus, during the entire trace interval, $t_0$-$t_4$, terminals 22 and 24 are essentially at ground potential due to the simultaneous conduction of damper diodes D2 and D1 or damper diode D2 and horizontal output transistor Q1.

In switched mode side pincushion circuit 60, transistor Q2 of modulator switch $S_m$ is operated at a line rate by a switching voltage $V_{b2}$, illustrated in solid-line in FIGURE 2h. Voltage $V_{b2}$ is developed by a control circuit 30 and is applied to the base of transistor Q2 via a resistor 25. At a controlled, variable instant within the line trace interval, at time $t_2$ of FIGURE 2h, for example, switched mode control voltage $V_{b2}$ goes low, turning on transistor Q2. Supply voltage $+V_0$ is applied at terminal 23 to modulator inductor $L_m$, as illustrated by the solid-line modulator voltage $V_m$ of FIGURE 2d. Since terminal 24 during the trace interval is at ground potential, the voltage developed across modulator inductor $L_m$ during the interval $t_2$-$t_4$ equals in magnitude supply voltage $V_0$. An upramping, sawtooth modulator current $i_m$, illustrated in solid-line in FIGURE 2e, is developed in modulator inductor $L_m$ between times $t_2$-$t_4$, reaching a peak magnitude $I_m$ at time $t_4$, the end of the trace interval. The peak magnitude $I_m$ is established by the turn-on time within the trace interval of modulator transistor switch Q2. A later turn-on time, for example, results in a lower peak magnitude current for modulator current $i_m$ at the end of the horizontal trace interval.

Near the end of the horizontal trace interval, horizontal oscillator and driver circuit 20 applies a reverse biasing voltage to the base of horizontal output transistor Q1 to terminate conduction of the transistor near time $t_4$ of FIGURE 2, the beginning of the horizontal retrace interval, $t_4$-$t_5$. During horizontal retrace, line deflection current $i_H$ and modulator current $i_m$ flow in deflection retrace capacitor $C_{RH}$ and modulator retrace capacitor $C_{Rm}$, respectively, reverse biasing damper diodes D1 and D2.

During horizontal retrace, horizontal deflection winding $L_H$ and deflection retrace capacitor $C_{RH}$ form a deflection retrace resonant circuit 40. Also, during this interval, modulator switch $S_m$ advantageously remains conductive enabling modulator inductor $L_m$ and modulator retrace capacitor $C_{Rm}$ to form a modulator retrace resonant circuit 50. The modulator retrace current flows in modulator switch $S_m$.

The resonance frequency of modulator retrace circuit 50 is advantageously selected to be approximately that of the horizontal retrace frequency of deflection retrace circuit 40. Thus, both horizontal deflection current $i_H$ and modulator $i_m$ undergo one-half cycle of resonant oscillation in their respective retrace resonant circuits during approximately the same interval, $t_4$-$t_6$, as illustrated in solid-line in FIGURES 2b and 2e.

The one-half cycle of resonant oscillation of currents $i_H$ and $i_m$ generate retrace pulse voltages $V_{RH}$ and $V_{Rm}$ in respective retrace capacitors $C_{RH}$ and $C_{Rm}$, as illustrated in solid-line in FIGURES 2c and 2f, respectively. The peak amplitudes, $V_{PH}$ and $V_{Pm}$, of retrace pulse voltages $V_{RH}$ and $V_{Rm}$, respectively, occur near the center of retrace, at time $t_5$, when currents $i_H$ and $i_m$ reverse direction.

After time $t_5$, the center of retrace, modulator current $i_m$ is negative and is returned to the $+V_0$ supply via the now conducting diode D3 of modulator switch $S_m$, reaching a negative peak value of substantially $-I_m$ at the end of retrace. Also at the end of retrace, near time $t_6$, retrace capacitors $C_{RH}$ and $C_{Rm}$ have fully discharged, enabling damper diodes D1 and D2 to become conductive, thereby initiating the beginning of the next horizontal trace interval.

When damper diode D2 begins conducting negative modulator current $i_m$ at the beginning of horizontal trace, near time $t_6$ of FIGURE 2e, terminal 24 again becomes grounded. The negative modulator current $i_m$ flows from ground to the $+V_0$ supply via damper diode D2 and diode D3 of modulator switch $S_m$. After time $t_6$, the beginning of the next horizontal trace interval, switched mode correction voltage $V_m$, of FIGURE 2d, is developed across modulator inductor $L_m$. Modulator current $i_m$, after time $t_6$, becomes an upramping, negative sawtooth current. Also, near time $t_6$, switched mode control circuit 30 generates the upper level of switching voltage $V_{b2}$ of FIGURE 2h, thereby placing transistor Q2 of switch $S_m$ in a cutoff condition. Thus, when modulator current $i_m$ reaches zero at time $t_8$ of FIGURE 2e, modulator switch $S_m$ be-

comes open-circuited due to the reverse biasing of diode D3 and the cutoff of transistor Q2.

No current flows in modulator inductor $L_m$ from time $t_8$ until time $t_{10}$, when transistor Q2 is again turned-on to advantageously apply modulator voltage $V_m$ directly to modulator inductor $L_m$. During the interval, $t_8$-$t_{10}$, modulator switch $S_m$ interrupts the current path that trace switch $S_H$ provides for modulator current $i_m$ between voltage source $+V_0$ and modulator inductor $L_m$. During this interval, the potential developed across modulator inductor $L_m$ between terminals 23 and 24 is zero, with the two terminals being maintained essentially at ground potential by conduction in trace switch $S_m$.

Although switched mode control circuit 30 turns off transistor Q2 at the end of retrace near time $t_0$, the exact turn-off instant is not critical, provided the turn-off instant occurs when modulator current $i_m$ is negative. Thus control circuit 30 may turn off transistor Q2 at any instant after time $t_5$, the center of retrace, and before time $t_8$, when the negative modulator current $i_m$ has decreased in magnitude to zero.

Switched mode side pincushion correction circuit 60 modulates the amplitude of line scanning current $i_H$ by modulating the duty cycle of modulator voltage $V_m$. The DC component, $V_{m0}$, of modulator voltage $V_m$ of FIGURE 2d, is controlled by and related to the duty cycle of modulator voltage $V_m$. Modulator inductor $L_m$, horizontal deflection winding $L_H$ and flyback transformer primary winding W1 are equivalent to DC short-circuit paths. Thus, the DC value of the voltage at terminal 24 equals $V_{m0}$, the DC value at terminal 23, and the DC value at terminal 22 and at the top terminal of trace capacitor $C_t$ equals the B+ voltage at terminal 21.

The average trace voltage $V_t$ developed across capacitor $C_t$, which determines the peak amplitude $I_{PH}$ of line scanning current $i_H$, equals the difference between the B+ voltage and the average modulator voltage $V_{m0}$. Decreasing the average modulator voltage $V_{m0}$ increases the average trace voltage and the amplitude of the line scanning current. Increasing the average modulator voltage $V_{m0}$ decreases the average trace voltage and the amplitude of the line scanning current.

The dashed-line waveforms of FIGURES 2b-2f and 2h illustrate operation of side pincushion correction circuit 60 in a manner that produces an increased amplitude line deflection current $i_H$, such as when scanning the center lines of a raster field. Control circuit 30 initiates the generation of the lower level of switching control voltage $V_{b2}$ at a retarded instant, $t_3$, within the horizontal trace interval, as illustrated in dashed-line in FIGURE 2h.

Modulator current $i_m$, illustrated in dashed-line in FIGURE 2e, begins to increase in an upramping manner from the zero current level at the retarded instant $t_3$. Thus, when retrace begins at time $t_4$, modulator current $i_m$ has reached a peak current level $I'_m$ that is smaller in magnitude than the peak level $I_m$ of the corresponding solid-line waveform. Because the peak magnitude of modulator current $i_m$ is smaller, the modulator retrace pulse voltage $V_{Rm}$, illustrated in dashed-line in FIGURE 2f, that is developed during horizontal retrace between times $t_4$-$t_6$, attains a lower peak magnitude $V'_{Pm}$ than the corresponding solid-line waveform.

At the beginning of the next horizontal trace interval, modulator current $i_m$ begins it s upward ramping from a negative level, $-I'_{m'}$, that is of a peak magnitude that is smaller than in the corresponding solid-line waveform. Modulator current $i_m$ reaches the zero current level at the earlier instant $t_7$ within the horizontal trace interval. At time $t_7$, diode D3 of modulator switch $S_m$ becomes reversed biased, open-circuiting the modulator switch and initiating the lower level of modulator voltage $V_m$, as illustrated in dashed-line in FIGURE 2d.

By turning on modulator switch $S_m$ at the retarded instant $t_3$ within the horizontal trace interval, the upper, positive level of modulator voltage $V_m$ is developed for a shorter interval, $t_3$-$t_7$, resulting in a lower average modulator voltage $V'_{m0}$ of FIGURE 2d. The lower average voltage $V'_{m0}$ produces a higher average trace voltage $V_t$ across trace capacitor $C_t$. The higher average trace voltage produces a higher amplitude line scanning current of magnitude $I'_{PH}$, as illustrated in dashed-line in FIGURE 2b. The higher amplitude line scanning current produces during the horizontal retrace interval a higher amplitude retrace pulse voltage $V_{RH}$ having a peak magnitude $V'_{PH}$, illustrated in dashed-line in FIGURE 2c.

The retrace pulse voltage $V_R$ that is applied to flyback transformer primary winding W1 is illustrated in FIGURE 2a. Flyback transformer retrace pulse voltage $V_R$ equals the sum of the deflection retrace pulse voltage $V_{RH}$ and the modulator retrace pulse voltage $V_{RM}$. The sum remains unchanged even though the individual pulse components are varied by side pincushion correction circuit 60. The sum remains unchanged because the pulse components vary in an inverse or complementary relationship. Thus, the modulation of line scanning current $i_H$ does not affect the amplitude of flyback transformer retrace pulse voltage $V_R$, which amplitude remains constant and is determined by the B+ supply voltage developed at terminal 21. Retrace pulse voltage $V_R$ is used to generate the ultor accelerating potential at a terminal U of a high voltage circuit 43 that is coupled to a high voltage winding W2 of flyback transformer T1. Retrace pulse voltage $V_R$ is also used to energize other, eg

television receiver, load circuits, illustrated schematically in FIGURE 1 by the block 44 coupled to a winding W3 of flyback transformer T1.

Control circuit 30 generates switched mode control voltage $V_{b2}$ in the following manner. A positive horizontal flyback voltage pulse 41 developed by a winding W4 of flyback transformer T1 is differentiated by a differentiating network comprising capacitor 36 and resistors 37 and 38. The differentiated flyback pulse is applied to the base of a PNP transistor Q3. The trailing edge of horizontal flyback pulse 41 produces a negative spike or pulse near time $t_0$ of FIGURE 2 that turns on transistor Q3 and charges a capacitor 35 of a ramp generating network 45 to a voltage $V_1$, as illustrated in FIGURE 2g by the voltage $V_{Hs}$ developed across capacitor 35.

The short duration negative going spike decays rapidly near time $t_6$ to turn of transistor Q3 shortly after it is turned on. Thus, near time $t_6$, capacitor 35 begins to discharge through a resistor 34 of ramp generating network 45. Voltage $V_{Hs}$ of FIGURE 2g is therefore a ramp voltage that decreases to the lower voltage level $V_2$ by time $t_6$, when the negative going spike produced by the subsequent horizontal flyback pulse 41 resets the ramp.

Horizontal ramp voltage $V_{Hs}$ is AC coupled to the base of a control transistor Q5 via an emitter-follower transitor Q4, the wiper arm of an emitter resistor 33, a DC blocking capacitor 31 and a summing resistor 32. Horizontal ramp voltage $V_{Hs}$ is summed at the base of transistor Q5 with a vertical (field) rate parabola voltage 42, conventionally derived, that is AC coupled to the base of the transistor via a resistor 28 and a DC blocking capacitor 29. DC bias for the base of transistor Q5 is provided by the $+V_0$ supply that is coupled to the transistor base via a horizontal size control potentiometer 26 and a resistor 27.

The collector of control transistor Q5 is coupled to the $+V_0$ supply via a resistor 39 and is directly coupled to the base of an inverting transistor Q6. The collector of inverting transistor Q6 is coupled to the $+V_0$ supply via a resistor 47 and is coupled to the base of modulator switch transistor Q2 via resistor 25. Switched mode control voltage $V_{b2}$ is developed at the collector of inverting transistor Q6.

In operation, when horizontal ramp voltage $V_{Hs}$ is reset to its upper voltage level $V_1$ at time $t_0$, the positive going edge of the ramp is coupled to the base of control transistor Q5, turning the transistor on and turning off transistor Q6. The upper voltage level of switched mode control voltage $V_{b2}$ of FIGURE 2h is thereby developed to place modulator switch transistor Q2 in a reverse biased state.

At a controllable instant within the horizontal trace interval, AC-coupled ramp voltage $V_{Hs}$ has decreased to a level sufficient to cutoff control transistor Q5, enabling the lower level of switched mode control voltage $V_{b2}$ to be generated. Modulator switch transistor Q2 is thereby turned on and applies the $+V_0$ voltage directly to modulator inductor $L_m$.

The time within horizontal trace when control transistor Q5 is turned off is determined by the level that vertical parabola voltage 42 assumes during a given horizontal deflection cycle. Near the center of vertical raster scanning, vertical parabola voltage 42 attains a level that provides a bias to control transistor Q5 that permits horizontal ramp voltage $V_{Hs}$ to turn off the transistor at the relatively retarded instant $t_3$ when the ramp voltage has decreased to a voltage level $V_b$ of FIGURE 2g. Side pincushion correction circuit 60 thereby propduces a relatively high amplitude line scanning current $i_H$. Near the top and bottom of vertical raster scanning, vertical parabola voltage 42 is at a relatively low voltage level, permitting horizontal ramp voltage $V_{Hs}$ todecrease to a voltage level $V_a$ before turning off control transistor Q5 at the relatively advanced instant $t_2$. Side pincushion correction circuit 60 thereby produces a relatively small amplitude line scanning current.

Other modulation control voltages, in addition to or in place of vertical parabola voltage 42, may be coupled to the base of transistor Q5 to modulate the amplitude of line scanning current $i_H$. For example, a modulation control voltage representative of beam current loading of ultor terminal U may be used to correct for raster width variations with ultor loading.

As described, side pincushion correction circuit 60 provides modulation of line deflection current $i_H$ by advantageously operating in the switched mode while avoiding the use of a modulator capacitor. Switched mode modulator voltage $V_m$ is applied directly to modulator inductor $L_m$. Modulator inductor $L_m$ functions to integrate the rectangular wave voltage $V_m$, thereby avoiding the use for that purpose of an additional, large valued input choke.

It is also a feature of the circuit that the modulator switch $S_m$ controllably decouples modulator inductor $L_m$ from line deflection switch $S_H$ and supply voltage $+V_0$ for a variable period during the horizontal trace interval, thereby reducing the amount of circulating current flowing between modulator inductor $L_m$ and trace switch $S_H$.

Additionally, because modulator switch $S_m$ is conductive during the entirety of horizontal retrace, deflection retrace resonant circuit 40 and modulator retrace resonant circuit 50 are advantageously coupled together by modulator switch $S_m$ in a balanced bridge configuration during the entirety of horizontal retrace. This bridge configuration avoids undesirable retrace time modulation of deflection

retrace pulse voltage $V_{RH}$ and flyback transformer retrace pulse voltage $V_R$. The bridge configuration also exists during trace but only when modulator switch $S_m$ is conductive. One branch is the series coupled deflection winding $L_H$ and trace capacitor $C_t$. Another branch is the series coupled modulator inductor $L_m$ and the $+V_o$ supply voltage source.

## Claims

1. A deflection circuit with a switched mode modulator circuit, comprising:

a line deflection winding ($L_H$);

a trace capacitance ($C_t$) for developing a line trace voltage;

a trace switch ($S_H$) coupled to said line deflection winding ($L_H$) and said trace capacitance ($C_t$) and operated at a line rate for applying said trace voltage to said line deflection winding ($L_H$) during a line trace interval ($t_0$-$t_4$) to generate a line scanning current ($i_M$) in said line deflection winding ($L_H$);

a deflection retrace capacitance ($C_{RH}$) coupled to said line deflection winding ($L_H$) for forming a deflection retrace resonant circuit (40) during a line retrace interval ($t_4$-$t_5$) to generate a deflection retrace pulse voltage (VR);

a modulator inductance ($L_m$) coupled to said trace switch ($S_H$) and to said line deflection winding ($L_H$);

a modulator retrace capacitance ($C_{Rm}$) coupled to said modulator inductance ($L_m$) for forming a modulator retrace resonant circuit (50) to generate a modulator retrace current in said modulator inductance ($L_m$) during said line retrace interval ($t_4$-$t_5$);

a source ($V_o$) of supply voltage; and

a modulator switch ($S_m$) coupled to said trace switch ($S_H$), to said source ($V_o$) and to said modulator inductance ($L_m$) and responsive to a line rate signal ($V_{Hs}$) and to a modulator control signal (42) for switching between conductive and nonconductive states at a controllable instant ($t_2$) within said line trace interval that varies in accordance with said modulation control signal (42) to generate a switched mode modulation voltage that is directly applied to said modulator inductance ($L_m$) for modulating said line scanning current ($i_H$) in accordance with said modulator control signal (42);

characterized in that said modulator switch ($S_m$) couples said source ($V_o$) of supply voltage to said modulator inductance ($L_m$) and is conductive during said line retrace interval to provide therethrough a current path for said modulator retrace current.

2. A circuit according to Claim 1 characterized in that said modulator inductance ($L_m$) integrates said switched mode modulation voltage into said modulator current.

3. A circuit according to Claim 1 characterized in that, during said trace interval, said trace switch ($S_H$) in cooperation with said modulator switch ($S_m$) develops said supply voltage ($V_o$) between first (23) and second (24) terminals of said modulator inductance ($L_m$) when said modulator switch ($S_m$) is in one of two conductive states and maintains the two terminals (23,24) at the same potential when said modulator switch ($S_m$) is in the other conductive state.

4. A circuit according to Claim 1 characterized in that said modulator switch ($S_m$) conducts modulator current in said modulator inductance ($L_m$) during the entirety of said retrace interval and during the beginning and ending portions of said trace interval and prevents current from flowing in said modulator inductance ($L_m$) during said variable period within said trace interval.

5. A circuit according to Claim 4 characterized in that said modulator switch ($S_m$) includes a first element (Q2) that conducts said modulator current during the ending portion of said trace interval and during the beginning portion of said retrace interval and includes a second element (D3) that conducts said modulator current during the remaining portion of said retrace interval and during said beginning portion of said trace interval.

6. A circuit according to Claim 4 characterized in that said modulator switch ($S_m$) switches into conduction at said controllable instant for applying said supply voltage ($V_o$) to said modulator inductance ($L_m$) to initiate an upramping portion of said modulator current ($i_m$).

7. A circuit according to Claim 4 characterized in that said modulator switch ($S_m$) interrupts during said variable period a current path for said modulator current ($i_m$) provided by said trace switch ($S_H$) between said source ($V_o$) and said modulator inductance ($L_m$).

8. A circuit according to Claim 1 characterized in that said modulator switch ($S_m$), when conductive, directly applies said supply voltage ($V_o$) to a first terminal (23) of said modulator inductance ($L_m$) and, when nonconductive, decouples said modulator inductance ($L_m$) with re-

retrace pulse voltage $V_{RH}$ and flyback transformer retrace pulse voltage $V_R$. The bridge configuration also exists during trace but only when modulator switch $S_m$ is conductive. One branch is the series coupled deflection winding $L_H$ and trace capacitor $C_t$. Another branch is the series coupled modulator inductor $L_m$ and the $+V_o$ supply voltage source.

## Claims

1. A deflection circuit with a switched mode modulator circuit, comprising:

a line deflection winding ($L_H$);

a trace capacitance ($C_t$) for developing a line trace voltage;

a trace switch ($S_H$) coupled to said line deflection winding ($L_H$) and said trace capacitance ($C_t$) and operated at a line rate for applying said trace voltage to said line deflection winding ($L_H$) during a line trace interval ($t_0$-$t_4$) to generate a line scanning current ($i_M$) in said line deflection winding ($L_H$);

a deflection retrace capacitance ($C_{RH}$) coupled to said line deflection winding ($L_H$) for forming a deflection retrace resonant circuit (40) during a line retrace interval ($t_4$-$t_6$) to generate a deflection retrace pulse voltage (VR);

a modulator inductance ($L_m$) coupled to said trace switch ($S_H$) and to said line deflection winding ($L_H$);

a modulator retrace capacitance ($C_{Rm}$) coupled to said modulator inductance ($L_m$) for forming a modulator retrace resonant circuit (50) to generate a modulator retrace current in said modulator inductance ($L_m$) during said line retrace interval ($t_4$-$t_6$);

a source ($V_o$) of supply voltage; and

a modulator switch ($S_m$) coupled to said trace switch ($S_H$), to said source ($V_o$) and to said modulator inductance ($L_m$) and responsive to a line rate signal ($V_{Hs}$) and to a modulator control signal (42) for switching between conductive and nonconductive states at a controllable instant ($t_2$) within said line trace interval that varies in accordance with said modulation control signal (42) to generate a switched mode modulation voltage that is directly applied to said modulator inductance ($L_m$) for modulating said line scanning current ($i_H$) in accordance with said modulator control signal (42):

characterized in that said modulator switch ($S_m$) couples said source ($V_o$) of supply voltage to said modulator inductance ($L_m$) and is conductive during said line retrace interval to provide therethrough a current path for said modulator retrace current.

2. A circuit according to Claim 1 characterized in that said modulator inductance ($L_m$) integrates said switched mode modulation voltage into said modulator current.

3. A circuit according to Claim 1 characterized in that, during said trace interval, said trace switch ($S_H$) in cooperation with said modulator switch ($S_m$) develops said supply voltage ($V_o$) between first (23) and second (24) terminals of said modulator inductance ($L_m$) when said modulator switch ($S_m$) is in one of two conductive states and maintains the two terminals (23,24) at the same potential when said modulator switch ($S_m$) is in the other conductive state.

4. A circuit according to Claim 1 characterized in that said modulator switch ($S_m$) conducts modulator current in said modulator inductance ($L_m$) during the entirety of said retrace interval and during the beginning and ending portions of said trace interval and prevents current from flowing in said modulator inductance ($L_m$) during said variable period within said trace interval.

5. A circuit according to Claim 4 characterized in that said modulator switch ($S_m$) includes a first element (Q2) that conducts said modulator current during the ending portion of said trace interval and during the beginning portion of said retrace interval and includes a second element (D3) that conducts said modulator current during the remaining portion of said retrace interval and during said beginning portion of said trace interval.

6. A circuit according to Claim 4 characterized in that said modulator switch ($S_m$) switches into conduction at said controllable instant for applying said supply voltage ($V_o$) to said modulator inductance ($L_m$) to initiate an upramping portion of said modulator current ($i_m$).

7. A circuit according to Claim 4 characterized in that said modulator switch ($S_m$) interrupts during said variable period a current path for said modulator current ($i_m$) provided by said trace switch ($S_H$) between said source ($V_o$) and said modulator inductance ($L_m$).

8. A circuit according to Claim 1 characterized in that said modulator switch ($S_m$), when conductive, directly applies said supply voltage ($V_o$) to a first terminal (23) of said modulator inductance ($L_m$) and, when nonconductive, decouples said modulator inductance ($L_m$) with re-

spect to said source of supply voltage ($V_o$).

9. A circuit according to Claim 8 characterized in that said trace switch ($S_H$) directly couples a second terminal (24) of said modulator inductance ($L_m$) to said source of supply voltage during the entirety of said trace interval when said trace switch ($S_H$) is conductive and wherein a resonant current from said modulator retrace capacitance ($C_{Rm}$) flows between said first (23) and second (24) terminals of said modulator inductance ($L_m$) during said retrace interval when said trace switch ($S_H$) is nonconductive.

10. A circuit according to Claim 9 characterized in that, during said trace interval, said trace switch ($S_H$) in cooperation with said modulator switch ($S_m$) develops said supply voltage ($V_o$) between said first (23) and second (24) terminals of said modulator inductance ($L_m$) when said modulator switch ($S_m$) is conductive and maintains the two terminals (23,24) at the same potential when said modulator switch ($S_m$) is nonconductive.

11. A circuit according to Claim 1 characterized in that said modulator switch ($S_m$) is conductive during the entirety of said retrace interval to couple via said modulator switch said deflection retrace resonant circuit (40) to said modulator retrace resonant circuit (50) in a bridge configuration.

12. A circuit according to Claim 11 characterized in that the resonance frequencies of said deflection (40) and modulator (50) retrace resonant circuits are substantially the same.

13. A circuit according to Claim 12 charaterized in that said trace switch ($S_H$) comprises a first damper diode (D1) paralleling said deflection retrace capacitance ($C_{RH}$), a second damper diode (D2) coupled to said first damper diode (D1) and to said modulator inductance ($L_m$) and paralleling said modulator retrace capacitance ($C_{Rm}$), and a switching element (Q1) having a first main current terminal (collector) coupled to said first damper diode (D1) and to said deflection winding ($L_H$) and having a second main current terminal (emitter) coupled to said second damper diode (D2) and to said source of supply voltage (ground).

14. A deflection circuit with a switched mode side pincushion correction circuit, comprising:

a line deflection winding ($L_H$);

a trace capacitance ($C_t$) for developing a line trace voltage;

trace switching means ($S_H$) coupled to said line deflection winding ($L_H$) and said trace capacitance ($C_t$) and operated at a line rate for applying said trace voltage to said line deflection winding ($L_H$) during a line trace interval to generate a line scanning current in said line deflection winding ($L_H$);

a deflection retrace capacitance ($CR_H$) coupled to said line deflection winding ($L_H$) for forming a deflection retrace resonant circuit (40) during a line retrace interval to generate a deflection retrace pulse voltage (VR);

a modulator inductance ($L_m$) coupled to said trace switching means ($S_H$) and to said line deflection winding ($L_H$);

a modulator retrace capacitance ($C_{Rm}$) coupled to said modulator inductance ($L_m$) for forming a modulator retrace resonant circuit (50) during said line retrace interval;

a source ($V_o$) of supply voltage; and

modulator switching means ($S_m$) coupled to said trace switching means ($S_H$), to said source ($V_o$) and to said modulator inductance ($L_m$) and responsive to line ($V_{Hs}$) and field (42) rate signals for applying said supply voltage ($V_o$) to said modulator inductance ($L_m$) at a variable instant ($t_2$) within said line trace interval ($t_0$-$T_4$) that varies in accordance with said field rate signal (42) to provide a side pincushion corrected line scanning current, characterized in that said modulator switching means ($S_m$) couples said source ($V_o$) of supply voltage to said modulator inductance ($L_m$), to generate an upramping modulator current in said modulator inductance ($L_m$) that flows from said source ($V_o$) of supply voltage and that starts at a zero current level at said variable instant to reach at the end of said trace interval a peak magnitude that changes in accordance with said field rate signal (42).

15. A circuit according to Claim 14 characterized in that said modulator switching means ($S_m$) is conductive during the entirety of said retrace interval to return said modulator current to said source ($V_o$) of supply voltage during the ending portion of said retrace interval and during the beginning portion of said trace interval until said modulator current reaches a zero current level at a second variable instant within said trace interval that is earlier than the first mentioned variable instant and that varies in accordance with said field rate signal (42).

16. A circuit according to Claim 15 characterized in that the duration between the two aforementioned variable instants also varies in accor-

dance with said field rate signal (42).

17. A deflection circuit with a switched mode side pincushion correction circuit, comprising:

a line deflection winding ($L_H$);

a trace capacitance ($C_t$) for developing a line trace voltage;

trace switching means ($S_H$) coupled to said line deflection winding ($L_H$) and said trace capacitance ($C_t$) and operated at a line rate for applying said trace voltage to said line deflection winding ($L_H$) during a line trace interval to generate a line scanning current in said line deflection winding ($L_H$);

a deflection retrace capacitance ($CR_H$) coupled to said line deflection winding ($L_H$) for forming a deflection retrace resonant circuit (40) during a line retrace interval to generate a deflection retrace pulse voltage;

a modulator inductance ($L_m$) coupled to said trace switching means ($S_H$) and to said line deflection winding ($L_H$);

a modulator retrace capacitance ($C_{Rm}$) coupled to said modulator inductance ($L_m$) for forming a modulator retrace resonant circuit (50) during said line retrace interval;

a source ($V_o$) of supply voltage; and

modulator switching means ($S_m$) coupled to said trace switching means ($S_H$), to said source ($V_o$) and to said modulator inductance ($L_m$), and being responsive to line ($V_{Hs}$) and field (42) rate signals for switching between conductive and nonconductive states at a controllable instant within said line trace interval that varies in accordance with said field rate signal (42) to provide a side pincushion corrected line scanning current, characterized in that said modulator switching means ($S_m$) couples said source ($V_o$) to said modulator inductance ($L_m$), and interrupts a modulator current path through said modulator inductance ($L_m$) and said trace switching means ($S_H$) for a variable period within said line trace interval in accordance with said field rate signal (42).

18. A deflection circuit with a switched mode modulator circuit, comprising:

a line deflection winding ($L_H$);

a trace switch ($S_H$) coupled to said line deflection winding ($L_H$) for generating a line scanning current (iH) in said line deflection winding ($L_H$);

a deflection retrace capacitance ($CR_H$) coupled to said line deflection winding ($L_H$) for forming a deflection retrace resonant circuit (40) during a line retrace interval to generate a deflection retrace pulse voltage (VR);

a modulator inductance ($L_m$) coupled to said trace switch ($S_H$) and to said line deflection winding ($L_H$);

a modulator retrace capacitance ($C_{Rm}$) coupled to said modulator inductance ($L_m$) for forming a modulator retrace resonant circuit (50) during said line retrace interval; and

a source ($V_o$) of DC supply voltage;

characterized by

a bidirectionally conductive modulator switch ($S_m$) coupled to said source ($V_o$) and to said modulator inductance ($L_m$) for generating a bidirectional current between said source ($V_o$) and said modulator inductance ($L_H$) via said modulator switch ($S_m$), said modulator switch ($S_m$) being responsive to a line rate signal ($V_{Hs}$) and to a modulator control signal (42) for switching between conductive and nonconductive states at a controllable instant within said line scanning interval that varies in accordance with said modulation control signal (42) for modulating said bidirectional current in accordance with said modulation control signal.

**Patentansprüche**

1. Ablenkschaltung mit einer in Schalterbetrieb arbeitsfähigen/ arbeitenden Modulatorschaltung (kurz: Schalt-Modulator)
   - mit einer Zeilen-Ablenkwicklung ($L_H$);
   - mit einer Hinlauf-Kapazität ($C_t$) zur Erzeugung einer Zeilen-Hinlaufspannung;
   - mit einem Hinlaufschalter ($S_H$), welcher mit der Zeilen-Ablenkwicklung ($L_H$) und der Hinlauf-Kapazität ($C_t$) gekoppelt ist und mit einer Zeilenrate - zum Anlegen der Hinlaufspannung an die Ablenkwicklung ($L_H$) während eines Zeilen-Hinlaufintervalles ($t_0$-$t_4$)
   - betreibbar ist, womit in der Zeilen-Ablenkwicklung ($L_H$) ein zeilenabtastender (line scanning) Strom ($i_M$) erzeugbar ist;
   - mit einer Ablenk-Rücklaufkapazität ($C_{RH}$), welche mit der Zeilen-Ablenkwicklung ($L_H$) - unter Bildung einer Ablenk-Rücklauf-Resonanzschaltung (40) während eines Zeilen-Rücklaufintervalls ($t_4$-$t_6$) - gekoppelt ist, womit ein Ablenk-Rücklauf-Spannungspuls ($V_R$) bildbar ist;
   - mit einer Modulator-Induktivität ($L_m$), welche mit dem Hinlauf-Schalter ($S_H$) und der Zeilen-Ablenkwicklung ($L_H$) gekoppelt ist; mit einer Modulator-Rücklaufkapazität ($C_{Rm}$), welche mit der Modulator-Induktivität ($L_m$)
   - unter Bildung einer Modulator-Rücklauf-Resonanzschaltung (50) - gekopppelt ist, womit ein Modulator-Rücklaufstrom in der Modulator-Induktivität ($L_m$) während

des Zeilen-Rücklaufintervalles ($t_4$-$t_6$) erzeugbar ist;

- mit einer Versorgungsspannunsquelle ($V_0$);
- mit einem Modulatorschalter ($S_m$), der mit dem Hinlaufschalter ($S_H$), der Quelle ($V_0$) und der Modulatorinduktivität ($L_M$) gekopppelt ist und abhängig von einem Zeilenratensignal ($V_{HS}$) und einem Modulator-Steuersignal (42) von leitenden zu nitchtleitenden Zuständen an einem steuerbaren Zeitpunkt ($t_2$), innerhalb des - sich in Übereinstimmung mit dem Modulator-Steuersignal (42) ändernden - Zeilenhinlaufintervalles, schaltet, wodurch eine Schaltbetriebs-Modulatorspannung erzeugbar ist, die direkt an die Modulatorinduktivität ($L_m$) anlegbar ist zur Modulation des Zeilenabtast-Stromes ($i_H$) abhängig von dem Modulator-Steuersignal (42);

**dadurch gekennzeichnet,**
daß der Modulatorschalter ($S_m$) die Versorgungsspannungsquelle ($v_0$) mit der Modulatorinduktivität ($L_m$) koppelt und während des Zeilenrücklaufintervalls leitet, um einen Strompfad für den Modulator Rücklaufstrom zu bilden.

2. Schaltung nach Anspruch 1,
**dadurch gekennzeichnet,**
daß die Modulatorinduktivität ($L_m$) die geschaltete Modulatorspannung zum Modulatorstrom integriert.

3. Schaltung nach Anspruch 1,
**dadurch gekennzeichnet,**
daß der Hinlaufschalter ($S_H$) in Kooperation mit dem Modulatorschalter ($S_m$) während des Hinlaufintervalles die Versorgungsspannung ($V_0$) zwischen erstem (23) und zweitem (24) Anschluß der Modulatorinduktivität ($L_m$) anglet, wenn der Modulatorschalter ($S_m$) in einem von zwei leitenden Zuständen ist und die beiden Anschlüsse (23, 24) auf gleichen Potential hält, wenn der Modulatorschalter ($S_m$) in dem anderen leitenden Zustand ist.

4. Schaltung nach Anspruch 1,
**dadurch gekennzeichnet,**
daß der Modulatorschalter ($S_m$) den Modulatorstrom der Modulatorinduktivität ($L_m$) währen der Gesamtheit des Rücklaufintervalles und während des Anfangs- und Endabschnitts des Hinlaufintervalls führt und die Stromführung der Modulatorinduktivität ($L_m$) verhindert, während des variablen Abschnitts innerhalb des Hinlaufintervalls.

5. Schaltung nach Anspruch 4,
**dadurch gekennzeichnet,**
daß der Modulatorschalter ($S_m$) ein erstes Element (Q2) aufweist, welches den Modulatorstrom während des Endabschnitts des Hinlaufintervalls und während des Anfgangsabschnitts des Rücklaufintervalls führt und ein zweites Element (D3) aufweist, welches den Modulatorstrom während des verbleibenden Abschnitts des Rücklaufintervalls und während des Anfangsabschnitts des Hinlaufintervalls führt.

6. Schaltung nach Anspruch 4,
**dadurch gekennzeichnet,**
daß der Modulatorschalter ($S_m$) zu dem steuerbaren Zeitpunkt leitfähig wird, um die Versorgungsspannung ($V_0$) an die Modulatorinduktivität ($L_m$) anzulegen, womit ein aufwärtssteigender Abschnitt des Modulatorstromes ($i_m$) begonnen wird.

7. Schaltung nach Anspruch 4,
**dadurch gekennzeichnet,**
daß der Modulatorschalter ($S_m$) einen - von dem Hinlaufschalter ($S_H$) zwischen der Quelle ($V_0$) und der Modulatorinduktivität ($L_m$) gebildeten - Strompfad für den Modulatorstrom ($i_m$) während des variablen Abschnitts unterbricht.

8. Schaltung nach Anspruch 1,
**dadurch gekennzeichnet,**
daß der Modulatorschalter ($S_m$) im leitfähigen Zustand direkt die Versorgungsspannung ($V_0$) an einen ersten Anschluß (23) der Modulatorinduktivität ($L_m$) anlegt und im nichtleitenden Zustand die Modulatorinduktivität ($L_m$) von der Versorgungsspannungsquelle ($V_0$) abkoppelt.

9. Schaltung nach Anspruch 8,
**dadurch gekennzeichnet,**
daß der Hinlaufschalter ($S_H$) einen zweiten Anschluß (24) der Modulatorinduktivität ($L_m$) direkt mit der Versorgungsspannunsquelle während der Gesamtheit des Hinlaufintervalles koppelt, wenn der Hinlaufschalter ($S_H$) leitet und wobei ein Resonanzstrom der Modulator-Rücklaufkapazität ($C_{Rm}$) zwischen dem ersten (23) und dem zweiten (24) Anschluß der Modulatorinduktivität ($L_m$) während des Rücklaufintervalles bei nichtleitendem Hinlaufschalter ($S_H$) fließt.

10. Schaltung nach Anspruch 9,
**dadurch gekennzeichnet,**
daß während des Hinlaufintervalles der Hinlaufschalter ($S_H$) in Kooperation mit dem Modulatorschalter ($S_m$) die Versorgungsspannung ($V_0$) zwischen dem ersten (23) und zweiten (24) Anschluß der Modulatorinduktivität ($L_m$) bildet,

wenn der Modulatorschalter ($S_m$) leitet und die beiden Anschlüsse (23, 24) auf gleichem Potential hält, wenn der Modulatorschalter ($S_m$) nicht leitet.

11. Eine Schaltung nach Anspruch 1, **dadurch gekennzeichnet,** daß der Modulatorschalter ($S_m$) während der Gesamtheit des Rücklaufintervalles leitet, wodurch die Ablenk-Rücklaufresonanzschaltung (40) über ihn ($S_m$) an die Modulator-Rücklaufresonanzschaltung (50) in Brückenkonfiguration gekoppelt wird.

12. Schaltung nach Anspruch 11, **dadurch gekennzeichnet,** daß die Resonanzfrequenzen des Ablenk- (40) und Modulator- (50) Rücklaufresonanzschaltkreises im wesentlichen übereinstimmmen.

13. Schaltung nach Anspruch 12, **dadurch gekennzeichnet,** daß der Hinlaufschalter ($S_H$) aufweist:
- eine erste Dämptungsdiode (D1), welche parallel zu der Ablenk-Rücklaufkapazität ($C_{RH}$) liegt,
- eine zweite Dämpfungsdiode (D2), welche mit der ersten Dämfungsdiode (D1) und der Modulatorinduktivität ($L_m$) gekoppelt ist und welche parallel zu der Modulator-Rücklaufkapazität ($C_{Rm}$) liegt, und
- ein Schaltelement (Q1) mit einem ersten Strom-Hauptanschluß (Kollektor), der mit der ersten Dämpfungsdiode (D1) und der Ablenkwicklung ($L_H$) gekoppelt ist und mit einem zweiten Strom-Hauptanschluß (Emitter), welcher mit der zweiten Dämpfungsdiode (D2) und der Versorungsspannungsquelle (Masse) gekoppelt ist.

14. Ablenkschaltung mit einer Schaltbetriebs-Seiten-Kissenverzerrungs-Korrekturschaltung, die aufweist:
- eine Zeilen-Ablenkwicklung ($L_H$);
- eine Hinlaufkapazität ($C_t$) zur Bildung einer Zeilen-Hinlaufspannung;
- eine Hinlauf-Schalteinrichtung ($S_H$), welche mit der Zeilen-Ablenkwicklung ($L_H$) und der Hinlaufkapazität ($C_t$) gekoppelt ist und mit einer Zeilenrate betreibbar ist zum Anlegen der Hinlaufspannung an die Zeilen-Ablenwicklung ($L_H$) während eines Zeilen-Hinlaufintervalls, wobei ein Zeilen-Ablenkstrom (scanning current) in der Zeilen-Ablenkwicklung ($L_H$) erzeugt wird;
- eine Ablenk-Rücklaufkapazität ($C_{RH}$), welche mit der Zeilen-Ablenkwicklung ($L_H$) zur Bildung einer Ablenk-Rücklaufresonanzschaltung (40) während eines Zeilen-Rücklaufintervalles gekoppelt ist, womit ein Ablenk-Rucklaufspannungspuls ($V_R$) erzeugt wird;
- eine Modulatorinduktivität ($L_m$), welche mit der Hinlauf-Schalteinrichtung ($S_H$) und der Zeilen-Ablenkwicklung ($L_H$) gekoppelt ist;
- eine Modulator-Rücklaufkapazität ($C_{Rm}$), welche mit der Modulatorinduktivität ($L_M$) zur Bildung einer Modulator-Rücklaufresonanzschaltung (50) während des Zeilen-Rücklaufintervalls gekopppelt ist;
- eine Versorgungsspannungsquelle ($V_0$);
- eine Modulator-Schalteinrichtung ($S_m$), welche mit der Hinlauf-Schalteinrichtung ($S_H$), mit der Quelle ($V_0$) und der Modulatorinduktivität ($L_m$) gekopppelt ist und welche abhängig von Zeilen- ($V_{Hs}$) und Halbbild- (42) Signalraten die Versorgungsspannung ($V_0$) an die Modulatorinduktivität ($L_m$) zu einem variierbaren Zeitpunkt ($t_Z$) innerhalb des Zeilen-Hinlaufintervalles ($t_0$-t4), der in Übereinstimmung mit der Halbbildrate (field rate, 42) varriert, anlegt, wodurch ein Zeilen-Abtaststrom erzeugt wird, der seitenkissenverzerrungskorrigiert ist,

**dadurch gekennzeichnet,** daß die Modulator-Schalteinrichtung ($S_m$) die Versorgungsspannungsquelle ($V_0$) mit der Modulatorinduktivität ($L_m$) koppelt, um einen aufwärts-ansteigenden Modulatorstrom in der Modulatorinduktivität ($L_m$) zu erzeugen, welcher von der Versorgungsspannungsquelle ($V_0$) fließt und der bei einem Strompegel von Null zu dem variablen Zeitpunkt beginnt, um am Ende des Hinlaufintervalles einen Maximalwert zu erreichen, welcher sich in Übereinstimmung mit dem Halbbildraten-Signal (42) verändert.

15. Schaltung nach Anspruch 14, dadurch gekennzeichnet, daß die Modulator-Schalteinrichtung ($S_m$) während der Gesamtheit des Rücklaufintervalles leitet, um den Modulatorstrom während des Endabschnitts des Rücklaufintervalls und während des Anfangsabschnitts des Hinlaufintervalls in die Versorungsspannungsquelle ($V_0$) zurückzuspeisen, bis der Modulatorstrom einen Stromwert von Null zu einem zweiten veränderbaren Zeitpunkt innerhalb des Hinlaufintervalles erreicht, welcher vor dem erstgenannten varrierbaren Zeitpunkt liegt und der in Übereinstimmung mit dem Halbbildraten-Signal (42) variiert.

16. Schaltung nach Anspruch 15, **dadurch gekennzeichnet,** daß die Dauer zwischen den zwei vorgenannten variierbaren Zeitpunkten in Übereinstimmung mit dem Signal für Halbbildraten (42) varriiert.

17. Ablenkschaltung mit einem im Schaltbetrieb arbeitsfähigen Seiten-Kissenverzerrungs-Korrekturschaltkreis, welcher aufweist:
    - eine Zeiten-Ablenkwicklung ($L_H$);
    - eine Hinlaufkapazität ($C_t$) zum Erzeugen einer Zeilen-Hinlaufspannung;
    - eine Hinlaufschalteinrichtung ($S_H$), welche mit der Zeilen-Ablenkwicklung ($L_H$) und der Hinlauf-Kapazität ($C_t$) gekoppelt ist und welche mit einer Zeilenrate betreibbar ist zum Anlegen der Hinlaufspannung an die Zeilen-Ablenkwicklung ($L_H$) während eines Zeilen-Hinlaufintervalles, um einen Zeilen-Abtaststrom (scanning current) in der Zeilen-Ablenkwicklung ($L_H$) zu erzeugen;
    - eine Ablenk-Rücklaufkapazität ($C_{RH}$), welche mit der Zeilen-Ablenkwicklung ($L_H$ ) zum Bilden eines Ablenk-Rücklauf-Resonankreises (40) während eines Zeilen-Rücklaufintervalles gekoppelt ist, um einen Ablenk-Rücklauf-Spannungspuls zu erzeugen;
    - eine Modulatorinduktivität ($L_m$), welche mit der Hinlauf-Schalteinrichtung ($S_H$) und der Zeilen-Ablenkwicklung ($L_H$) gekoppelt ist;
      eine Modulator-Rücklaufkapazität ($C_{Rm}$), welche mit der Modulatorinduktivität ($L_m$) zum Bilden eines Modulator-Rücklauf-Resonanzkreises (50) während des Zeilen-Rücklaufintervalles gekoppelt ist;
    - eine Versorgungsspannungsquelle ($V_0$);
    - eine Modulatorschalteinrichtung ($S_m$), welche mit der Hinlaufschalteinrichtung ($S_H$), der Quelle ($V_0$) und der Modulatorinduktivität ($L_m$) gekoppelt ist und welche abhängig von Zeilenraten- ($V_{Hs}$) und Halbbildraten-(42) Signalen zwischen leitenden und nichtleitenden Zuständen zu einem steuerbaren Zeitpunkt innerhalb des Zeilen-Hinlaufintervalls schalten, welcher in Übereinstimmung mit dem Halbbildraten-Signal (42) variiert, um einen Zeilen-Abststrom, der seiten-kissenverrzerrungskorrigiert ist, zu erzeugen,

    **dadurch gekennzeichnet,**
    daß die Modulatorschalteinrichtung ($S_m$) die Quelle ($V_0$) an die Modulatorinduktivität ($L_m$) koppelt und einen Modulator-Strompfad durch die Modulatorinduktivität ($L_m$) und die Hinlaufschalteinrichtung ($S_H$) für eine variierbare Zeitspanne innerhalb des Zeilen-Hinlaufintervalls - in Übereinstimmung mit dem Halbbildraten-Signal (42) - unterbricht.

18. Ablenkschaltkreis mit einer Schaltbetriebs-Modulatorschaltung, welche aufweist:
    - eine Zeilen-Ablenkwicklung ($L_H$),
    - einen Hinlaufschalter ($S_H$), welcher mit der Zeilen-Ablenkwicklung ($L_H$) zur Erzeugung eines zeilenabtastenden Stromes ($i_H$) in der Zeilen-Ablenkwicklung ($L_H$) gekoppelt ist;
    - eine Ablenk-Rücklaufkapazität ($C_{RH}$), welche mit der Zeilen-Ablenkwicklung ($L_H$) zur Bildung einer Ablenk-Rücklaufresonanzschaltung (40) während eines Zeilen Rücklaufintervalls gekoppelt ist, zur Erzeugung eines Ablenk-Rücklauf-Spannungspules ($V_R$);
    - eine Modulatorinduktivität ($L_m$), welche mit dem Hinlaufschalter ($S_H$) und der Zeilen-Ablenkwicklung ($L_H$) gekoppelt ist;
    - eine Modulator-Rücklaufkapazität ($C_{Rm}$), welche mit der Modulatorinduktivität ($L_m$) zur Bildung eines Modulator-Rucklauf-Resonanzkreises (50) während des Zeilen-Rücklaufintervalles gekoppelt ist;
    - eine DC-Versorgungsspannungsquelle ($V_0$);

    **gekennzeichnet durch**
    einen bidirektional-leitfähigen Modulatorschalter ($S_m$), welcher mit der Quelle ($v_0$) und der Modulatorinduktivität ($L_m$) zur Erzeugung eines bidirektionalen Stromes zwischen Quelle ($V_0$) und der Modulatorinduktivität($L_m$) über den Modulatorschalter ($S_m$) gekoppelt ist, wobei der Modulatorschalter ($S_m$) abhängig von einem Zeilenraten-Signal ($V_H$) und einem Modulator-Steuersignal (42) zwischen leitenden und nichtleitenden Zuständen zu einem steuebaren Zeitpunkt innerhalb des Zeilen-Abtastintervalls schaltet, welcher in Übereinstimmung mit dem Modulator-Steuersignal (42) zum Modulieren des bidirektionalen Stromes in Übereinstimmung mit dem Modulator-Steuersignal variiert.

**Revendications**

1. Circuit de déviation avec un circuit modulateur en mode commuté, comprenant :
   une bobine pour déviation horizontale ($L_H$) ;
   un condensateur de tracé ($C_t$) pour développer une tension de tracé de ligne ;
   un commutateur de tracé ($S_H$) couplé à ladite bobine pour déviation de ligne ($L_H$) et

audit condensateur de tracé ($C_t$) et actionné à une vitesse de ligne pour appliquer ladite tension de tracé à ladite bobine de déviation horizontale ($L_H$) pendant un intervalle de temps de tracé de ligne ($t_0$-$t_4$) pour générer un courant de balayage de ligne ($i_M$) dans ladite bobine de déviation horizontale ($L_H$) ;

un condensateur de retour de déviation ($C_{RH}$) couplé à ladite bobine de déviation horizontale ($L_H$) pour former un circuit résonnant de retour de déviation (40) durant un intervalle de retour de ligne ($t_4$-$t_5$) pour générer une tension à impulsions de retour de déviation (VR) ;

une inductance de modulation ($L_m$) couplée audit commutateur de tracé ($S_H$) et à ladite bobine de déviation horizontale ($L_H$) ;

un condensateur de retour de modulation ($C_{Rm}$) couplé à ladite inductance de modulation ($L_m$) pour former un circuit résonnant de retour de modulation (50) afin de générer un courant de retour de modulation dans ladite inductance de modulation ($L_m$) pendant ledit intervalle de retour de ligne ($t_4$-$t_5$) ;

une source ($V_0$) de tension d'alimentation ; et

un commutateur de modulation ($S_m$) couplé audit commutateur de tracé ($S_H$), à ladite source ($V_0$) et à ladite inductance de modulation ($L_m$) et sensible à un signal d'amplitude de ligne ($V_{HS}$) et à un signal de commande de modulation (42) pour commuter entre l'état conducteur et l'état non conducteur à un instant que l'on peut commander ($t_2$) à l'intérieur d'un intervalle de tracé de ligne qui varie selon ledit signal de commande de modulation (42) afin de générer une tension de modulation à mode commuté qui est directement appliquée à ladite inductance de modulation ($L_m$) pour moduler ledit courant de balayage horizontal ($i_H$) selon ledit signal de commande de modulation (42) ;

caractérisé en ce que ledit commutateur de modulation ($S_m$) couple ladite source ($V_0$) de tension d'alimentation à ladite inductance de modulation ($L_m$) et est conducteur pendant ledit intervalle de retour horizontal pour fournir à travers lui un passage de courant pour ledit courant de retour de modulation.

2. Circuit selon la revendication 1, caractérisé en ce que ladite inductance de modulation ($L_m$) intègre ladite tension de modulation à mode commuté audit courant de modulation.

3. Circuit selon la revendication 1 caractérisé en ce que, pendant ledit intervalle de tracé, ledit commutateur de tracé ($S_H$) en coopération avec ledit commutateur de modulation ($S_m$) développe ladite tension d'alimentation ($V_0$) entre la première borne (23) et la seconde borne (24) de ladite inductance de modulation ($L_m$) quand ledit commutateur de modulation ($S_m$) est dans l'un des deux états conducteurs et maintient les deux bornes (23,24) au même potentiel quand ledit commutateur de modulation ($S_m$) est dans l'autre état conducteur.

4. Circuit selon la revendication 1 caractérisé en ce que ledit commutateur de modulation ($S_m$) conduit le courant de modulation dans ladite inductance de modulation ($L_m$) pendant l'intégralité dudit intervalle de retour et pendant les parties de début et de fin dudit intervalle de tracé et empêche le courant de circuler dans ladite inductance de modulation ($L_m$) pendant ladite période variable à l'intérieur dudit intervalle de tracé.

5. Circuit selon la revendication 4 caractérisé en ce que ledit commutateur de modulation ($S_m$) inclut un premier élément (Q2) qui conduit ledit courant modulateur pendant la partie finale dudit intervalle de tracé et pendant la partie initiale dudit intervalle de retour et inclut un second élément (D3) qui conduit ledit courant de modulation pendant la partie restante dudit intervalle de retour et pendant ladite partie initiale dudit intervalle de tracé.

6. Circuit selon la revendication 4 caractérisé en ce que ledit commutateur de modulation ($S_m$) commute en conduction audit instant que l'on peut commander pour appliquer ladite tension d'alimentation ($V_0$) à ladite inductance de modulation ($L_m$) pour initier une partie de pente croissante dudit courant modulateur ($i_m$)

7. Circuit selon la revendication 4 caractérisé en ce que ledit commutateur de modulation ($S_m$) interrompt pendant ladite période variable un passage de courant pour ledit courant de modulation ($i_m$) fourni par ledit commutateur de tracé ($S_H$) entre ladite source ($V_0$) et ladite inductance de modulation ($L_m$).

8. Circuit selon la revendication 1 caractérisé en ce que ledit commutateur de modulation ($S_m$), quand il est dans l'état conducteur, applique directement ladite tension d'alimentation ($V_0$) à une première borne (23) de ladite inductance de modulation ($L_m$) et, quand il est dans l'état non conducteur , découple ladite inductance de modulation ($L_m$) par rapport à ladite source de tension d'alimentation ($V_0$).

9. Circuit selon la revendication 8 caractérisé en ce que ledit commutateur de tracé ($S_H$) couple directement une seconde borne (24) de ladite inductance de modulation ($L_m$) à ladite source de tension d'alimentation quand ledit conmutateur de tracé est conducteur et dans lequel un courant de résonance issu dudit condensateur du retour de modulation ($C_{Rm}$) circule entre lesdites première (23) et seconde (24) bornes de ladite inductance de modulation ($L_m$) pendant ledit intervalle de retour quand ledit commutateur de tracé ($S_H$) est non conducteur.

10. Circuit selon la revendication 9 caractérisé en ce que, pendant ledit intervalle de tracé, ledit commutateur de tracé ($S_H$) en coopération avec ledit commutateur de modulation ($S_m$) développe ladite tension d'alimentation ($V_0$) entre lesdites première (23) et seconde (24) bornes de ladite inductance de modulation ($L_m$) quand ledit commutateur de modulation ($S_m$) est conducteur et maintient les deux bornes (23, 24) au même potentiel quand ledit commutateur de modulation ($S_m$) est non conducteur.

11. Circuit selon la revendication 1 caractérisé en ce que ledit commutateur de modulation ($S_m$) est conducteur pendant l'intégralité dudit intervalle de retour pour coupler via ledit commutateur de modulation ledit circuit résonant de retour de déviation (40) audit circuit résonant de retour de modulation (50) dans une configuration en pont.

12. Circuit selon la revendication 11 caractérisé en ce que les fréquences de résonance desdits circuits résonants de retour de déviation (40) et de modulation (50) sont sensiblement les mêmes.

13. Circuit selon la revendication 12 caractérisé en ce que ledit commutateur de tracé ($S_H$) comprend une première diode d'amortissement (D1) en parallèle audit condensateur du retour de déviation ($C_{RH}$), une seconde diode d'amortissement (D2) couplée à ladite première diode d'amortissement (D1) et à ladite inductance de modulation ($L_m$) et en paralléle audit condensateur de retour de modulation ($C_{Rm}$), et un élément de commutation (Q1) ayant une première borne de courant principal (collecteur) couplée à ladite première diode d'amortissement (D1) et à ladite bobine de déviation ($L_H$) et ayant une seconde borne de courant principal (émetteur) couplée à ladite seconde diode d'amortissement (D2) et à ladite source de tension d'alimentation (terre).

14. Circuit de déviation avec un circuit de correction de coussin latéral à mode commuté, comprenant :

une bobine de déviation horizontale ($L_H$) ;

un condensateur de tracé ($C_t$) pour développer une tension de tracé de ligne ;

des moyens de commutation de tracé ($S_H$) couplés audit enroulement de déviation horizontale ($L_H$) et audit condensateur de tracé ($C_t$) et actionné à une vitesse de ligne pour appliquer ladite tension de tracé audit enroulement de déviation horizontale ($L_H$) pendant un intervalle de tracé de ligne pour générer un courant de balayage de ligne dans ladite bobine de déviation horizontale ($L_H$) ;

un condensateur de retour de déviation ($CR_H$) couplé audit enroulement de déviation horizontale ($L_H$) pour former un circuit résonant de retour de déviation (40) pendant ledit intervalle de retour horizontal ;

une source ($V_0$) de tension d'alimentation ; et

des moyens de commutation de modulateur ($S_m$) couplés auxdits moyens de commutation de tracé ($S_H$) , à ladite source ($V_0$) et à ladite inductance de modulation ($L_m$) et sensibles aux signaux d'amplitude de ligne ($V_{Hs}$) et de champ (42) pour appliquer ladite tension d'alimentation ($V_0$) à ladite inductance de modulateur ($L_m$) à un instant variable ($t_2$) dans ledit intervalle de tracé horizontal ($t_0$- $T_4$) qui varie selon ledit signal d'amplitude de champ (42) pour fournir un courant de balayage horizontal à correction de coussin latéral, caractérisé en ce que lesdits moyens de commutation de modulateur ($S_m$) couplent ladite source ($V_0$) de tension d'alimentation à ladite inductance de modulation ($L_m$), pour générer un courant de modulation à rampe croissante dans ladite inductance de modulation ($L_m$) qui circule de ladite source ($V_0$) de tension d'alimentation et qui démarre à un niveau de courant nul audit instant variable pour atteindre à la fin dudit intervalle de tracé une amplitude maximale qui change selon ledit signal d'amplitude de champ (42).

15. Circuit selon la revendication 14 caractérisé en ce que lesdits moyens de commutation du modulateur ($S_m$) sont conducteurs pendant l'intégralité dudit intervalle de retour pour ramener ledit courant de modulation à ladite source ($V_0$) de tension d'alimentation pendant la partie finale dudit intervalle de retour et pendant la partie initiale dudit intervalle de tracé jusqu'à ce que ledit courant de modulation atteigne un niveau de courant nul à un second instant variable à l'intérieur dudit intervalle de tracé

qui est antérieur au premier instant variable cité et qui varie selon ledit signal d'amplitude de champ (42).

16. Circuit selon la revendication 15 caractérisé en ce que la durée entre les deux instants susdits varient également selon ledit signal d'amplitude de champ (42).

17. Circuit de déviation avec un circuit de correction de coussin latéral en mode commuté, comprenant :

une bobine de déviation horizontale ($L_H$) ;

un condensateur de tracé ($C_t$) pour développer une tension de tracé horizontal ;

des moyens de commutation de tracé ($S_H$) couplés à ladite bobine de déviation horizontale ($L_H$) et audit condensateur de tracé ($C_t$) et fonctionnant à une amplitude de ligne pour appliquer ladite tension de tracé à ladite bobine de déviation horizontale ($L_H$) pendant un intervalle de tracé de ligne pour générer un courant de balayage de ligne dans ladite bobine de déviation horizontale ($L_H$) ;

un condenstateur de retour de déviation ($CR_H$) couplé à ladite bobine de déviation horizontale ($L_H$) pour former un circuit résonnant de retour de déviation (40) pendant un intervalle de retour horizontal pour générer une tension à impulsions de retour de déviation ;

une inductance de modulation ($L_m$) couplée auxdits moyens de commutation de tracé ($S_H$) et à ladite bobine de déviation horizontale ($L_H$) ;

un condensateur de retour de modulation ($C_{Rm}$) couplé à ladite inductance de modulation ($L_m$) pour former un circuit résonnant de retour de modulation (50) pendant ledit intervalle de retour horizontal ;

une source ($V_0$) de tension d'alimentation ; et

des moyens de commutation du modulateur ($S_m$) couplés auxdits moyens de commutation de tracé ($S_H$) , à ladite source ($V_0$) et à ladite inductance de modulation ($L_m$), et, sensibles aux signaux d'amplitude de ligne ($V_{HS}$) et de champ (42) pour commutation entre les états conducteur et non conducteur à un instant que l'on peut commander à l'intérieur de l'intervalle de tracé horizontal qui varie selon ledit signal d'amplitude de champ (42) pour fournir un courant de balayage de ligne avec correction de coussin latéral, caractérisé en ce que lesdits moyens de commutation du modulateur ($S_m$) couplent ladite source ($V_0$) à ladite inductance de modulation ($L_m$), et interrompent un parcours du courant de modulation à travers ladite inductance de modulation ($L_m$) et lesdits moyens de commutation de tracé horizontal ($S_H$) pendant une période variable à l'intérieur dudit intervalle de tracé horizontal selon ledit signal d'amplitude de champ (42).

18. Circuit de déviation avec un circuit de modulation à mode commuté, comprenant :

une bobine de déviation horizontale ($L_H$) ;

un commutateur de tracé ($S_H$) couplé à ladite bobine de déviation horizontale ($L_H$) pour générer un courant de balayage de ligne (iH) dans ladite bobine de déviation horizontale ($L_H$) ;

un condensateur de retour de déviation ($CR_H$) couplé à ladite bobine de déviation horizontale ($L_H$) pour former un circuit résonnant de retour de déviation (40) pendant un intervalle de retour de ligne pour générer une tension à impulsions de retour de déviation (VR) ;

une inductance de modulation ($L_m$) couplée audit commutateur de tracé ($S_H$) et à ladite bobine de déviation horizontale ($L_H$) ;

un condensateur de retour de modulation ($C_{Rm}$) couplé à ladite inductance de modulation ($L_m$) pour former un circuit résonnant de retour de modulation (50) pendant ledit intervalle de retour de ligne ; et

une source ($V_0$) de tension DC d'alimentation ;

caractérisé par

un commutateur de modulation conducteur de façon bidirectionnelle ($S_m$) couplé à ladite source ($V_0$) et à ladite inductance de modulation ($L_m$) pour générer un courant bidirectionnel entre ladite source ($V_0$) et ladite inductance de modulation ($L_m$) via ledit commutateur de modulation ($S_m$), ledit commutateur de modulation ($S_m$) étant sensible à un signal d'amplitude de ligne ($V_{Hs}$) et à un signal de commande de modulation (42) pour commuter entre les états conducteur et non conducteur à un instant que l'on peut contrôler à l'intérieur dudit intervalle de balayage de ligne qui varie selon ledit signal de commande de modulation (42) pour moduler ledit courant bidirectionnel selon ledit signal de commande de modulation.