METHOD FOR FORMING STRUCTURES IN FINFET DEVICES

FIELD OF THE INVENTION

The present invention relates generally to semiconductor manufacturing and, more particularly, to forming FinFET devices.

BACKGROUND OF THE INVENTION

The escalating demands for high density and performance associated with ultra large scale integration semiconductor devices require design features, such as gate lengths, below 100 nanometers (nm), high reliability and increased manufacturing throughput. The reduction of design features below 100 nm challenges the limitations of conventional methodology.

For example, when the gate length of conventional planar metal oxide semiconductor field effect transistors (MOSFETs) is scaled below 100 nm, problems associated with short channel effects, such as excessive leakage between the source and drain, become increasingly difficult to overcome. In addition, mobility degradation and a number of process issues also make it difficult to scale conventional MOSFETs to include increasingly smaller device features. New device structures are therefore being explored to improve FET performance and allow further device scaling.

Double-gate MOSFETs represent new structures that have been considered as candidates for succeeding existing planar MOSFETs. In double-gate MOSFETs, two gates may be used to control short channel effects. A FinFET is a double-gate structure that exhibits good short channel behavior. A FinFET includes a channel formed in a vertical fin. The FinFET structure may also be fabricated using layout and process techniques similar to those used for conventional planar MOSFETs.

SUMMARY OF THE INVENTION

Implementations consistent with the principles of the invention provide single-crystal silicon fin structures formed on opposite sides of a dielectric fin structure. The material for the dielectric fin structure is chosen such that a significant stress is induced in the single-crystal silicon material. Accordingly, enhanced mobility can be achieved.

In accordance with the purpose of this invention as embodied and broadly described herein, a semiconductor device includes a first fin structure that comprises a dielectric material and includes a first side surface and a second side surface; a second fin structure that comprises a single-crystal silicon material and is formed adjacent to the first side surface of the first fin structure; a third fin structure that comprises the single-crystal silicon material and is formed adjacent to the second side surface of the first fin structure; a source region that is formed at one end of the first fin structure, the second fin structure, and the third fin structure; a drain region that is formed at an opposite end of the first fin structure, the second fin structure, and the third fin structure; and at least one gate.

In another implementation consistent with the present invention, a method of manufacturing a semiconductor device that includes a substrate and a dielectric layer formed on the substrate is disclosed. The method includes etching the dielectric layer to form a first fin structure; depositing an amorphous silicon layer; etching the amorphous silicon layer to form a second fin structure adjacent a first side surface of the first fin structure and a third fin structure adjacent a second, opposite side surface of the first fin structure; depositing a

metal layer on at least upper surfaces of the second fin structure and the third fin structure; performing a metal-induced crystallization operation to convert the amorphous silicon in the second and third fin structures to a single-crystal silicon material; forming a source region and a drain region; depositing a gate material over the first, second, and third fin structures; and patterning and etching the gate material to form at least one gate electrode.

In yet another implementation consistent with the principles of the invention, a semiconductor device that includes a first fin structure, a second fin structure, and a third fin structure is disclosed. The first and second fin structures include a single-crystal silicon material. The third fin structure is located between the first fin structure and the second fin structure and includes a dielectric material. The third fin structure causes stress to be induced in the single-crystal silicon material of the first fin structure and the second fin structure.

BRIEF DESCRIPTION OF THE DRAWINGS

The accompanying drawings, which are incorporated in and constitute a part of this specification, illustrate an embodiment of the invention and, together with the description, explain the invention. In the drawings,

Fig. 1 illustrates an exemplary process for forming fin structures for a FinFET device in an implementation consistent with the principles of the invention;

Figs. 2-9 illustrate exemplary views of a FinFET device fabricated according to the processing described in Fig. 1;

Figs. 10-15 illustrate exemplary views for forming multiple fin structures in an alternative implementation consistent with the principles of the invention; and

Figs. 16 and 17 illustrate exemplary views for creating a trench according to an alternative implementation consistent with the principles of the invention.

DETAILED DESCRIPTION

The following detailed description of implementations consistent with the present invention refers to the accompanying drawings. The same reference numbers in different drawings may identify the same or similar elements. Also, the following detailed description does not limit the invention. Instead, the scope of the invention is defined by the appended claims and their equivalents.

Implementations consistent with the principles of the invention provide single-crystal silicon fin structures that are formed on opposite sides of a dielectric fin structure. The material for the dielectric fin structure is chosen such that a significant stress is induced in the single-crystal silicon material to enhance mobility.

EXEMPLARY PROCESSING

Fig. 1 illustrates an exemplary process for forming fin structures for a FinFET device in an implementation consistent with the principles of the invention. Figs. 2-9 illustrate exemplary views of a FinFET device fabricated according to the processing described in Fig. 1. The fabrication of one FinFET device will be described hereinafter. It will be appreciated, however, that the techniques described herein are equally applicable to forming more than one FinFET device.

With reference to Figs. 1 and 2, processing may begin by forming a dielectric fin structure 210 on a substrate 200 of a semiconductor device (act 105). In one implementation, substrate 200 may comprise silicon. In alternative implementations consistent with the present invention, substrate 200 may comprise other semiconducting materials, such as germanium, or combinations of semiconducting materials, such as silicon-germanium. In another alternative, substrate 200 may include an insulator, such as an oxide layer, formed on a silicon or germanium substrate. Dielectric fin structure 210 may comprise a dielectric material that causes significant tensile stress (strain) in the dual fin structures that will be formed adjacent dielectric fin structure 210. In one implementation, dielectric fin structure 210 may comprise an oxide or a nitride.

Dielectric fin structure 210 may be formed in a conventional manner. For example, a dielectric material may be deposited over substrate 200 to a thickness ranging from about 200 Å to about 1000 Å. A mask may be formed over a portion of the dielectric material and the dielectric material may then be etched in a conventional manner, with the etching terminating on substrate 200 to form dielectric fin structure 210. The resulting dielectric fin structure 210 may have a width ranging from about 100 Å to about 1000 Å.

After forming dielectric fin structure 210, an amorphous silicon layer 310 may be deposited on the semiconductor device, as illustrated in Fig. 3 (act 110). In one implementation consistent with the principles of the invention, amorphous silicon layer 310 may be deposited to a thickness ranging from about 100 Å to about 1000 Å.

Amorphous silicon layer 310 may then be etched in a conventional manner, with the etching terminating at substrate 200 to form amorphous silicon spacer (fin) structures 410, as illustrated in Fig. 4 (act 115). Each amorphous silicon fin structure 410 may have a height ranging from about 200 Å to about 1000 Å and a width ranging from about 100 Å to about 1000 Å.

A dielectric layer 510 may be deposited on the semiconductor device, as illustrated in Fig. 5 (act 120). In one implementation consistent with the principles of the invention, dielectric layer 510 may be deposited to a thickness ranging from about 200 Å to about 1000 Å. Dielectric layer 510 may comprise an oxide or other dielectric materials.

The semiconductor device may be polished via a chemical-mechanical polishing (CMP) (or other technique) to planarize the top surface of the semiconductor device such that the top surface of each of amorphous silicon fin structures 410 is exposed, as illustrated in Fig. 6 (act 120). During the CMP, a portion of the upper surface of dielectric fin structure 210 and amorphous silicon fin structures 410 may be removed so that the upper surface of each of amorphous silicon fin structures 410 is exposed. For example, after the CMP, the height of fins 210 and 410 may range from abou5 150 Å to about 200 Å.

A metal layer 710, such as nickel, may be deposited on the semiconductor device, as illustrated in Fig. 7 (act 125). In one implementation, nickel layer 710 may be deposited to a thickness of about 20 Å.

A metal-induced crystallization (MIC) operation may then be performed. The MIC operation may involve annealing nickel layer 710 at about 500 °C to about 550 °C for several hours, which acts to diffuse the nickel into the amorphous silicon to convert the amorphous silicon in fin structures 410 to single-crystal silicon 810, as illustrated in Fig. 8 (act 130). As a result of the MIC operation, a thin layer of a nickel silicon (NiSi) compound 820 may formed between substrate 200 and single-crystal silicon fin structures 810. In one implementation, the thickness of NiSi layer 820 may range from about 20 Å to about 200 Å.

After single-crystal silicon fin structures 810 are formed, conventional FinFET fabrication processing can be utilized to complete the transistor (e.g., forming the source and drain regions), contacts, interconnects and inter-level dielectrics for the FinFET device. For example, dielectric layer 510 may be removed, a protective dielectric layer, such as a silicon nitride or silicon oxide may be formed on the top surface of fins 210 and 810, followed by the formation of a gate dielectric on the side surfaces of single-crystal silicon fin structures 810. Source/drain regions may then be formed at the respective ends of fins 210 and 810, followed by formation of one or more gates. For example, a silicon layer, germanium layer, combinations of silicon and germanium or various metals may be used as the gate material. The gate material may then be patterned and etched to form the gate electrodes. For example, Fig. 9 illustrates an exemplary top view of the semiconductor device consistent with the principles of the invention after the source/drain regions and gate electrodes are formed. As illustrated, the semiconductor device includes a double-gate structure with fins 210 and 810, source and drain regions 910 and 920, and gate electrodes 930 and 940.

Source/drain regions 910 and 920 may then be doped with n-type or p-type impurities based on the particular end device requirements. In addition, sidewall spacers may optionally be formed prior to the source/drain ion implantation to control the location of the source/drain junctions based on the particular circuit requirements. Activation annealing may then be performed to activate source/drain regions 910 and 920.

The present invention has been described above as forming a number of fin structures. It should be understood that methods consistent with the present invention may be used to form any number of fins, based on the particular circuit requirements.

Thus, in accordance with the principles of the invention, single-crystal silicon fin structures may be formed, having a dielectric fin structure located between the single-crystal silicon fin structures. The material for the dielectric fin structure may be chosen so as to induce a significant stress (strain) in the single-crystal silicon fin structures. As a result, enhanced mobility in the single-crystal silicon fin structures is achieved.

OTHER IMPLEMENTATIONS

Figs. 10-15 illustrate exemplary views for forming multiple fin structures in an alternative implementation consistent with the principles of the invention. With reference to Fig. 10, processing may begin with a semiconductor device that includes an oxide layer 1010 formed on a substrate 1000. Substrate 1000 may comprise silicon or other semiconducting materials, such as germanium, or combinations of semiconducting materials, such as silicon-germanium. Oxide layer 1010 may have a height ranging from about 200 Å to about 1000 Å.

Oxide layer 1010 may be etched to form a trench 1020, as illustrated in Fig. 10. In one implementation, trench 1020 may have a width ranging from about 200 Å to about 2000 Å. Next, amorphous silicon may be deposited and etched to form amorphous silicon spacers 1110, as illustrated in Fig. 11. Each of amorphous silicon spacers 1110 may have a width ranging from about 100 Å to about 1000 Å. A dielectric material 1210 may be deposited in the gap between amorphous silicon spacers 1110, as illustrated in Fig. 12. The dielectric material may comprise an oxide or other dielectric materials.

A layer of nickel 1310 may deposited on a top surface of amorphous silicon spacers 1110, as illustrated in Fig. 13. The thickness of nickel layer 1310 may be about 20 Å. A MIC operation may then be

performed. The MIC operation may involve annealing nickel layer 1310 at about 500 °C to about 550 °C for several hours to convert amorphous silicon spacers 1110 to single-crystal silicon fin structures 1410, as illustrated in Fig. 14. As a result of the MIC operation, a thin layer of a nickel silicon (NiSi) compound 1420 may be formed between substrate 1000 and single-crystal silicon fin structures 1410. In one implementation, the thickness of NiSi layer 1420 may range from about 20 Å to about 200 Å.

Oxide layer 1010 may then be removed in a conventional manner, as illustrated in Fig. 15. Accordingly, a spacer-induced merged FET can be produced.

In another implementation, spacers may be used to create a narrow trench that can provide a coupling effect between both sides of the trench. As illustrated in Fig. 16, a semiconductor device may include an oxide layer 1610 formed on a substrate (not shown) with a silicon layer 1620 formed thereon. A material, such as a silicon nitride or a silicon oxide, may be deposited and patterned to form hard masks 1640. Next, a spacer material, such as SiN, SiO, or some other material, may be deposited and etched to form spacers 1630 on the side surfaces of hard masks 1640. Silicon layer 1620 may then be etched using spacers 1630 and hard masks 1640 as masks to form a narrow trench 1710, as illustrated in Fig. 17. Trench 1710 may have a width ranging from about 100 Å to about 1000 Å. Trench 1710 advantageously provides a coupling effect between fins 1620 located on both sides of trench 1710.

CONCLUSION

Implementations consistent with the principles of the invention provide single-crystal silicon fin structures that are formed on opposite sides of a dielectric fin structure. The material for the dielectric fin structure is chosen such that a significant stress is induced in the single-crystal silicon material. In this manner, enhanced mobility can be achieved.

The foregoing description of exemplary embodiments of the present invention provides illustration and description, but is not intended to be exhaustive or to limit the invention to the precise form disclosed. Modifications and variations are possible in light of the above teachings or may be acquired from practice of the invention. For example, in the above descriptions, numerous specific details are set forth, such as specific materials, structures, chemicals, processes, etc., in order to provide a thorough understanding of the present invention. However, the present invention can be practiced without resorting to the details specifically set forth herein. In other instances, well known processing structures have not been described in detail, in order not to unnecessarily obscure the thrust of the present invention. In practicing the present invention, conventional deposition, photolithographic and etching techniques may be employed, and hence, the details of such techniques have not been set forth herein in detail.

While a series of acts has been described with regard to Fig. 1, the order of the acts may be varied in other implementations consistent with the present invention. Moreover, non-dependent acts may be implemented in parallel.

No element, act, or instruction used in the description of the present application should be construed as critical or essential to the invention unless explicitly described as such. Also, as used herein, the article "a" is intended to include one or more items. Where only one item is intended, the term "one" or similar language is used.

The scope of the invention is defined by the claims and their equivalents.

WHAT IS CLAIMED IS:

1. A semiconductor device, comprising:

a first fin structure (210) comprising a dielectric material and including a first side surface and a second side surface;

a second fin structure (810) comprising a single-crystal silicon material and being formed adjacent to the first side surface of the first fin structure (210);

a third fin structure (810) comprising the single-crystal silicon material and being formed adjacent to the second side surface of the first fin structure (210);

a source region (910) formed at one end of the first fin structure (210), the second fin structure (810), and the third fin structure (810);

a drain region (920) formed at an opposite end of the first fin structure (210), the second fin structure (810), and the third fin structure (810); and

at least one gate (930, 940).

2. The semiconductor device of claim 1 wherein a width of the first fin structure (210) ranges from about 200 Å to about 1000 Å.

3. The semiconductor device of claim 1 wherein the dielectric material includes one of an oxide and a nitride.

4. The semiconductor device of claim 1 wherein a width of each of the second fin structure (810) and the third fin structure (810) ranges from about 100 Å to about 1000 Å.

5. A method of manufacturing a semiconductor device that includes a substrate (200) and a dielectric layer (210) formed on the substrate (200), the method characterizing:

etching the dielectric layer (210) to form a first fin structure (210);

depositing an amorphous silicon layer (310);

etching the amorphous silicon layer (310) to form a second fin structure (410) adjacent a first side surface of the first fin structure (210) and a third fin structure (410) adjacent a second, opposite side surface of the first fin structure (210);

depositing a metal layer (710) on at least upper surfaces of the second fin structure (410) and the third fin structure (410);

performing a metal-induced crystallization operation to convert the amorphous silicon in the second and third fin structures (410) to a single-crystal silicon material;

forming a source region (910) and a drain region (920);

depositing a gate material over the first, second, and third fin structures (210, 810); and

patterning and etching the gate material to form at least one gate electrode (930, 940).

6. The method of claim 5 wherein the dielectric layer (210) comprises at least one of an oxide and a nitride.

7. A semiconductor device comprising:

a first fin structure (810) comprising a single-crystal silicon material;

a second fin structure (810) comprising the single-crystal silicon material; and

a third fin structure (210) located between the first fin structure (810) and the second fin structure (810) and comprising a dielectric material, the third fin structure (210) causing stress to be induced in the single-crystal silicon material of the first fin structure (810) and the second fin structure (810).

8. The semiconductor device of claim 7 wherein a width of each of the first fin structure (810) and the second fin structure (810) ranges from about 100 Å to about 1000 Å.

9. The semiconductor device of claim 8 wherein a width of the third fin structure (210) ranges from about 100 Å to about 1000 Å.

10. The semiconductor device of claim 9 wherein the dielectric material comprises at least one of an oxide and a nitride.