

Single-VCO CDR for TMDS Data at Gigabit Rate

Abstract

[0065] A clock and data recovery circuit has a voltage controlled oscillator that provides a clocking signal synchronized to a received serialized data. A multiple phase generator converts the clocking signal to a plurality of multiple phased clocking signals. A data capture device acquires the serialized data with each of the plurality of multiple phased clocking signals to create multiple phased data signals. A phase detector determines if the clocking signal is in phase with the recovered serialized data and providing a lead signal and a lag signal indicating whether the clocking signal is in phase with the recovered serialized data. A frequency initializing device assists acquisition of lock of the voltage controlled oscillator to a reference clock signal. A recovered data selector selects which of the multiple phased data signals are to be transferred to external circuitry for further processing.

Figure 3 is suggested for publication.