# AN IMD SCHEME BY POST-PLASMA TREATMENT OF FSG AND TEOS OXIDE CAPPING LAYER

## ABSTRACT

A method of forming a metal interconnect within a fluorinated silica glass dielectric layer while preventing outgassing from the FSG dielectric layer, comprising the following steps. A semiconductor structure having a metal structure, with an overlying liner layer, formed thereover is provided. A FSG dielectric layer is formed over the liner layer. The FSG dielectric layer having an exposed upper surface. The FSG dielectric layer is treated with a first nitrogen gas/plasma treatment to form a fluorine depleted upper capping layer from the exposed surface of the FSG dielectric layer. A TEOS oxide layer is formed over the upper capping layer. The TEOS oxide layer is planarized to form a planarized TEOS oxide layer. The planarized TEOS oxide layer, the upper capping layer, the treated FSG dielectric layer, and the liner layer are patterned to form a via hole therethrough, exposing a portion of the metal structure and exposing sidewalls of the patterned treated FSG dielectric layer within the via opening. At least the exposed sidewalls of the patterned treated fluorinated silicon glass dielectric layer within the via opening is treated with a second nitrogen gas/plasma treatment to form a fluorine depleted sidewall capping layer from the exposed sidewalls of the patterned treated fluorinated silicon glass dielectric layer, wherein the upper and sidewall capping layers prevent the outgassing from the patterned FSG dielectric layer. A metal interconnect is formed within the via opening.

Fig. 8