The inter-module insulating layer 304 may be formed of silicon-containing dielectric material such as silicon oxide, silicon nitride, or silicon oxynitride.

[0028] In one example, the first region R1 is a high voltage region and the second region R2 is a low voltage region. In another example, the first region R1 is p-type MOSFET (p-MOSFET) region and the second region R2 is an n-type MOSFET (n-MOSFET) region. Each of the GAA FET module TR1 and TR2 may include a channel region CH and source/drain regions SD that are separated by the channel region CH in the *X*-direction. The source/drain regions SD may be wider in the *Y*-direction than the channel region CH.

[0029] Referring to Figures 3A, 3B, and 3C, the source/drain regions SD may include first semiconductor layers 306 and second semiconductor layers 308 that alternately and repeatedly stacked on the substrate 302. The first semiconductor layer 306 is formed of a first material having etch selectivity to a second material of which the second semiconductor layer 308 is formed (*i.e.*, an etch rate of the first material is higher than an etch rate of the second material). The etch selectivity (*i.e.*, a ratio of the etch rate of the first material to the etch rate of the second material) is between about 10:1 to 200:1. Example combinations of the first material and the second material include silicon germanium (SiGe)/silicon (Si), silicon germanium (SiGe)/germanium (Ge), and germanium tin (GeSn)/silicon (Si). Portions of the first semiconductor layers 306 in the source/drain regions SD may be separated in the *X*-direction by gate electrodes GE, each of which is surrounded by a gate stack 310, formed in the channel region CH. The second semiconductor layer 308 in the channel region CH may serve as nanowires or nanotubes having a width of between several nanometers and several tens of nanometers.

[0030] The first and second semiconductor layers 306 and 308 may be formed using any suitable deposition technique, such as chemical vapor deposition (CVD), atomic layer deposition (ALD), or physical vapor deposition (PVD), and patterning technique, such as a lithography and etch process.

[0031] The first and second semiconductor layer 306 and 308 may each have thickness of between about 6 nm and about 14 nm, for example, about 10 nm.

[0032] Referring to Figure 3D, the gate stack 310 includes an interfacial layer 312, a high-κ gate dielectric layer 314, a first high-κ dielectric cap layer 316, a p-type work