

## DOPING PROFILE IMPROVEMENT OF IN-SITU DOPED N-TYPE EMITTERS

The present invention relates generally to bipolar processing, and more specifically relates to a process for making the leading slope of the doping profile of an n-type in-situ doped epitaxial Si (epi) layer more steep by co-doping the epi layer with germanium (Ge) for the first few seconds of the deposition.

In common bipolar processing, the emitter-base junction of a transistor is typically formed by going through the following steps shown in Figure 1. First, at step A, boron (B) 10 is implanted in a single-crystalline silicon substrate 12. Subsequently, as shown in step B, a polysilicon (poly) layer 14 is deposited on top of the substrate 12, and is separated from the substrate 12 by a very thin layer of silicon dioxide 16. The polysilicon layer 14 needs to be n-type doped by either in-situ doping or by first growing undoped poly, which is later implanted with arsenic (As), phosphorus (P) or antimony (Sb). As is more common than P, and Sb is rarely used. Ultimately, as shown in step C, an emitter-base junction 18 is formed during a high temperature treatment. The high temperature causes the B and the As (or P/Sb) to diffuse. The junction 18 is established where the B and As diffusion fronts meet. The high temperature may cause the interfacial oxide layer 16 to break up, resulting in some recrystallization of the polysilicon layer 14.

In Figure 2, the doping profiles are depicted: (1) as implanted (solid lines); and (2) after the high-temperature treatment that establishes the emitter-base junction (dashed lines). The As profile 20 is shown on the left side and the B profile 22 is shown on the right, with the y-axis representing the concentration and the x-axis represents depth. Due to the fact that the diffusion constant in polysilicon is several orders of magnitude higher than in single-crystalline silicon, the implanted Gaussian profile has a strong tendency to become flat when exposed to temperatures that are sufficiently high to drive the As across

the interfacial oxide layer into the substrate. Thus, the As distribution 24 in the polysilicon becomes almost flat after exposure to a moderate temperature budget.

The interfacial oxide 16 between poly- and mono-silicon decreases the base current of the transistor and gives rise to a high current amplification factor. It also contributes to the series resistance in the emitter, as do the grain boundaries in the polysilicon layer 12.

In recent developments, the B base implantation has been replaced by an in-situ B-doped epitaxial layer to better control the doping profiles. True block-shaped doping profiles are possible with abrupt transitions in dope concentration. This technology, based on low-temperature epitaxy rather than on implantations to determine the doping profiles, is used for instance in SiGe HBTs (Heterojunction Bipolar Transistors), not only to determine the B profile, but also to determine the Ge and, if applicable, the C profile. The steeper dopant transitions and thinner layers, together with SiGe band-gap engineering, give rise to exceptionally high operating frequencies for these transistors.

Due to the decreasing dimensions, it is getting increasingly difficult to evenly implant the poly-emitter in these transistors and in-situ doped poly is the mainstay. As the emitter resistance becomes a limiting factor in high-frequency operations, it is very advantageous to lower this resistance. This can be done by growing an epitaxial (epi) layer rather than a polysilicon layer. The specific resistance of an epi layer is lower than the specific resistance of a polysilicon layer, due to the lack of grain boundaries in epi. Also, by definition, there is no interfacial oxide layer adding to the resistance when the top layer is grown epitaxially.

Figure 3 depicts the process steps for growing an emitter epitaxially. Step A depicts the result of growing a B-doped base epi layer 26 (in a HBT, the SiGe and C-doped SiGe layers will also be grown epitaxially, which is not shown). Step B depicts the process after growing the As-doped top layer epitaxially (i.e., the mono-emitter layer) 28.

Note that there is no interfacial oxide layer. Step C depicts the process after a high temperature treatment has been applied, and the emitter base junction 30 is established.

Although the processing steps between poly- and mono-emitter seem similar, there are considerable differences. These differences are evident in Figure 4, which shows the doping profiles of the deposited base and mono-emitter layers. Similar to Figure 2, Figure 4 shows the doping profiles as grown (solid lines) and after the high-temperature treatment (dashed lines). Again, the As profile 32 is shown on the left, while the B profile 34 is shown on the right. Note the block-shaped doping profiles obtained by low-temperature epitaxy. When comparing Figure 4, to Figure 2, it can be seen that steeper doping profiles are achieved. Steeper profiles allow the vertical dimensions of the transistor to shrink, enhancing its high frequency performance.

Unfortunately, in reality the As doping profile is not as ideal as is suggested in the plot of Figure 4. Compared to other dopants used in low-temperature epitaxy (e.g., B, Ge, C), which can be grown block-shaped with a steepness of the slopes exceeding the resolution capability of SIMS (Secondary Ion Mass Spectroscopy, an analyzing method for these layers), the steepness of the slope of an As profile is not so good. Upon turning on the AsH<sub>3</sub> gas flow, the As concentration has the tendency to rise very slowly until it reaches its equilibrium value. See, e.g., W.B. de Boer, F. Roozeboom "Advances in Rapid Thermal and Integrated Processing," published by Kluwer Academic Publishers, 101 Philip Drive, Norwell, MA 02601, ISBN 0-7923-4011-6, p. 443-463 (1995). The problem is so bad that it is very difficult to control the As doping level in thin epitaxially grown layers. See, e.g., US Patent 6,579,752, entitled "Phosphorus Dopant Control in Low Temperature Si and SiGe Epitaxy," issued to De Boer on June 17, 2003, which is hereby incorporated by reference. Although a mono-emitter may not be very critical in terms of thickness or doping level, the sloped profile at the onset of the growth of the emitter layer

is undesirable. Namely, steep slopes enable a decrease in the vertical dimensions of the transistor, enhancing its speed. This benefit is lost when the slopes get less steep.

Fig. 5 is a SIMS (Secondary Ion Mass Spectroscopy) plot of an As-doped mono-emitter layer, clearly showing the low rate at which the As concentration rises after the  $\text{AsH}_3$  flow has been turned on. The long slope before the concentration hits its equilibrium level is typical for n-type dopants in low-temperature epitaxy. The slope of approximately 23 nm/dec is much weaker than 4-6 nm/dec, which is common for true block-shaped profiles when the SIMS resolution determines the slope. A slope of 23 nm/dec is real and is not SIMS determined.

(Note that when the SIMS profile is plotted on a log-scale, the slope of a line on this scale is often expressed in nm/dec, i.e., how many nm on the horizontal scale are needed for the concentration to increase by a factor of 10. A smaller number indicates a steeper slope.)

A known way to improve the steepness of the slope is to expose the surface upon which the epi layer is to be grown to a certain  $\text{AsH}_3$  concentration before starting to grow. See, e.g., W.D. van Noort et al, "Advances in Rapid Thermal Processing," The Electrochemical Society Proceedings, Volume 99-10, ISBN 1-56677-232-X, p. 335-342 (1999). However, at these high As concentrations, there is a risk that the equilibrium concentration will be exceeded, which may lead to crystallographic defects in the epitaxial layer that is to follow. Defects in general are undesirable, even more so because they originate on an interface that is very sensitive and which can have a large influence on the transistor behavior, as is known from the poly emitter. It is also not sure how effective this method (i.e., exposing the surface to an As concentration prior to growing) is at the high concentrations that are needed for the mono emitter.

The present invention provides a method to improve the steepness of the slope of an n-type doping profile when growing a mono-emitter. During the first few seconds of

the growth, a germanium (Ge) source (e.g.,  $\text{GeH}_4$ ) is added to the gas flow. The remainder of the mono-emitter layer is deposited as usual, with just a Si source (e.g.,  $\text{SiH}_4$ ) and an n-type dopant source (e.g.,  $\text{AsH}_3$ ) added to a main flow of  $\text{H}_2$ . Using this technique, the n-type dopant reaches its equilibrium concentration almost immediately.

In a first aspect, the invention provides a method for forming an emitter-base junction, comprising: providing a base epitaxial layer; and growing a doped mono-emitter layer on the base epitaxial layer using a gas flow comprised of a set of process gases, wherein gas flow includes an addition of a Ge source to the process gases for a first few seconds of the gas flow.

In a second aspect, the invention provides a method of processing a wafer, comprising the steps of: placing the wafer into a reactor chamber; maintaining an elevated temperature within the reactor chamber prior to processing; passing hydrogen through the reactor chamber; turning on a set of process gases, wherein the process gases include a Ge source; turning off the Ge source within a first few seconds; and turning off the remaining process gases at a substantially later time.

In a third aspect, the invention provides a method for processing a semiconductor, comprising: growing a doped mono-emitter layer on a base layer using a gas flow comprised of a set of process gases, wherein gas flow includes an addition of a Ge source to the process gases for a first few seconds of the gas flow.

These and other features of this invention will be more readily understood from the following detailed description of the various aspects of the invention taken in conjunction with the accompanying drawings in which:

Figure 1 depicts the steps of forming an emitter-base junction using a polysilicon layer.

Figure 2 depicts the doping profiles, as implanted and after the high-temperature treatment, for establishing the emitter-base junction.

Figure 3 depicts the steps of an alternative method of forming an emitter-base junction using an epitaxial layer rather than a polysilicon layer.

Figure 4 depicts the doping profiles, as implanted and after the high-temperature treatment, for establishing the emitter-base junction using an epitaxial layer.

Figure 5 depicts a SIMS plot of an As-doped mono-emitter layer.

Figure 6 depicts a SIMS plot of an As-doped mono-emitter layer with a Ge spike at the interface, in accordance with the present invention.

Figure 7 depicts a second SIMS plot of an As-doped mono-emitter layer with a Ge spike at the interface, in accordance with the present invention.

Figure 8 depicts a flow diagram showing a method of implementing an embodiment of the invention.

An illustrative embodiment of invention is described that provides a method for growing emitter-base junctions using an epitaxial layer, which includes the step of adding a germanium (Ge) source (e.g.,  $\text{GeH}_4$ ) to the gas flow for a few seconds at the onset of the growth of an As-doped epitaxial layer. This not only creates a Ge spike at the interface of the B-doped substrate and the As-doped epitaxial emitter layer, but also improves the slope of the As profile. The incorporation of As in SiGe is distinct from the incorporation of As in Si in that a very thin SiGe layer suffices to quickly reach a high As concentration, consequently the slope is steep. Figure 6 shows a SIMS plot of a mono-emitter layer with a Ge spike 40 at the interface. The slope of the leading edge of the As profile 46 improves considerably relative to the SIMS plot shown in Figure 5 for a mono-emitter layer fabricated without the addition of  $\text{GeH}_4$ . As can be seen, the slope 46 in Figure 6 is about 4nm/dec compared to the slope 44 of 23nm/dec for the plot of Figure 5.

An example of how to grow an As-doped mono-emitter layer with a Ge spike at the interface is described below with reference to Figure 8. First, at step S1, the wafer is cleaned in such a way that no or very little native oxide is left in the Si windows in which the epitaxial layer is to be deposited. Next, at step S2, the wafer is placed in the load lock of an epitaxial reactor chamber, e.g., an ASM EPSILON™ 2000, taking care that the wafer's exposure to ambient air is minimized as much as possible. At step S3, cycle purging is performed to remove the air from the load lock, and then transfer the wafer into the reactor chamber.

At step S4, the wafer temperature in the reactor chamber is maintained at about 700°C. A continuous flow of about 20 standard liters/minute (slm) of hydrogen is also maintained through the reactor chamber. The common bake step (to remove the native oxide) at a temperature higher than the deposition temperature prior to epi growth is skipped to reduce the temperature budget of the wafer. The wafer spends one minute in the chamber at 700°C to stabilize its temperature before the process gases are turned on. This is sufficient to grow a good quality epi layer. At step S5, the process gases are turned on. In this illustrative embodiment, the process gasses include about: 100 standard cubic cm/minute (sccm) of SiH<sub>4</sub> (100%), 50 sccm of GeH<sub>4</sub> (1% in H<sub>2</sub>), and 180 sccm AsH<sub>3</sub> (0.7% in H<sub>2</sub>). The H<sub>2</sub> flow of about 20 slm is continuously maintained and the deposition process is done at atmospheric pressure. At step S6, after about 2 seconds, the GeH<sub>4</sub> flow is turned off. The other gas flows are maintained for about 180 more seconds before being turned off. At step S7, the wafer is removed from the reactor after the process gases have been purged out of the reactor chamber and the wafer has been cooled before being unloaded.

It should be understood that the specific duration of time during which the Ge source is added to the process gases can vary without departing from the scope of the

invention. In general, Ge is added during a small fraction, typically 5% or less, of the time needed to grow the mono-emitter.

This process results in an epitaxial layer with the doping profile having a Ge spike 40 at the interface and a steep leading slope 46 of the As profile, as depicted in Figure 6. Figure 7 shows a SIMS plot for the case where the  $\text{SiH}_4$  flow was increased to 150 sccm and the  $\text{GeH}_4$  (1%) flow was decreased to only 10 sccm for 5 seconds. The SIMS plot of this layer in Figure 7 shows a much smaller Ge spike 42, as would be expected. As can be seen, lowering the Ge spike 42 deteriorates the slope 48 of the leading edge of the As profile. Thus, the smaller Ge spike 42 is less effective in improving the steepness of the leading slope 48 of the As profile. The slope deteriorates from 4 nm/dec in Figure 6 (with the large Ge spike 40), to 17 nm/dec in Figure 7 (with the small Ge spike 42), to 23 nm/dec in Figure 5 when no Ge is applied.

Although described herein with reference to mono-emitters in a HBT technology, it is understood that the method described here can be used in general to improve the leading slope of in-situ deposited n-type doped layers. For instance, the method may be used with As, P and Sb, doping in-situ epitaxial and poly-silicon layers deposited by means of chemical vapor deposition (CVD). Moreover, it is understood that the invention may apply to any Si source suitable for growing Si layers by CVD. The most common sources are  $\text{SiH}_4$ ,  $\text{Si}_2\text{H}_6$ ,  $\text{Si}_3\text{H}_8$ ,  $\text{SiH}_2\text{Cl}_2$ ,  $\text{SiHCl}_3$  and  $\text{SiCl}_4$ . Any Ge source suitable to grow SiGe layers may also be used, e.g.,  $\text{GeH}_4$ ,  $\text{GeCl}_4$ .

The method is particularly useful in the temperature range of about 600-850°C, wherein the upper limit is determined by diffusion (e.g., in HBT's, deterioration of the base B profile by diffusion) and the lower limit is determined by the growth rate (e.g., below 600°C, the growth rate is too low to be of practical importance when relatively thick layers have to be deposited).

The Ge content in the spike, probably best expressed in a dose ( $\text{at}/\text{cm}^2$ ) as the SIMS will not fully resolve the spike, should be higher than  $2\text{E}14 \text{ at}/\text{cm}^2$ , as this is approximately the (insufficient) Ge content in the Ge spike of Figure 7. A Ge dose of about  $5\text{E}14 \text{ at}/\text{cm}^2$  (roughly half a monolayer when dealing with (100) oriented silicon wafers) or higher should provide sufficient results.

As noted, the invention can be applied in general to improve the profile of n-type dopants in Si layers grown by CVD. One illustrative area where it would be very useful is to better control the dopant profile of the emitters in bipolar (nnp) transistors, when the emitter is made by means of CVD and is doped in-situ. When the emitter is grown epitaxially (mono-emitter), the invention will improve transistor performance as it makes the leading slope of the n-type dopant profile steeper. Apart from the better profile control, this also allows one to reduce the vertical dimensions of the transistor, which translates in better performance at higher frequencies.

The foregoing description of the invention has been presented for purposes of illustration and description. It is not intended to be exhaustive or to limit the invention to the precise form disclosed, and obviously, many modifications and variations are possible. Such modifications and variations that may be apparent to a person skilled in the art are intended to be included within the scope of this invention as defined by the accompanying claims.

### CLAIMS

1. A method for forming an emitter-base junction, comprising:
  - providing a base layer (26); and
  - growing a doped mono-emitter layer (28) on the base layer (26) using a gas flow comprised of a set of process gases, wherein gas flow includes an addition of a germanium (Ge) source to the process gases for a first few seconds of the gas flow.
2. The method of claim 1, wherein the base layer comprises a B-doped base epitaxial layer.
3. The method of claim 2, wherein the doped mono-emitter layer is selected from the group consisting of: an As-doped epitaxial layer; a P-doped epitaxial layer, and a Sb-doped epitaxial layer.
4. The method of claim 1, wherein the Ge source is added for approximately 5% or less of an amount of time required to grow the doped mono-emitter layer.
5. The method of claim 1, wherein the Ge source is selected from the group consisting of:  $\text{GeH}_4$  and  $\text{GeCl}_4$ .
6. The method of claim 1, wherein the process gases further include: an Si source and an As source.
7. The method of claim 1, wherein the base layer comprises a C-doped SiGe layer.

8. A method of processing a wafer, comprising the steps of:
- placing the wafer into a reactor chamber;
  - maintaining an elevated temperature within the reactor chamber prior to processing;
  - passing hydrogen through the reactor chamber;
  - turning on a set of process gases, wherein the process gases include a germanium (Ge) source;
  - turning off the Ge source within a first few seconds; and
  - turning off the remaining process gases at a substantially later time.
9. The method of claim 8, wherein the elevated temperature is about 700 degrees Celsius.
10. The method of claim 8, wherein the elevated temperature is provided for about one minute.
11. The method of claim 8, wherein the process gases include an Si source and an As source.
12. The method of claim 8, wherein the wherein the Ge source is selected from the group consisting of:  $\text{GeH}_4$  and  $\text{GeCl}_4$ .
13. The method of claim 8, wherein the wherein the Ge source is added for approximately 5% or less of the amount of time required to grow a doped mono-emitter.

14. The method of claim 8, wherein the remaining process gases are turned off about 180 seconds later.

15. A method for processing a semiconductor, comprising:

growing a doped mono-emitter layer (28) on a base epitaxial layer (26) using a gas flow comprised of a set of process gases, wherein gas flow includes an addition of a germanium (Ge) source to the process gases for a first few seconds of the gas flow.