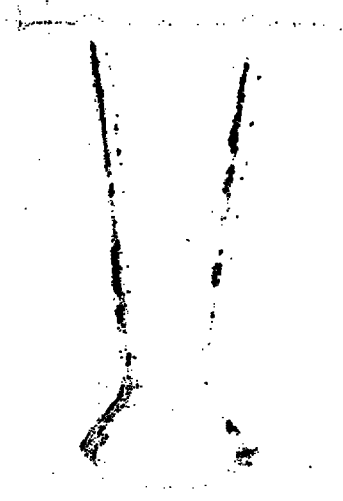


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TITLE OF THE INVENTION

DATA CONVERSION METHOD

AND RECORDING/REPRODUCING APPARATUS USING THE SAME

BACKGROUND OF THE INVENTION

Field of the Invention

The present invention relates to a data conversion method for converting digital data to signals suitable for the recording system or the transmission channel used when recording or transmitting the digital data onto magnetic tape, and a recording/reproducing apparatus employing the data conversion method.

Description of Related Art

Prior art data conversion methods employed in magnetic recording/reproducing apparatus include, for example, an 8/10 modulation method such as disclosed in "THE DAT CONFERENCE STANDARD" (issued June 1987). The 8/10 modulation method is a data conversion method in which digital data are partitioned into datawords of 8 bits each for conversion into 10-bit codewords. Fig. 1 is a circuit block diagram for explaining this data conversion method, and Fig. 2 is a data conversion table used for the same. In Fig. 1, the



reference numeral 1 designates an encoder for accepting eight-bit digital data and a one-bit table select signal (Q') at its respective inputs and for outputting a total of 11 bits, i.e. a 10-bit codeword plus a one-bit signal (Q) for selecting the table for the next codeword. Further, the numeral 2 denotes a flip-flop for delaying the codeword table select signal by one dataword. The encoder 1 includes a read-only memory (ROM) or the like which contains the data conversion table shown in Fig. 2, wherein codewords of CDS (Codeword Digital Sum) = 0 are mapped on a one-to-one basis to 256 datawords from "00" to "FF" of hexadecimal numeral, while in the case of codewords of CDS $\neq$ 0, pairs of codewords, one with CDS = +2 and the other with CDS = -2, are each mapped to one dataword, the table of $Q' = -1$ consisting of codewords of CDS = +2 and the table of $Q' = +1$ consisting of codewords of CDS = -2. The table select signal (Q) is used to select the CDS (the table) having the direction that suppresses the dispersion of charges in the codeword sequence.

The operation of the above circuit will now be explained with reference to the timing diagram of Fig. 3. In Fig. 3, the reference signs (a), (Q), and (b) correspond to inputs/outputs at the respective parts shown in Fig. 1, and the reference signs (c) and (d) respectively represent an output signal from an NRZI



converter (not shown) and a DSV (Digital Sum Variation) value at the end of codeword.

First, an eight-bit dataword "FF" is input to the encoder 1, along with the table select signal (Q') = -1, and consequently, the encoder 1 outputs a 10-bit codeword "1111101010" of CDS = +2 corresponding to "FF" for $Q' = -1$. At the same time, the table select signal $Q = -1$ is output for the next codeword. The parallel 10-bit signal is then converted to a serial signal, after which the signal is NRZI-modulated. As a result, the DSV value at the end of the codeword becomes +2.

Next, when "00" is input to the encoder 1, the encoder 1 outputs $Q = 1$ together with a 10-bit signal "0101010101" of CDS = 0 corresponding to "00" for $Q' = -1$ which is produced by introducing a one-symbol delay in the previous output $Q = -1$. As a result, the DSV value at the end of the codeword after NRZI modulation remains at +2.

Next, when "11" is input to the encoder 1, the encoder 1 outputs $Q = -1$ together with a 10-bit signal of CDS = -2 corresponding to "11" for $Q' = 1$. As a result, the DSV value at the end of the codeword after NRZI modulation becomes zero. In this manner, for each eight-bit dataword input to the encoder 1, a codeword to be output is selected



from the table of either $Q' = -1$ or $Q' = 1$ corresponding to the dataword on the basis of the table select signal output previously. The DSV at the end of each codeword after NRZI modulation can only take the value 0, +2 or -2. This means that the DSV dispersion is suppressed, as a result of which DC-free data conversion is realized.

As described above, according to the prior art data conversion method, eight-bit data is converted to a 10-bit codeword of $CDS = 0$ or $CDS = +2$ or -2 , and a DC-free signal is produced with the DSV dispersion suppressed, thereby minimizing intersymbol interference on the transmission channel and thus increasing the recording density per track. However, for recent digital magnetic recording/reproducing apparatus using a rotary head, a recording density as high as several square micrometers per bit is demanded, which necessitates not only increasing the recording density per track but also reducing the track width down to several micrometers. To implement such apparatus, it is essential to employ a dynamic tracking following (DTF) control system whereby pilot signals for tracking are recorded on the main track recorded by the rotary head and the playback head is controlled to follow the recorded track curves during playback. When the prior art data conversion method is employed in such apparatus for multiplex recording of the pilot signals, the digital signal spectral distribution has to be



obtained down to ultra low frequency ranges although the recorded information signals contain no DC components; the resulting problem is that the pilot signals cause external disturbances, leading to increased errors in the detection of the digital signals.

One possible approach to overcoming the problem of the pilot signals causing external disturbances to the digital signals may be by generating pilot signals synchronized to the digital signals. However, the prior art data conversion method is effective only in suppressing the DSV dispersion and is not capable of actively controlling the DSV, and therefore, has the problem that it cannot generate pilot signals synchronized to the digital signals.

Fig. 4 shows a DAT recording format employed in a magnetic recording apparatus using the 8/10 modulation method. As shown, according to the format of Fig. 4, ATF areas for tracking control are provided in each of which a pilot signal for tracking control is recorded. Further, Fig. 5 shows a digital VTR recording format which is disclosed in Japanese Patent Application Laid Open No.3-217179 (1991). As shown, the track is divided into a video data area, an audio data area, a servo pilot area, and a sub code area, the pilot signal being recorded in the servo pilot area only.



According to the above construction of the prior art, it is not possible to control the DSV in such a manner as desired, and a separate area has to be reserved for recording a pilot signal for tracking control. Accordingly, accurate tracking control cannot be realized without increasing the data amount and hence increasing the recording rate, which makes it difficult to achieve high density recording.

SUMMARY OF THE INVENTION

It is an object of the present invention to provide a data conversion method which, by suppressing low frequency components, can minimize intersymbol interference on the transmission channel, thus permitting increased per-track recording density, as in the prior art data conversion method, and which is capable of generating pilot signals synchronized to digital signals, which has not been possible with the prior art method, and thus achieves increased recording density with reduced track width.

It is another object of the present invention to provide a recording/reproducing apparatus optimized for the data conversion method capable of generating pilot signals synchronized to digital signals.



It is a further object of the present invention to provide a data conversion method which is capable of generating pilot signals for tracking control and which involves hardly any increase in the recording rate and therefore permits high density recording, and a recording/reproducing apparatus using such a data conversion method.

According to the present invention, there is provided a data conversion method for word-converting an r -bit first dataword to an m -bit second dataword ($r < m$) and converting the word-converted m -bit second dataword to an n -bit codeword ($m < n$), in which, for r/m word-conversion, a sequence of first datawords is divided into groups of x bits where x is the least common multiple of r and m , an arbitrary first dataword selected from x/r groups of first datawords is divided into x/m , and $r/(x/m)$ -bit data obtained by dividing the first dataword into x/m is appended to the LSB (or MSB) side of one or other of the non-divided first datawords to form the m -bit second dataword. The m -bit second dataword can thus be handled as $r + (r/(x/m))$ (or $(r/(x/m)) + r$). Therefore, if, in m/n conversion, the n -bit codeword is formed by dividing it into n_1 and n_2 bits, the data conversion can be performed by relating r to n_1 and $r/(x/m)$ to n_2 . This serves to reduce the possibility of error propagation due to a bit error that may occur in reverse data conversion.



Furthermore, when converting the word-converted m-bit second dataword to the n-bit codeword, the number of successive 0s between a bit "1" and the next bit "1" in each n-bit codeword is limited to 4, and two codewords, one with $CDS = +1$ and the other with $CDS = -1$, are paired and related to the m-bit second dataword, the two codewords being selectively used in accordance with a DSV control signal. This enables the DSV to be controlled at a desired value for each codeword, thereby achieving spectrum suppression in a relatively low frequency range. Also, by controlling the CDS polarity in accordance with the DSV control signal, a pilot signal of the DSV variation cycle synchronized to digital data can be generated in the low frequency band where the digital data power spectrum exhibits an abrupt drop.

When the above data conversion method is employed in a recording/reproducing apparatus, the number of first datawords to be recorded in a data block where an error-correcting code and an error-detection code are appended for every synchronizing signal is set at an integral multiple of x/r . The recording/reproducing apparatus thus constructed achieves an efficient code format that does not require redundant bits.



The recording/reproducing apparatus employing the above data conversion method has: decoding means for decoding n_1 bits in the reproduced n -bit codeword into r bits, the reproduced n -bit codeword being divided into n_1 bits and n_2 bits for reverse conversion into the m -bit second dataword; decoding means for decoding the n_2 bits into $r/(x/m)$ bits; decoding means for decoding the n bits into the m bits; identifying means for identifying the type of bits at prescribed positions in the n -bit codeword and for outputting an identification signal designating the identified type; and means for selecting decoded data from the respective decoding means on the basis of the identification signal supplied from the identifying means and for outputting the decoded second dataword. This construction serves to reduce the possibility of the error propagation that may occur between decoded first datawords due to a single bit random error in the n -bit codeword.

Another recording/reproducing apparatus of the invention has: means for recording multiple kinds of data in partitioned areas; means for relating 14-bit codewords of $CDS = 0$ and pairs of codewords of $CDS = \pm 2$ to respective 12-bit datawords when encoding and recording at least one of the multiple kinds of data and for encoding the data by selectively using these codewords; and means for appending one bit to each 14-bit codeword to form a pair of codewords,



one with CDS = +1 and the other with CDS = -1, when encoding and recording at least one other of the multiple kinds of data and for encoding the data by selectively using these codewords.

In the above recording/reproducing apparatus, when encoding and recording at least one of the area-partitioned multiple kinds of data, either a 14-bit codeword of CDS = 0 or a pair of codewords differing only in MSB, one with CDS = +2 and the other with CDS = -2, are related to one dataword, and the dataword is encoded by selectively using these codewords, thus constructing a DC-free code of $T_{min} = 0.86T$ and $T_{max} = 4.29T$; on the other hand, when encoding and recording at least one other of the multiple kinds of data, one bit is appended to each 14-bit codeword to form a pair of codewords, one with CDS = +1 and the other with CDS = -1, and the data is encoded by selectively using these codewords, thus constructing a code that provides the DSV coming round to the same value at prescribed intervals.

The above and further objects and features of the invention will more fully be apparent from the following detailed description with accompanying drawings.

BRIEF DESCRIPTION OF THE DRAWINGS

Fig. 1 is a diagram showing the circuit configuration



of a prior art data converting apparatus.

Fig. 2 is a code conversion table according to a prior art data conversion method.

Fig. 3 is a diagram for explaining the operation of the data converting apparatus of Fig. 1.

Fig. 4 is a diagram showing a recording format of a prior art DAT.

Fig. 5 is a diagram showing a recording format of a prior art digital VTR.

Figs. 6 is a diagram showing the number of codewords for deriving codewords in accordance with a first embodiment of the invention.

Figs. 7 is a diagram showing the number of codewords for deriving codewords in accordance with a first embodiment of the invention.

Figs. 8 is a diagram for explaining the construction of code conversion tables according to the first embodiment of the invention.

Figs. 9 is a diagram for explaining the construction of code conversion tables according to the first embodiment of the invention.

Figs. 10 is a diagram for explaining the construction of code conversion tables according to the first embodiment of the invention.

Figs. 11 is a diagram showing code conversion according



to the first embodiment of the invention.

Figs. 12 is a diagram showing code conversion according to the first embodiment of the invention.

Figs. 13 is a diagram showing code conversion according to the first embodiment of the invention.

Figs. 14 is a diagram showing code conversion according to the first embodiment of the invention.

Figs. 15 is a diagram showing code conversion according to the first embodiment of the invention.

Figs. 16 is a diagram showing code conversion according to the first embodiment of the invention.

Figs. 17 is a diagram showing code conversion according to the first embodiment of the invention.

Figs. 18 is a diagram showing code conversion according to the first embodiment of the invention.

Figs. 19 is a diagram showing code conversion according to the first embodiment of the invention.

Figs. 20 is a diagram showing code conversion according to the first embodiment of the invention.

Figs. 21 is a diagram showing code conversion according to the first embodiment of the invention.

Figs. 22 is a diagram showing code conversion according to the first embodiment of the invention.

Figs. 23 is a diagram showing code conversion according to the first embodiment of the invention.



Figs. 24 is a diagram showing code conversion according to the first embodiment of the invention.

Figs. 25 is a diagram showing code conversion according to the first embodiment of the invention.

Figs. 26 is a diagram showing code conversion according to the first embodiment of the invention.

Fig. 27 is a diagram showing the circuit configuration of a data converting apparatus for implementing the code conversion method of the first embodiment.

Fig. 28 is a diagram for explaining the operation of the data converting apparatus of Fig. 27.

Fig. 29 is a power spectrum diagram showing the effect of the first embodiment.

Fig. 30 is a diagram showing the structure of a first dataword block recorded by a recording/reproducing apparatus employing the data conversion method of the first embodiment.

Fig. 31 is a diagram showing the structure of the first dataword block recorded by the recording/reproducing apparatus employing the data conversion method of the first embodiment along with the structure of the first datawords recorded at the top of the block.

Fig. 32 is a diagram showing the configuration of a circuit for implementing a decoding method in the



recording/reproducing apparatus employing the data conversion method of the first embodiment.

Fig. 33 is a diagram showing classifications for 5-bit LSB codewords in the codewords of the first embodiment.

Figs. 34 is a diagram showing code conversion according to a second embodiment of the invention.

Figs. 35 is a diagram showing code conversion according to a second embodiment of the invention.

Figs. 36 is a diagram showing code conversion according to a second embodiment of the invention.

Figs. 37 is a diagram showing code conversion according to a second embodiment of the invention.

Figs. 38 is a diagram showing code conversion according to a second embodiment of the invention.

Figs. 39 is a diagram showing code conversion according to a second embodiment of the invention.

Figs. 40 is a diagram showing code conversion according to a second embodiment of the invention.

Figs. 41 is a diagram showing code conversion according to a second embodiment of the invention.

Figs. 42 is a diagram showing code conversion according to a second embodiment of the invention.

Figs. 43 is a diagram showing code conversion according to a second embodiment of the invention.

Figs. 44 is a diagram showing code conversion according



to a second embodiment of the invention.

Figs. 45 is a diagram showing code conversion according to a second embodiment of the invention.

Figs. 46 is a diagram showing code conversion according to a second embodiment of the invention.

Figs. 47 is a diagram showing code conversion according to a second embodiment of the invention.

Figs. 48 is a diagram showing code conversion according to a second embodiment of the invention.

Figs. 49 is a diagram showing code conversion according to a second embodiment of the invention.

Fig. 50 is a diagram showing the circuit configuration of a data converting apparatus for implementing the data conversion method of the second embodiment.

Fig. 51 is a diagram showing a code select table according to the second embodiment.

Fig. 52 is a diagram for explaining the operation of the data converting apparatus of Fig. 50.

Fig. 53 is a diagram showing a recording format of a recording/reproducing apparatus according to the second embodiment.

DESCRIPTION OF THE PREFERRED EMBODIMENTS

(Embodiment 1)

A first embodiment of the invention will now be



described below with reference to accompanying drawings.

Now suppose a first dataword length $r = 8$, a word-converted second dataword length $m = 12$, and a data-converted codeword length $n = 15$, to form a code with a modulation parameter $T_{\max}/T_{\min} = 5$. At this time, $d = 0$ and $k = 4$, where d is the minimum number of 0s between an arbitrary 1 and the next 1, and k is the maximum number of 0s between an arbitrary 1 and the next 1. The NRZI (F) rule is used to form the code. To achieve such a data conversion, the maximum number of successive 0s in each codeword is limited to 3 on the MSB side, 1 on the LSB side, and 4 within codeword. In this situation, the number of possible codewords having the MSB of 0 and satisfying the 0 run length condition is given in Fig. 6 for each CDS.

To form a DC-free code, 2^{12} pairs (4096 pairs) of codewords, each pair having codewords of different CDS polarities, should be provided. The numbers given in Fig. 6 are only for codewords whose MSB is 0; by converting the MSB to 1, codewords of reverse CDS polarity can be obtained while satisfying the 0 run length condition. Accordingly, of the codewords given in Fig. 6, only the codewords of $CDS = \pm 1$ are enough to satisfy the minimum required number of second datawords $= 2^{12}$ ($4096 < \text{number of codewords} = 4650$). Therefore, by using only the codewords of $MSB = 0$ and $CDS = \pm 1$ and by setting the MSB to 0 or 1, it is possible to suppress



the dispersion of DSV.

Fig. 7 shows possible combinations of codewords n_1 and n_2 when the codewords of $CDS = \pm 1$ given in Fig. 6 are each divided into $n_1 = 10$ bits and $n_2 = 5$ bits, n_1 representing the 10 bits on the MSB side and n_2 representing the 5 bits on the LSB side. In Fig. 7, Group A consists of n_1 codewords of $CDS = 0$, Group B of n_1 codewords of $CDS = +2$, Group C of n_1 codewords of $CDS = -2$, Group D of n_1 codewords of $+4$, and Group E of n_1 codewords of $CDS = -4$. Each of the codeword groups A to E is subdivided in accordance with the 0 run length at codeword end resulting from the concatenation of the codewords n_1 and n_2 .

First, we focus our attention on Group A. It can be seen that there are 18 different n_2 codewords that can be paired with A1 while, of the 18 codewords, 17 codewords excluding the codeword "02" can also be paired with A2. Therefore, for Group A, 16 codewords, excluding the codewords "02" and "05", are used, and $m = 12$ bits are divided into $m_1 = 8$ bits and $m_2 = 4$ bits at the time of m/n conversion, to realize m_1/n_1 (8/10) conversion and m_2/n_2 (4/5) conversion, respectively. This coding technique serves to avoid propagation of errors between divided codewords at the time of decoding. To utilize this property, when 8-bit first datawords of length (r) supplied from an error-correcting circuit are word-converted to 12-bit second data-



words of length (m), four bits separated from the eight bits are mapped to m_2 , while non-divided 8 bits are mapped to m_1 . As a result, when a random error occurred to one bit in n bits during the reconstruction process, the error occurring to the first dataword after decoding is limited only to one dataword; the error is thus prevented from propagating between datawords.

In the first embodiment, 1s and 0s used to represent one-bit signals are binary numbers, a 1 representing a high level and a 0 a low level. On the other hand, "0" to "F" used to represent datawords, codewords, or parallel data bit sequences are hexadecimal numbers.

If the above coding method is provided in 256 pairs, a single bit error in n bits during the reconstruction process can be prevented from propagating between first datawords after decoding. However, as is apparent from Fig. 7, under the condition that satisfies the modulation parameter of the data conversion method of the first embodiment, the above coding method can be applied only to Group A, and cannot be applied to the other Groups B to E.

In view of the above situation, we now consider a method of coding, as shown in Figs. 8 to 10 wherein the m_1/n_1 , m_2/n_2 coding method is divided into three major coding groups, i.e. the first coding group consisting only of Group A codewords corresponding to the first datawords m_1



= "00" to "73", the second coding group consisting of Group B and Group C codewords corresponding to the first datawords m_1 = "74" to "BA", and the third coding group consisting of the codewords in the other groups as well as the remaining codewords in Group B and Group C corresponding to the first datawords m_1 = "BB" to "FF".

First, referring to the first coding group of Fig. 8 which consists only of Group A codewords, if an error occurred to one bit in n bits in the reconstruction process, the error occurring to the first dataword after decoding is limited only to one dataword and is thus prevented from propagating between datawords.

Next, in the second coding group shown in Fig. 9, there is provided a one-to-one correspondence for the m_2/n_2 conversion, but for the m_1/n_1 conversion, two n_1 codewords are mapped to one m_1 . Therefore, of the encoded 15 bits, if the 10 bits mapped to n_1 contains a single bit error, the error occurring to the first dataword after decoding is limited only to one dataword and is thus prevented from propagating between datawords. However, if there is an error in one bit out of the five bits mapped to n_2 , error propagation can occur between first datawords after decoding from the probability point of view.

Further, in the third encoding group shown in Fig. 10, one m_1 is mapped to a plurality of n_1 codewords for the



m1/n1 conversion, while for the m2/n2 conversion, a plurality of m2 codewords are mapped to one n2. Therefore, any one bit error can cause error propagation between first datawords after decoding from the probability point of view whether the error is in n1 or n2.

In the data conversion method wherein an 8-bit first dataword is word-converted to a 12-bit second dataword which is further converted to a 15-bit codeword, the above coding method has the effect of reducing the possibility of error propagation that may occur between first datawords after decoding due to a single bit detection error in the encoded 15 bits.

Code conversion tables thus constructed are shown in Figs. 11 to 26. The numbers given in Figs. 11 to 26 represent binary digital signals in hexadecimal notation; "0" to "F" in the uppermost row each correspond to the four bits on the LSB side of a 12-bit input codeword, and "00" to "FF" in the leftmost column each correspond to the eight bits on the MSB side of a 12-bit input codeword, each row and column intersection "XXXX" forming the resulting 16-bit codeword. For example, when a 12-bit dataword "15A" is input, a codeword "9539" is obtained from the intersection between the row of "15" and the column of "A" (see Fig. 12). For a 12-bit input codeword (the second codeword), the resulting codeword consists of 16 bits, of which the MSB



corresponds to a Q signal ("1" for a high level and "0" for a low level, representing the end level of an NRZI-modulated codeword when the MSB of the premodulation codeword is "0"), the 15th bit represents the CDS information ("1" for +1 and "0" for -1), and the remaining bits from the 14th bit to the LSB correspond to the bits from the 14th bit to the LSB of the 15-bit codeword to be NRZI-modulated. For the m/n (12/15) data conversion, the codeword output is selected as 16 bits because the codeword MSB control is performed by comparing the CDS information of the codeword to be converted with the end level of the previous NRZI-modulated codeword on the basis of a DSV control signal of 50% duty cycle derived by further dividing the data conversion rate signal.

Fig. 27 is a diagram showing an example of a circuit configuration implementing the first embodiment. The reference numeral 3 designates a clock generator circuit which generates, from a channel clock for transmitting a data-converted code, a symbol clock of $f_{CH}/10$ for transmitting a first codeword (r), a clock ($f_{MW}/2$) of $f_{CH}/30$ (a value obtained by multiplying 24, the least common multiple of r and m, by n/m (10/8)) for word-converting the first dataword to the second dataword, a clock (f_{MW}) for parallel-transmitting a converted n-bit codeword, and a DSV control signal (i) for determining the variation frequency of DSV.



The numeral 4 is a shift register constructed from three stages of flip-flops (F-F) for transmitting 8-bit first datawords in parallel at the symbol clock (f_{sym}); 5 is a latch circuit that latches at the clock ($f_{MW}/2$) the 24-bit parallel signal output from the shift register 4; 6 is a selector for word-converting the first datawords of 3 bytes to two second datawords by using the clock ($f_{MW}/2$) as a select switch; 7 is an encoder for data-converting each 12-bit dataword to a codeword selected from the tables shown in Figs. 11 to 26; and 8 is an MSB controller for outputting the MSB of the codeword in accordance with the Q and CDS information supplied from the encoder 7 and the DSV control signal (i) supplied from the clock generator circuit 3, the MSB controller 8 having four EXOR circuits, A to D, and a one-word delay for delaying the end level of the previous NRZI-modulated codeword by one encoding cycle by using the clock (f_{MW}). Further, the numeral 9 designates a parallel/serial converter for loading the encoded 15-bit parallel signal at the clock (f_{MW}) and for converting the parallel signal to a serial signal which is transmitted at the channel clock (f_{CH}), and the numeral 10 indicates an NRZI modulator for causing state inversion (high to low and low to high transitions) when signal "1" is input.

Fig. 28 is a timing diagram for explaining the operation of the circuit shown in Fig. 27. The reference



signs (a) to (k), (m), (n), and (r) correspond to the respective points designated by the same signs appearing at the inputs/outputs of the respective circuit sections.

The operation of the circuit will now be described in detail. 8-bit first datawords (r) fed from an error-correcting circuit section are shifted at the symbol clock (f_{sym}) into and along the shift register 4 and are output as a 3-byte or 24-bit parallel signal. The 24-bit parallel signal is latched by the latch circuit 5 at the clock ($f_{MW}/2$) of three-symbol cycle. That is, three bytes of signals "08", "1A", and "93" are latched by the latch circuit 5 at the rising edge, between times 3 and 4, of the clock ($f_{MW}/2$) shown in Fig. 28. Of the three bytes of parallel signals, the first byte (8 bits) "08" is input to DH11 - DH4 of the selector 6, and the four bits of "1" on the MSB side of the second byte are input to DH3 - DH0 of the selector 6. Further, the last byte (8 bits) "93" is input to DL11 - DL4 of the selector 6, and the four bits of "A" on the LSB side of the second byte are input to DH3 - DH0, respectively. As a result, between time 4 and the first half of time 5 in Fig. 28, the selector 6 outputs a 12-bit parallel signal "081". Between the second half of time 5 and time 6, the selector 6 outputs a 12-bit parallel signal "93A".

With the above operation, the three 8-bit first



datawords "08", "1A", and "93" are word-converted to two 12-bit second datawords, "081" and "93", by dividing the second of the three first datawords into two and appending the respective halves to the LSBs of the first and third bytes of the first dataword. Likewise, the three bytes of the first dataword, "41", "DE", and "F2", latched by the latch circuit 5 at the rising edge, between times 6 and 7, of the clock ($f_{MW}/2$) in Fig. 28, are word-converted by the selector 6 to two second datawords "41D" and "F2E".

Next, we will describe in detail the operation for converting the 12-bit second datawords to 15-bit codewords. For the convenience of explanation, it is assumed that, at time 4 in Fig. 28, the output Q' of the one-word delay in the MSB controller 8 is low, and that the DSV value for the codeword sequence up to the converted second dataword immediately preceding "081" is 0.

In this condition, when the second dataword "081" is input to the encoder 7 during the period from time 4 to the first half of time 5, the encoder 7 outputs a signal, 8BC9, in accordance with the conversion tables shown in Figs. 11 to 26, the signal having a total of 16 bits, i.e. a codeword formed from the LSB to the 14th bit and the CDS signal and Q signal, one bit each, associated with the codeword. To describe the contents of the signal, of the four bits "1000" corresponding to "8", the MSB represents the Q signal, "0"



for a low level and "1" for a high level. Further, of "1000" corresponding to "8", the bit immediately preceding the MSB represents the CDS signal for the codeword, "0" indicating CDS = -1 and a low level and "1" indicating CDS = +1 and a high level. The remaining two bits of the "1000" corresponding to "8", plus the 12 bits "BC9", a total of 14 bits, constitute the data-converted codeword which has 14 bits of "00101111001001" from the 14th bit to the LSB.

Of the signals thus created, the Q signal and the CDS signal are input, along with the DSV control signal (i), to the MSB controller 8 which then determines and outputs the MSB of the codeword in accordance with the operation hereinafter described. The DSV control signal (i) is set at "1" (high level) if the DSV is to be dispersed in the positive direction and at "0" (low level) if the DSV is to be dispersed in the negative direction. In the present embodiment, the DSV control signal is set at a high level for the duration of times 4, 5, and 6 and at a low level for the duration of times 7, 8, and 9, so that the CDS is controlled to give +1 for encoding the second datawords "081" and "93A" and -1 for encoding the second datawords "41D" and "F2E".

The operation of the MSB controller 8 will now be described in detail. First, using the EXOR circuit A, it is checked whether the CDS value of the codeword currently



output agrees with the direction in which the DSV is to be dispersed; if they agree, a 0 is output, and if they do not agree, a 1 is output, thereby making the CDS value of the codeword agree with the dispersing direction of the DSV. Note, however, that the above output condition is based on the assumption that encoding is performed with the start point of the codeword at a low level at the time of NRZI modulation. Also note that the MSB needs to be determined by referencing the Q' signal (a 0 for a low level and a 1 for a high level) indicating the end level of the previous NRZI-modulated codeword. The output of the EXOR circuit A and the Q' signal are both input to the EXOR circuit B, and when the Q' signal is "0" (indicating that the NRZI-modulated word level at the end of the previous codeword is low), the output level of the EXOR circuit A appears unchanged at the output of the EXOR circuit B. On the other hand, when the Q' signal is "1" (indicating that the NRZI-modulated word level at the end of the previous codeword is high), since the polarity of the CDS of the codeword is inverted after NRZI modulation, the output level of the EXOR circuit A appears inverted at the output of the EXOR circuit B. The output of the EXOR circuit B is supplied as the MSB of the codeword to the parallel/serial converter 9.

To describe the above operation as applied to the present embodiment, when the second dataword "081" is input



to the encoder 7, the CDS signal output from the encoder 7 is "0", and the DSV control signal (i) is at a high level ("1") that causes the DSV to disperse in the positive direction, as can be seen from Fig. 28, so that the EXOR circuit A outputs a high level signal ("1"). At this time, the Q' signal that indicates the end level of the previous NRZI-modulated codeword is at a low level ("0"), so that the EXOR circuit B outputs a 1 as the MSB of the codeword.

As a result, a 15-bit parallel signal "1001011101" is loaded into the parallel/serial converter 9 in the middle of time 5 when the clock (fMW) goes low. The loaded bits are then output serially at the channel clock (fCH) from the parallel/serial converter 9 to form a code sequence with the MSB at the top of the sequence. The code sequence output from the parallel/serial converter 9 is fed to the NRZI modulator 10 where the polarity of the signal is inverted each time a "1" is input, the resulting signal being shown in Fig. 28(k). Here, with +1 as a high level and -1 as a low level, the CDS can be calculated as +1, which indicates that the DSV of the code sequence is in the positive dispersing direction.

With the above operation, the 12-bit dataword is data-converted to the 15-bit codeword in accordance with the DSV control signal, but it is further necessary to check the end level of the NRZI-modulated codeword, as previously de-



scribed. This is accomplished by the following operation.

The Q signal from the encoder 7 and the MSB signal from the EXOR circuit B are input to the EXOR circuit C in the MSB controller 8. When the MSB is "0", the Q signal appears unchanged at the output of the EXOR circuit C. On the other hand, when the MSB is "1", the number of inversions that occur in the NRZI modulation increases by one as the number of 1s in the codeword increases by one, and therefore, the Q signal is inverted for output. During the NRZI modulation, the polarity is inverted between positive and negative in accordance with the level of the connected signal.

Therefore, the output of the EXOR circuit C is input to the EXOR circuit D along with the Q' signal indicating the word end level of the previous NRZI-modulated codeword, and when the Q' signal is "0" (indicating the word end level after NRZI modulation is low), the output signal of the EXOR circuit C appears unchanged at the output of the EXOR circuit D. On the other hand, when the Q' signal is "1" (indicating the word end level after NRZI modulation is high), the output of the EXOR circuit C is inverted through the EXOR circuit D. The output of the EXOR circuit D is supplied to the one-word delay as a signal indicating the end level of the NRZI-modulated codeword for the immediately following data conversion.

To describe the above operation as applied to the



present embodiment, when the second dataword "081" is input to the encoder 7, the Q signal output from the encoder 7 is "1", and the MSB output from the EXOR circuit B is also "1", as can be seen from Fig. 28, so that the output of the EXOR circuit D is at a low level ("0"). At this time, the signal Q' that indicates the end level of the previous NRZI-modulated codeword is at a low level ("0"), and therefore, the EXOR circuit D outputs a signal "0" indicating that the end level of the NRZI-modulated codeword is low, the signal "0" being input at the clock (f_{MW}) to the one-word delay through which the signal is delayed by one encoding cycle. By repeating the above operation for every m/n data conversion with one word delay at each time, the end level of each codeword can be checked correctly for continuous sequences of codewords.

As described above, the data that has been word-converted by the selector 6 from 8-bit first datawords to 12 bit second datawords is converted by the encoder 7 to a 16-bit codeword, which is further converted by the MSB controller 8 to a 15-bit codeword, capable of determining the dispersing direction of the DSV as desired by the DSV control signal (i), by converting the two bits on the MSB side of the 16-bit codeword to a one-bit signal that determines the polarity of the CDS. Likewise, subsequent second datawords "93A", "41D", and "F2E" are respectively input to the



encoder 7 and converted to the signal shown in Fig. 28(j), with their CDSs being controlled in accordance with the DSV control signal (i). As a result, the DSV value at the codeword end obtained at the output of the NRZI modulator 10 has a variation width $p - p_2$ over four data conversion cycles as shown in Fig. 28(k), the resulting signal thus being made to synchronize with the DSV control signal.

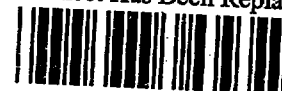
The power spectrum of the digital signal is dependent on the state transition probability, and by keeping the DSV variation cycle at a constant value, the state transition occurring at the DSV variation cycle becomes high, thus making it possible to obtain a spectrum having high power at frequencies corresponding to the DSV variation cycle. In the present embodiment, the cycle of the DSV control signal is selected to be equal to four m/n data conversion cycles. However, if the signal cycle is set equal to about 10 data conversion cycles, it will be possible to obtain a relatively low frequency signal corresponding to the DSV variation cycle synchronized with the digital data, and such a low frequency signal can be used as a tracking pilot signal that will become necessary when the track width is reduced. Fig. 29 is a diagram illustrating the power spectrum obtained when first datawords constructed from 8-bit M-sequence random signals expressed as $X^{23} + X^5 + 1$ are input in a circuit constructed in accordance with the first



embodiment but with the cycle of the DSV control signal set equal to ten m/n data conversion cycles. As can be seen from Fig. 29, the resulting spectrum has no DC content (DC-free) and, at the same time, exhibits high power only at frequencies corresponding to the cycle of the DSV control signal.

We will now describe a digital magnetic recording/reproducing apparatus that can be constructed into a system optimized for the above-described data conversion method.

Digital magnetic recording/reproducing apparatus such as DAT, digital VTR, etc. have the characteristic of being insusceptible to system variation in the sense that degradation in the signal-to-noise ratio does not lead to degradation in the audio and video reproduction performance as long as 1s and 0s can be distinguished. On the other hand, there is some danger with such digital apparatus that only a single bit error in a large volume of information may entirely change the contents of the information. Therefore, in digital magnetic recording/reproducing apparatus, it is essential to employ error-correcting codes for correction of errors caused on the transmission channel. Usually, error-correcting codewords are recorded in error-correcting code blocks separated from one another by a synchronizing signal as shown in Fig. 30. In Fig. 30, the numeral 21 is the



synchronizing signal for separating one error-correcting code block from another, 22 is an ID signal for the block identified by the track number or the synchronizing signal, 23 is a parity-check codeword for checking whether the ID signal is correctly reproduced, 24 is an audio/video sector, and 25 is an error-correcting code. Rotary head type digital magnetic recording/reproducing apparatus usually have about 100 such blocks per track, each block being separated by the synchronizing signal.

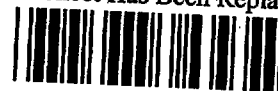
The following description deals with a method of setting the amount of information for each block.

The synchronizing signal 21 serves not only as a signal for separating each error-correcting code block but also as a signal for executing word synchronization for decoding the codeword, encoded and recorded as previously described, into the original dataword. The synchronizing signal thus has a very important role, and therefore, a unique signal that does not usually appear in the recorded signal sequences is often used as the synchronizing signal. This unique signal can only be obtained by reconvertng the data-converted codeword. According to the data conversion method of the first embodiment in which 8-bit first datawords are first converted to 12-bit second datawords and then converted to 15-bit codewords, the synchronizing signal length corresponds to 1.5 bytes in the original first datawords. There-



fore, if the synchronizing signal sector is constructed from one-byte synchronizing signal data plus 0.5 byte obtained by dividing the first dataword, these components would become separated at the time of decoding, so that the 0.5 byte in the synchronizing signal sector would cause a fixed error and therefore, the one byte data immediately following the synchronizing signal data would also cause a fixed error. This problem may be solved by inserting a dummy dataword of one byte immediately following the first dataword (which may be formed from a fixed pattern) used for the synchronizing signal.

However, it is not advantageous in terms of space utilization to add a dummy dataword in a limited package. Therefore, in the recording/reproducing apparatus employing the data conversion method of the first embodiment, the first dataword used for the synchronizing signal is constructed from a fixed pattern of one byte, and the immediately following first dataword is constructed from a fixed pattern of four bits on the MSB side and data (e.g., a cue signal, track address, etc.) of four or less bits on the LSB side. Ordinary 8-bit datawords are mapped starting with the first dataword of the third byte. The pattern of the synchronizing signal sector may be set in any pattern suitable for the reversion performed after ordinary data conversion.



We will now describe a method of setting the number of first datawords for each block separated by the synchronizing signal. According to the data conversion method of the first embodiment, r -bit first datawords are first word-converted to m -bit second datawords and then data-converted to n -bit codewords. This requires word synchronization for every x bits, where x is the least common multiple of r and m . For example, in the present embodiment, $r = 8$ and $m = 12$, and hence the least common multiple is 24 bits, so that the first codewords are word-synchronized for every three bytes. Since word synchronization is performed for every three bytes in each block, as described above, if the number of first datawords in the block is not an integral multiple of 3, the first dataword remaining after dividing the number by 3 will cause a fixed error. Therefore, in the recording/reproducing apparatus employing the data conversion method of the first embodiment, the number of first datawords per block is selected to be equal to an integral multiple of x/r .

The following describes a method of converting the reproduced 15-bit codeword back to the original 12-bit second dataword in the recording/reproducing apparatus employing the above-described data conversion method.

Fig. 32 is a diagram illustrating an example of a circuit configuration for decoding the reproduced 15-bit



code-word into the original 12-bit second dataword (m), employed in the recording/reproducing apparatus using the data conversion method of the first embodiment. In Fig. 32, the reference numeral 11 is an NRZI demodulator for NRZI-demodulating the reproduction signal transmitted by a reproduction channel clock; 12 is a serial/parallel converter for converting the NRZI-demodulated serial signal, fed from the NRZI demodulator 11, to a 15-bit parallel signal by using a reproduction word clock which is word-synchronized by a synchronizing signal appended to the top of each block; 13 is a first decoder for accepting at its input the 10 bits n1 on the MSB side of the 15-bit codeword (n) output from the serial/parallel converter 12 and for decoding the n1 into a dataword that forms the eight bits on the MSB side of the second dataword; and 14 is a second decoder for accepting at its input the five bits n2 on the LSB side of the 15-bit codeword (n) output from the serial/parallel converter 12 and for decoding the n2 into a dataword that forms the four bits on the LSB side of the second dataword. The numeral 15 designates a third decoder for decoding the 15-bit codeword, output from the serial/parallel converter 12, into 12-bit decoded data. The third decoder 15 is constructed to perform one-to-one decoding when the five bits on the LSB side is of a prescribed type.

Furthermore, the reference numeral 16 indicates an LSB



discriminating circuit which accepts at its input the five bits on the LSB side of the 15-bit codeword output from the serial/parallel converter 12, and which discriminates the type of the codeword and outputs a control signal (o) designating the classification type; and 17 refers to a selector which selects either the 12-bit dataword having decoded data from the first decoder 13 and the second decoder 14 or the 12-bit dataword from the third decoder 15 by using the control signal supplied from the LSB discriminating circuit 17 as a select SW, and which generates the second dataword (m) after decoding.

The operation of this embodiment will now be described. The reproduction signal is NRZI-demodulated by the NRZI demodulator 11 and fed to the serial/parallel converter 12 through which the demodulated serial signal is converted to a 15-bit codeword (n). Of the 15 bits in the codeword (n), the 10 bits n1 on the MSB side are entered to the first demodulator 13, and the five bits n2 on the LSB side are fed to the second demodulator 14 as well as to the LSB discriminating circuit 16. On the other hand, all the 15 bits of the codeword (n) are loaded directly into the third demodulator 15.

We will now describe in detail the operation of decoders for decoding the 15-bit codeword back into the 12-bit second dataword. From Figs. 8 to 10, the five-bit codeword



n2 on the LSB side of the 15-bit codeword can be classified in relation to the demodulated 4-bit dataword m2, as shown in Fig. 33. The codewords classified as the first LSB code group in Fig. 33 correspond to the LSB codewords n2 in the first and second coding groups in Figs. 8 and 9 as well as in the first n1 group for m1 = "BB" to "E7" in the third coding group in Fig. 10, and each n1 in the n1 group is related to one decoding data m1 within the limits of the first LSB code group. Further, the codewords classified as the second LSB code group correspond to the LSB codewords classified as the second n1 group in the third coding group as well as the fourth n1 group for m1 = "EE" to "FF" in the same coding group. The codewords classified as the third LSB code group correspond to the LSB codewords classified as the third n1 group, while the codewords classified as the fourth LSB code group correspond to the LSB codewords in the n1 group for m1 = "E8" to "FF". Note, however, that the n1 group in the second to the fourth LSB code groups overlaps with the n1 group in the first LSB code group, and that, in some cases, a plurality of m2 are mapped to one LSB codeword n2.

Now, the first decoder 13 decodes the 10 bits on the MSB side into an eight-bit dataword. In this case, the top bit in the 10-bit codeword is a control bit for controlling the DSV during demodulation and may therefore be disregarded



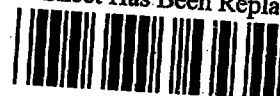
at the time of decoding. Thus, the remaining nine bits are decoded. The decoding is performed on the codewords in the first and second coding groups in Figs. 8 and 9 as well as in the first n_1 group for $m_1 = "BB"$ to $"E7"$ in the third coding group in Fig. 10, and the decoded 8-bit dataword is applied to $V_{11} - V_4$ on the selector 17 as data representing the eight bits on the MSB side of the second dataword. On the other hand, the second decoder 14 decodes the five bits on the LSB side into a four-bit dataword. In this case, the decoding is performed on the codeword n_2 in the first LSB code group. The decoded 4-bit dataword is applied to $V_3 - V_0$ on the selector 17 as data representing the four bits on the LSB side of the second dataword. The third decoder 15 decodes the input 15-bit codeword into a 12-bit dataword. In this case also, the top bit on the MSB side is excluded, as in the case of the first decoder 13, and the remaining 14 bits are decoded. The decoding is performed only when the five-bit LSB codeword falls in one of the second to the fourth LSB code groups, and the decoded 12-bit dataword is applied to $W_{11} - W_0$ on the selector 17.

The selector 17 is switched to select either the dataword supplied from the first decoder 13 and second decoder 14 or the dataword supplied from the third decoder 15, and outputs the selected dataword as the decoded second dataword; the switching of the selector 17 is controlled by



a control signal supplied from the LSB discriminating circuit 16. Of the 15 bits in the codeword, the five bits n2 on the LSB side are input to the LSB discriminating circuit 16 to discriminate the type of the LSB codeword. For example, if the LSB codeword n2 is a codeword discriminated as belonging to one of the second to the fourth LSB code groups, the LSB discriminating circuit 16 outputs a control signal (o) indicating the discriminated type and applies it to the select SW on the selector 17. When no control signal (o) is received, the selector 17 selects the eight-bit MSB dataword V11 - V4 supplied from the first decoder 13 and the four-bit LSB dataword V3 - V0 supplied from the second decoder 14 and outputs the resulting 12-bit dataword V. On the other hand, when the control signal (o) is received, the selector 17 is switched to select the 12-bit dataword W decoded by the third decoder 15.

Thus, the selector 17 outputs the 12-bit dataword m obtained by reconvertng the codeword that was encoded in accordance with the tables shown in Figs. 8 to 10. As described, the 15-bit codeword is decoded on a one-to-one basis to the 12-bit dataword only when the five-bit LSB codeword n2 is discriminated as belonging to one of the second to the fourth LSB code groups in Fig. 33; otherwise, the 15-bit codeword is decoded by dividing it into 10 bits on the MSB side and five bits on the LSB side. This con-



struction serves to reduce the possibility of the error propagation that may occur between decoded first datawords due to a single bit detection error in the 15-bit codeword.

In the above decoding method, the discrimination of the five-bit LSB codeword is determined by which of the two major groups, the first LSB code group or the second to fourth LSB code group, the LSB codeword belongs to. However, in an alternative method, the types of codeword may be classified into three major groups, for example, the first LSB code group, the second LSB code group, and the third/fourth LSB code group, and four decoders, i.e. the first to the fourth decoders, may be provided, the outputs of these decoders being selected accordingly by using a control signal from the LSB discriminating circuit. Such configuration may somewhat increase the circuit complexity compared to that of the above embodiment, but will serve to further reduce the possibility of error propagation between decoded first datawords.

Thus, according to the first embodiment, eight-bit first datawords are first word-converted to 12-bit second datawords, and then, the 12-bit second datawords are converted to 15-bit codewords, each having bits of CDS = +1 or -1, by executing word-synchronization for every two second datawords, which is the least common multiple of the first and second datawords. In the conversion process, the first



byte of the first dataword is mapped to the eight bits on the MSB side of the first of the two second datawords, and the four bits on the MSB side of the second byte of the first dataword are mapped to the four bits on the LSB side of the first of the two second datawords. For the second of the two second dataword, the third byte of the first dataword is mapped to the eight bits on the MSB side, while the four bits on the LSB side of the second byte of the first dataword are mapped to the four bits on the LSB side of the second of the two second datawords, thus accomplishing the 8/12 word-conversion. Thereafter, each 12-bit dataword is converted to a 15-bit codeword (12/15 data conversion). This encoding method permits the 8/10 encoding of non-divided first datawords and the 4/5 encoding of divided first datawords, which serves to reduce the possibility of the error propagation that may occur, due to a single bit error in the codeword, between first datawords during reverse conversion at the time of decoding. Furthermore, when this data conversion method is applied to a recording/reproducing apparatus, it is possible to construct a system capable of efficient recording of data without requiring redundant bits, the system being constructed such that the number of first datawords for each block separated by a synchronizing signal is set at a multiple of r/x and that the first dataword as the synchronizing signal at the beginning of the

block is formed from a fixed pattern and the immediately following first dataword is formed from a fixed pattern of four bits on the MSB side and data of four or less bits (e.g., cue signal, track address, etc.) on the LSB side.

On the other hand, when decoding the 15-bit codeword into the 12-bit second dataword, the 15-bit codeword is divided into 10 bits on the MSB side and five bits on the LSB side, and the 10 bits are decoded into eight bits by the first decoder and the five bits are decoded into four bits by the second decoder, while the 15 bits are decoded into 12 bits by the third decoder. The discriminating circuit discriminates the type of the five bits on the LSB side of the 15-bit codeword and outputs a control signal indicating the discriminated type, on the basis of which the decoded data from the decoders are selected to reconstruct the second dataword. Thus, the codeword is decoded by reverse conversion of 10/8 and 5/4, except when the LSB codeword falls under specific conditions. This has the effect of reducing the possibility of the error propagation that may occur between decoded first datawords due to a detection error in the codeword.

(Embodiment 2)

A second embodiment of the invention will now be described below. Suppose a code of dataword length = 12 and codeword length = 14 with one bit added to form a code with



$T_{max}/T_{min} = 5$. Here, let $d = 0$ and $k = 4$. The NRZI(F) rule is used to construct the code. To satisfy $k = 4$ in each codeword, the number of successive 0s in the codeword is limited to 4, and since one bit is inserted between codewords, the number of successive 0s is limited to 2 on the MSB side and 1 on the LSB side.

To form a DC-free code, 4096 pairs of codewords, each pair having codewords of different CDS polarities, should be provided. There are 2481 codewords with $CDS = 0$, 2169 codewords with $CDS = +2$, and 1888 codewords with $CDS = -2$, which satisfy the above conditions. Hence, 2481 codewords with $CDS = 0$ and 1615 pairs of codewords with $CDS = \pm 2$, which differ only in MSB, are used to suppress the dispersion of DSV to achieve DC-free modulation. Code conversion tables thus constructed are shown in Figs. 34 to 49. The data given in Figs. 34 to 49 represent binary digital signals in hexadecimal notation. For every 12-bit input data (dataword), there are output a total of 16 bits, i.e. a 14-bit codeword, one-bit data (hereinafter represented by Q) indicating the number of inversions performed on the NRZI-modulated codeword, and the CDS (a zero or nonzero bit) of the codeword.

Fig. 50 is a diagram illustrating an example of a circuit configuration implementing the second embodiment. In Fig. 50, the reference numeral 33 is an encoder for

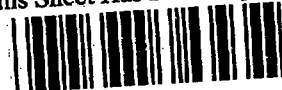


converting 12-bit digital data (dataword) to 16-bit digital data shown in Figs. 34 to 49; 34 and 36 are NOT gates; 35, 37, 38, and 39 are EXOR gates; 40, 42, and 48 are flip-flops; 41 and 46 are selectors; 43 is a parallel/serial converter for converting 14-bit or 15-bit parallel data to a serial data sequence; 44 is a counter; 45 is a four-input NAND gate; and 47 is an NRZI modulator for processing the codeword, converted to serial data, so that the signal polarity is inverted each time a 1 is input.

Fig. 51 shows a code select table used to determine a code to be selected in accordance with the current and the previous DSV control signal values, the CDS value of the codeword just selected, and the previous Q' signal.

Fig. 52 is a diagram illustrating code conversion and DSV value variation according to the second embodiment. In Fig. 52, (a) is a pilot signal (write at "1"); (b) is a DSV control signal (positive direction at "1"), (c) is input data (12 bits), (d) is a code select signal Q', (e) is a selected codeword, (f) is a signal waveform to be recorded, and (g) is a DSV value at the end of each codeword.

Fig. 53 is a diagram illustrating the recording format of a magnetic recording/reproducing apparatus according to the second embodiment. In Fig. 53, subcode signals, etc. are recorded in the subdata areas (SUB1, SUB2), and video and audio signals are recorded in the main



data area (MAIN). Pilot signals are recorded in the subdata areas (SUB1, SUB2).

The circuit operation of the second embodiment will now be described below with reference to Fig. 50.

First, when the pilot area signal output from the flip-flop 48 is "0", i.e. when data other than that for the subdata area is to be encoded for recording, 12-bit data is input to the encoder 33 where the 12-bit data is converted to a 14-bit codeword (parallel) by using the code select signal Q' supplied from the flip-flop 42. The resulting 14-bit codeword is supplied to the parallel/serial converter 43. The encoder 33 also outputs a Q signal which is supplied to the selector 41. On the other hand, the selector 46 selects "10" by the input pilot area signal "0", which sets the load value of the counter 14 to "0010", and the counter 14 outputs a load CLK of one CLK width to the parallel/serial converter 43 for every 14 CH-CLKs. The parallel/serial converter 43 converts the input 14-bit parallel codeword to serial data which is fed to the NRZI modulator 47. At this time, the output of the NOT gate 34, i.e. the LSB, is input to the parallel/serial converter 43, but since a load CLK is input for every 14 CH-CLKs, the LSB is not output from the parallel/serial converter 43. The serial codeword input to the NRZI modulator 47 is NRZI-modulated for output. The Q signal output from the encoder



33 is input to the selector 41 which selects the Q signal by the pilot area signal and supplies it to the flip-flop 42.

On the other hand, when the pilot area signal output from the flip-flop 48 is "1", i.e. when data for the subdata area is to be encoded for recording, 12-bit data is input to the encoder 33 which converts the 12-bit data to a 14-bit codeword (parallel) by using the code select signal Q' supplied from the flip-flop 42. The resulting 14-bit codeword is supplied to the parallel/serial converter 43. The encoder 33 also supplies a Q signal to the selector 41 and the NOT gate 34, and a CDS signal to the EXOR gate 35. The selector 46 selects "01" by the input pilot area signal "1", which sets the load value of the counter 14 to "0001", and the counter 14 supplies a load CLK of one CLK width to the parallel/serial converter 43 for every 15 CH-CLKs. The parallel/serial converter 43 converts the input 14-bit parallel codeword and LSB to serial data which is supplied to the NRZI modulator 47. The serial codeword input to the NRZI modulator 47 is NRZI-modulated for output. The DSV control signal is input to the flip-flop 40 and the EXOR gate 39, the output of the flip-flop 40 being coupled to the other input of the EXOR gate 39. The output of the EXOR gate 39, i.e. the exclusive OR sum of the current DSV control signal and the previous DSV control signal, is supplied to one input of the EXOR gate 38. The EXOR gate 35



EXORs the CDS signal output from the encoder 33 with the Q' signal. The output of the EXOR gate 35 is inverted through the NOT gate 36 and applied to one input of the EXOR gate 37. The EXOR gate 37 EXORs the output of the NOT gate 36 with the Q' signal and supplies the result to the other input of the EXOR gate 38. The EXOR gate 38 EXORs the outputs of the EXOR gates 37 and 39 and supplies the result to the other input of the selector 41. In this manner, the signal selected in accordance with the codeword select table is output as a Q" signal. The Q" signal is selected by the pilot area signal and is fed to the flip-flop 42 to form a code select signal Q' for the next coding.

Suppose, for example, that the pilot area signal is "0", the input data is "3FF", the previous polarity is "1", and the Q' signal is "0". In this case, the 14-bit codeword output from the encoder 33 is "11001000010111"; the CDS is -2 and the DSV is also -2. As a result, the Q signal "0" is output. Next, when data "200" is input, since the Q' signal, i.e. the previous Q signal, is "0", the selected codeword is "01110011011010"; the CDS is +2 and the DSV is 0. Next, when the pilot area signal and the DSV control signal both go to a "1" and data "E11" is input, since the Q' signal is "1", the output codeword is "11010111010101", and a Q signal of "0" and a CDS signal of "0" are output; CDS and DSV are both 0. When data "715" is input, since the Q'

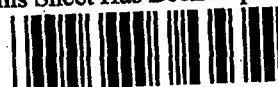


signal is "1", the selected codeword is "00101111101001" and the LSB is "0"; CDS and DSV are both +1. Next, when data "BFC" is input, since the Q' signal is "1", the selected codeword is "10100111101110" and the LSB is "1"; CDS is +1 and DSV is +2. The above operation is repeated for the subdata areas where the pilot area signal is "1", thereby achieving a modulation method in which the DSV varies at the cycle of the DSV control signal.

Using the above-described modulation method, a tracking servo pilot signal is recorded at two places within one track. Therefore, in the subdata areas (SUB1, SUB2), one LSB bit is added to the 14-bit codeword to form a 15-bit codeword, as described previously, and modulation is performed on the codeword including the pilot signal, while for other areas, the 14-bit codeword is directly modulated.

According to the format shown in Fig. 53, two subdata areas are provided within one track, and the pilot signals are recorded in these areas. Alternatively, three or more pilot signal recording areas may be provided within one track in order to enhance the tracking accuracy with a narrower track. It will also be appreciated that the pilot signal may be recorded in any portion within the subdata areas.

As described, according to the second embodiment, 12-bit datawords are each converted to a 14-bit codeword which,



after NRZI modulation, has a succession of the same level, more than one bit long and five bits at maximum, and provides $CDS = 0, +2$ or -2 , the CDS value being controlled to suppress the dispersion of DSV, thus accomplishing a DC-free modulation method. Furthermore, in areas where pilot signals are recorded, one bit is added to the 14-bit codeword to form codewords of $CDS = \pm 1$, and the modulation is performed so that the DSV varies in synchronism with the DSV control signal to produce a tracking control pilot signal. This eliminates the need for ATF areas, the areas where only tracking control signals are recorded. Moreover, since one bit is added to the codeword and the pilot signal is recorded in a restricted area, it is not necessary to substantially raise the recording rate, and therefore, high density recording is achieved. Furthermore, since the modulation method is basically the same for both the pilot signal areas and other areas, the configuration does not involve any appreciable increase in the circuit complexity.

As this invention may be embodied in several forms without departing from the spirit of essential characteristics thereof, the present embodiment is therefore illustrative and not restrictive, since the scope of the invention is defined by the appended claims rather than by the description preceding them, and all changes that fall within metes and bounds of the claims, or equivalence of



such metes and bounds thereof are therefore intended to be embraced by the claims.

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CLAIMS

1. A data conversion method for word-converting an r -bit first dataword to an m -bit second dataword ($r < m$) and converting the word-converted m -bit second dataword to an n -bit codeword ($m < n$), comprising the steps of:

dividing a sequence of first datawords into groups of x bits where x is the least common multiple of r and m ;

dividing into x/m an arbitrary first dataword selected from a group which consists of x/r first datawords; and

forming the m -bit second dataword by appending $r/(x/m)$ -bit data, obtained by dividing the first dataword into x/m , to the LSB or MSB side of one or other of the non-divided first datawords.

2. A recording/reproducing apparatus employing the data conversion method of claim 1, comprising:

means for formatting blocks so that each block separated by a synchronizing signal contains the first datawords of the number equal to an integral multiple of x/r .

3. A recording/reproducing apparatus employing the data conversion method of claim 1, comprising:

means for mapping r bits and $r/(x/m)$ bits to a second dataword corresponding to a synchronizing signal; and

means for mapping the remaining bits of the divided



first dataword to a signal, other than the synchronizing signal, that can complete as data with the remaining bits alone.

4. A recording/reproducing apparatus employing the data conversion method of claim 1, comprising:

first decoding means for decoding n_1 bits in the reproduced n -bit codeword into r bits, the reproduced n -bit codeword being divided into n_1 bits and n_2 bits for reverse conversion into the m -bit second dataword;

second decoding means for decoding the n_2 bits into $r/(x/m)$ bits;

third decoding means for decoding the n bits into the m bits;

identifying means for identifying the type of bits at prescribed positions in the n -bit codeword and for outputting an identification signal designating the identified type; and

means for selecting decoded data from the first, second, or third decoding means on the basis of the identification signal supplied from the identifying means and for outputting the decoded second dataword.

5. A data converting apparatus for word-converting an r -bit first dataword to an m -bit second dataword ($r < m$) and converting the word-converted m -bit second dataword to an n -



bit codeword ($m < n$), comprising:

means for dividing a sequence of first datawords into groups of x bits where x is the least common multiple of r and m ;

means for dividing into x/m an arbitrary first dataword selected from a group which consists of x/r first datawords; and

means for forming the m -bit dataword by appending $r/(x/m)$ -bit data, obtained by dividing the first dataword into x/m , to the LSB or MSB side of one or other of the non-divided first datawords.

6. A data conversion method for converting an m -bit dataword to a codeword consisting of a greater number of bits than m , comprising the steps of:

a first data conversion process wherein the m -bit dataword is converted to an n -bit codeword having a finite digital sum variation (DSV); and

a second data conversion process wherein the DSV is controlled at a desired value by appending one bit to the n -bit codeword obtained by the first data conversion process.

7. A data conversion method for dividing digital data first into 12-bit datawords and then converting the 12-bit datawords to 14-bit codewords,

wherein the number of successive 0s between a 1 and a 1 in each of the codewords is limited to 4 within the codeword



and to 3 between codewords, and codewords having a codeword digital sum (CDS) of 0 are directly related to the 12-bit data, while for codewords having a CDS of +2 or -2, two codewords that differ only in MSB are paired and related to the 12-bit data, the two codewords being switched selectively by using polarity signals of the respective codewords.

8. A data conversion method for dividing digital data first into 12-bit datawords and then converting the 12-bit datawords to 15-bit codewords,

wherein one bit is appended to a 14-bit codeword converted in accordance with the data conversion method of claim 7, to form a pair of codewords, one having a CDS of +1 and the other having a CDS of -1, with the number of successive 0s between a 1 and a 1 in the code sequence being limited to 4, and one or other of the pair of codewords is selected in accordance with a DSV control signal with the DSV being made to vary in synchronism with the DSV control signal.

9. A magnetic recording/reproducing apparatus for recording multiple kinds of data in partitioned areas, wherein

when converting digital data to codewords for recording, the data conversion method of claim 8 is used for

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recording one or more areas within one track and the data conversion method of claim 7 is used for recording the other areas in the same track.

10. A data converting apparatus for converting an m-bit dataword to a codeword consisting of a greater number of bits than m, comprising:

means for converting the m-bit data to an n-bit codeword having a finite digital sum variation (DSV) as a first data conversion process; and

means for controlling the DSV at a desired value by appending one bit to the n-bit codeword obtained by the first data conversion process as a second data conversion process.

11. A data conversion method for word-converting first datawords, the method comprising, for each group of n first datawords, dividing x of the datawords by (n-x) and adding each divided part to a respective one of the other datawords in the group to form respective second datawords, and converting the second datawords to codewords of greater length.



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