CLAIMS:

1. A semiconductor device, comprising:
a semiconductor fin disposed above a semiconductor substrate, the semiconductor fin having a central protruding segment spaced apart from a pair of protruding outer segments along a length of the semiconductor fin;
a cladding layer region disposed on the central protruding segment of the semiconductor fin;
a gate stack disposed on the cladding layer region; and
source/drain regions disposed in the pair of protruding outer segments of the semiconductor fin.

2. The semiconductor device of claim 1, further comprising:
a second cladding layer region disposed on one of the pair of protruding outer segments; and
a third cladding layer region disposed on the other of the pair of protruding outer segments,
wherein the second and third cladding regions are discrete from, but contiguous with, the cladding layer region disposed on the central protruding segment of the semiconductor fin.

3. The semiconductor device of claim 1, wherein the semiconductor fin and the cladding layer region together provide a compliant substrate.

4. The semiconductor device of claim 1, wherein the central protruding segment is spaced apart from the pair of protruding outer segments by an isolation layer.

5. The semiconductor device of claim 1, wherein the semiconductor fin consists essentially of silicon, and the cladding layer region consists essentially of germanium.

6. The semiconductor device of claim 4, wherein the semiconductor device is a PMOS device.

7. The semiconductor device of claim 1, wherein the semiconductor fin consists essentially of silicon, and the cladding layer region consists essentially of a III-V material.

8. The semiconductor device of claim 7, wherein the semiconductor device is an NMOS device.