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(54) Title: THREE-DIMENSIONAL STACKING SEMICONDUCTOR ASSEMBLIES WITH NEAR ZERO BOND LINE THICKNESS

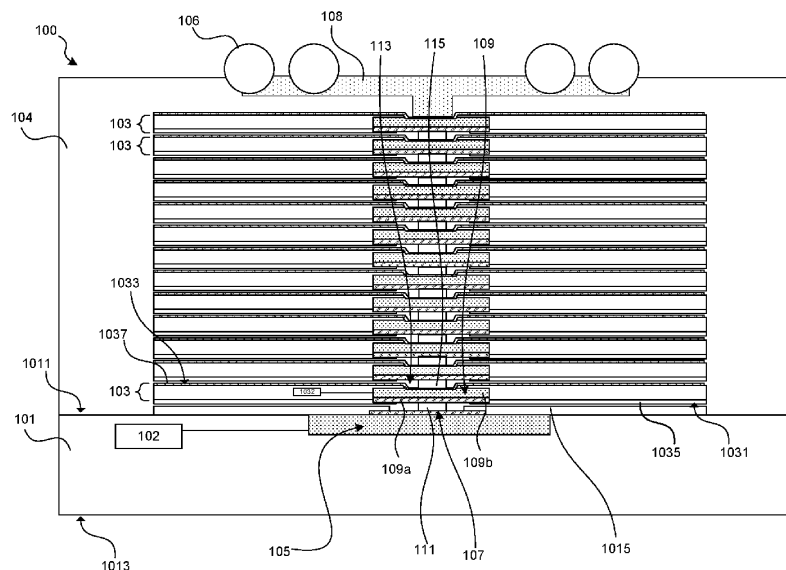


FIG. 1

(57) Abstract: Semiconductor device package assemblies and associated methods are disclosed herein. In some embodiments, the semiconductor device package assembly includes (1) a base component having a front side and a back side opposite the first side, the base component having a first metallization structure at the front side, the first metallization structure being exposed in a contacting area at the front side; (2) a semiconductor device package having a first side and a second side, the semiconductor device package having a second metallization structure at the first side; and (3) a metal bump at least partially positioned in the recess and electrically coupled to the second metallization structure and the first metallization structure.

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