

Specification

The invention relates to a method of regulating a clock motor having a permanent-magnetic rotor, which comprises at least one pair of poles, and a stator with two or more windings of which at least one winding is acted upon by control pulses as a working winding and at least one further winding serves as a control winding for the delivery of pulses proportional to the rotor movement in relation to the stator, which pulses are converted into rectangular actual-frequency pulses and, during the nominal running regulation, are compared, with regard to their width and phase position, with desired frequency pulses of preset frequency, while, in the event of actual-frequency pulses lagging behind the desired-frequency pulses, control pulses are delivered to the working winding to accelerate the permanent magnetic rotor and in the event of the speed of the permanent magnetic rotor dropping below a preset value, a self-starting is initiated for the step-by-step or quasi-continuous increase of the rotor speed, in that the control pulses are applied alternately to the working winding and control winding or cyclically to the working winding, control winding and further windings, and wherein, when a fixed speed is reached, the self-starting is automatically switched off and the nominal running regulation is switched on, as well as to a device for carrying out this method, as defined in the preamble to Claim 3.

A method and a device of the type mentioned at the beginning is known from DE-A 2 949 947; they serve for the regulation of reaction motors of time-keeping devices such as clocks, and the motor comprises a permanent magnetic rotor with at least one pair of poles and a stator with two or more windings to one of which driving pulses are applied. In the known method of regulation, a voltage proportional to the speed of rotation of the rotor is delivered by the second winding and compared with two

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reference voltages. In the event of voltages proportional to the speed which are higher than the two reference voltages, two substantially rectangular signals are delivered which are freed of interference pulses and, delayed by an adjustable time, are introduced as actual-frequency pulses into a regulating device for the nominal operation and there compared with desired-frequency pulses. Depending on this comparison, two different nominal-running pulses for accelerating or braking the motor respectively are delivered by the regulating device for the nominal operation. If the rotor speed drops below a preset value, a self-starting is initiated for the step-by-step or quasi-continuous increase in the rotor speed by cyclic switching over and reversal of the polarity of the driving pulses from the first to the second winding. For this purpose, driving pulses for the acceleration of the motor are produced from the interference-suppressed and delayed actual-frequency pulses and the desired-frequency pulses in that the rising edges of the driving pulses are initiated by the falling edges of the desired-frequency pulses and the falling edges of the driving pulses are initiated by the falling edges of the interference-suppressed and delayed actual-frequency pulses. If the rotor speed is too high, that is to say if the actual-frequency pulses are in advance of the desired-frequency pulses, pulses to brake the rotor are produced in that the rising edges of the braking pulses are initiated by the falling edges of the actual-frequency pulses and the falling edges of the braking pulses are initiated by the falling edges of the desired-frequency pulses.

A delay in the actual-frequency pulses is necessary in order to avoid driving or braking pulses which are dependent on the position of the desired-frequency pulses and may therefore brake in an acceleration range or accelerate in a braking range.

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When a prescribed speed is reached in self-starting operation, the self-starting operation is terminated and there is a change over to nominal running regulation with a 32 Hz regulation in which both the rising and the falling edges of the desired-frequency and actual-frequency pulses are used to initiate the driving pulses for the clock motor. This type of nominal running regulation includes a very rapid regulation since both half-waves are taken into consideration but to some extent it proves too powerful so that hunting occurs which leads to an excessive current consumption in the device. Since regulation is effected in both half-waves, corresponding driving or braking pulses are delivered to the working winding so that the voltage supply source is correspondingly heavily loaded.

A battery-operated electronic clock is known from GB-A 2 038 043 which comprises a stepping motor for the drive of a time indicating device. A driving winding of the stepping motor is provided with driving pulses from a driving circuit, the driving circuit being connected through a pulse transformer to a frequency divider connected to an oscillator for the delivery of both desired-frequency pulses and pulses of a higher frequency. The driving winding of the stepping motor is additionally connected, through a detector circuit, to a scanning-signal generating circuit which, at specific intervals of time, delivers interrupting pulses to the driving circuit to open the driving-winding connections so that the detector circuit can detect the winding voltage and generate a status control signal which is delivered to the pulse transformer. The driving power is fixed depending on the status control signal so that in the event of increased loading, for example on actuation of a calendar display, the driving power is increased. In this case, in order to monitor the stepping motor, various monitoring states are provided, each of which is initiated after the lapse of fixable

periods of time which in turn are each calculated from the beginning of a certain mode of operation of the stepping motor.

It is the object of the present invention to indicate a method and a device for the regulation of a clock motor with a permanent magnetic rotor which ensure a stable regulation with low current consumption.

According to the invention, this problem is solved, with regard to the method, in that immediately after the ending of each self-starting operation, for a fixed period of time, a first part of a nominal running regulation takes place during which the actual-frequency pulses derived from the control winding are compared more often with the desired frequency pulses than during a second part of the nominal running regulation taking place after the end of the fixable period of time. The solution according to the invention ensures that, after the end of the self-starting operation, there is at first a change-over, for a fixable period of time, to the powerful 32 Hz regulation which is, however, unstable and involves great current consumption and then, for the nominal running operation, to the weaker but more stable 16 Hz nominal running regulation involving less current consumption.

A device for carrying out the method is characterised in that a time stage for fixing the period of time of the first part of the nominal running regulation delivers a first signal to the interlock circuit and a second signal to one input of a NAND gate, the other input of which is acted upon by the one output signal of the shift register and which delivers an output signal, the output signals of the time stage, the output signal of the NAND gate and the driving pulses delivered to the working winding depending on the output signals of the shift register and of the NAND gate satisfying the following truth table:

Period of time	Signals		Decoded pulse edges f_s and i		Level Q_c	Driving pulses (Depending on $Q_A, Q_B, Q_C, I, \bar{I}$)
	E	D	rising	falling		
about 1 to 2 seconds after ending of the self- starting (t_2-t_5)	L	H	yes	yes	Dependent on gate 5	positive or negative pulses depending on $Q_B, Q_C, I, \bar{I}$
unlimited $t_5 \rightarrow \infty$	H	L	no	yes	always low	only positive pulses depending on Q_B

The ideas on which the invention is based will be explained in more detail with reference to an example of embodiment illustrated in the drawing.

Figure 1 shows a block circuit diagram of a clock motor with the whole regulating device;

Figure 2 shows a time diagram of the pulses and signals according to Figure 1;

Figure 3 shows a detailed illustration of the individual elements of the regulating circuit for regulating a clock motor with self-starting;

Figure 4 shows a time diagram of the pulses and signals appearing in the device according to Figure 3;

Figure 5 shows a detailed illustration of the elements of the regulating circuit for a clock motor with self-starting and stabilized regulation in nominal running operation and

Figure 6 shows a time diagram of the actual-frequency, desired-frequency and driving pulses of the device according to Figure 5.

In Figure 1 a block circuit diagram of the device for regulating a clock motor 2 is illustrated, which comprises a rotor 21 with permanent-magnetically formed poles and a stator, not illustrated in detail, with two windings 22 and 23. If pulses are applied to one of the two windings 22, 23, the rotor 21 can be brought to a speed of rotation corresponding to the number of pairs of poles and the frequency. The revolutions of the rotor 21 are transmitted, via a shaft and gearing, to a display system which, for example, renders possible an analogue display by means of a plurality of hands and a dial.

For the detection of the speed of rotation n and hence the actual frequency, the control winding 23 of the stator serves as a sensor winding to deliver a voltage U_n proportional to the speed for the speed regulation. This control winding 23, like the working winding 22, lies within the range of influence of the lines of flux of the poles of the rotor 21. During the rotation of the rotor 21, the lines of flux of the poles periodically intersect the sensor winding 23, as a result of which a sinusoidal voltage U_n , which is proportional to the speed of rotation n and hence to the actual frequency of the rotor 21 and which has zero-axis crossings, the so-called sensor signal, appears at the ends of the winding. This voltage U_n which is proportional to the speed is applied, together with two reference voltages U_r and U_s , to the inputs of a comparison element 4 where the sinusoidal signal tapped off at the control winding 23 is converted into two rectangular pulses for the speed regulation and for the initiation of the self-starting operation respectively. The substantially rectangular actual-frequency pulses i and the output signals v of the comparison element 4 are applied to the inputs of a following interference-suppression and delay element 51 for the output signal v or an interference-suppression element 521 for the actual-frequency pulses i . The interference-suppression

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and delay element 51 for the output signal v is acted upon by a clock frequency f_5 while a clock frequency f_1 is applied to the interference-suppression element 521 for the actual-frequency pulses i . The interference-suppressed actual-frequency pulses i are delivered both to a following phase comparator 6 and to a delay element 522.

The delay element 522 is acted upon by a third clock frequency f_3 and delivers, at its outputs, interference-suppressed and delayed actual-frequency pulses i and negated actual-frequency pulses i respectively. The interference-suppression and delay element 51, the interference-suppression element 521 and the delay element 522 for the output signal v and the actual-frequency pulses i are combined in chain-line in this example of embodiment to form a common interference-suppression and delay element 5.

In addition to the interference-suppressed actual-frequency pulses i , a second clock frequency f_2 and a desired-frequency signal f_s , necessary for the phase comparison, as well as a change-over signal β are applied to the phase comparator 6. The outputs of the delay element 522 and of the phase comparator 6 as well as the negated change-over signal $\bar{\beta}$ are connected to the inputs of a logic element 10 which delivers the braking or acceleration signals at its output to a control logic 9.

Apart from the interference-suppressed and delayed self-starting signal V , which is delivered by the interference-suppression and delay stage 51, one or more frequency signals f_{onz} , different from one another, as well as a signal N are fed into a self-starting stage 8. The signal N is generated in a waiting-time element 7 which consists of one or more delay stages and to which a fourth clock frequency f_4 is fed. The reset inputs of all delay stages of the waiting-time element 7 are reset synchronously depending on the interference-suppressed and delayed self-starting signal V , which is likewise fed in, and on the change-over signal β .

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Apart from the change-over signal $\bar{\beta}$ or the negated change-over signal β , two pulse trains F_1 or $\bar{F}_1$ and F_2 or $\bar{F}_2$ together with the output signal of the combinational logic 10 are supplied by the self-starting stage 8 to the following control logic 9, at the output of which pulse trains T_n S_n for actuating switches of a following switching stage 3 which is connected both to a voltage source $+U_B$, $-U_B$ and to the windings 22 and 23 of the clock motor 2. The switching stage 3 connects the working winding 22 of the clock motor 2 or, in self-starting operation, both the working winding 22 and the control winding 23 of the clock motor 2, to the one pole or the other of the voltage source $+U_B$ or $-U_B$.

Associated with the device is a generator which comprises an oscillating crystal 1 and a frequency divider 11, at which rectangular pulses f_n appear with the clock frequencies f_1 to f_5 and the frequencies f_{onz} and the frequency f_s for the desired-frequency signal and which are supplied at the above-mentioned points to the corresponding components of the device.

The mode of operation of this device in the range of the nominal running regulation, that is to say after the ending of self-starting operation during the usual regulating state, is explained in more detail below with reference to the time diagram of the individual signals shown in Figure 2.

The sinusoidal voltages illustrated in Figures 2a and b represent the voltages, which are electrically offset by 90° in relation to one another, at the control winding U_{23} and at the working winding U_{22} . By means of the comparison element 4, a rectangular output voltage i is produced by means of the set reference voltage U_s (Figure 2c), the correct direction of rotation of the rotor 21 and hence of the control-winding voltage U_{23} being illustrated in full lines and the direction of rotation opposite to the

correct direction of rotation being illustrated in chain line. This rectangular output signal i of the comparison element 4 is freed of interference signals by means of the interference-suppression element 521 and supplied, as pulse train i_1 to the following delay element 522, the output signal I of which is illustrated in Figure 2d. This signal is delayed by a time Δt in relation to the rising or falling edge of the actual-frequency pulse i . In Figure 2e, this signal delayed by the time Δt is illustrated as signal $\bar{I}$ for the direction of rotation opposite to the correct direction of rotation.

Figure 2f shows the rectangular desired-frequency pulses f_s , the frequency of which corresponds to the time standard of the clock. As can be seen from this time diagram, in the correct direction of rotation, the rising edge of the desired-frequency pulse f_s appears at the moment t_1 before the rising edge of the actual-frequency pulse i at the moment t_2 . In this range of time between the moments t_1 and t_2 , that is to say beginning with the rising edge of the desired-frequency pulse f_s and ending with the rising edge of the actual-frequency pulse i in the negative half-wave range and beginning with the falling edge of the desired-frequency pulse f_s and ending with the falling edge of the actual-frequency pulse i in the positive half-wave range, driving pulses are delivered to the working winding 22. These driving pulses, which are represented as pulses A and B in Figure 2g, are only given to the working winding 22, however, when, in the negative half-wave range, the delayed signal $I = \text{low}$ or, in the positive half-wave range, the delayed actual-frequency signal $I = \text{high}$. If the delayed actual-frequency signal I were to rise or fall within the range of time which lies between the rising or falling edges of the desired-frequency pulse f_s and of the actual-frequency pulse i , the driving pulse A or B would fall accordingly with the rising or falling edge of the delayed actual-frequency signal I .

If the actual-frequency pulse 1 is in advance of the desired-frequency pulse f_s , that is to say, if the rising edge of the actual-frequency pulse 1 appears at the moment t_3 before the rising edge of the desired-frequency pulse f_s at the moment t_4 , the rotor 21 of the clock motor 2 is braked by short-circuiting the working winding 22. This short-circuiting of the working winding 22 is initiated by the rising edge of the actual-frequency pulse 1 and ends with the rising edge of the desired-frequency pulse f_s (range C) and/or with the falling edge of the actual-frequency pulse 1 and the falling edge of the desired-frequency pulse f_s (range D).

The detailed illustration of the regulating circuit to be seen from Figure 3 shows the elements illustrated in Figure 1 surrounded by chain lines.

The comparison element 4 contains two comparators C1 and C2, the positive inputs of which are connected to the one end of the control winding 23. Whereas the negative input of the first comparator C1 is connected to the one reference voltage U_s , the negative input of the second comparator C2 is connected to the other reference voltage U_r and to the other end of the control winding 23. The reference voltages U_r and U_s respectively are taken off at a resistance divider with the resistors R1 to R3. The outputs of the two comparators C1 and C2 with the output signals v and i are fed separately to the one interference-suppression and delay stage 51 and to the interference-suppression stage 521 respectively. The interference-suppression and delay stage 51 contains 4 clocked flip-flops D1 to D4 which are connected in series, the clock inputs C_k of which are acted upon synchronously by a fixable fifth clock frequency f_5 , in this case a frequency of 256 Hz, and of which only the first and fourth flip-flops D1 and D4 are shown for the purpose of better illustration.

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The input of the first clocked flip-flop D1 is connected to the output of the first comparator C1. The outputs Q of the clocked flip-flop are each connected to the input of the following clocked flip-flop. The output of the fourth flip-flop D4 is applied to the input of a following first NAND gate G24 to the other input of which there is connected the output of the first clocked flip-flop D1. The negated outputs $\bar{Q}$ of the first and fourth clocked flip-flops D1 and D4 respectively are connected to the inputs of a second NAND gate G26.

The suppression element 521 contains three clocked flip-flops D5-D7 which are connected in series and the clock inputs C_k of which are acted upon synchronously by a first clock frequency f_1 , in this case a frequency of 1024 Hz. As with the interference-suppression and delay stage 51, the input of the first clocked flip-flop D5 is connected to the output of the second comparator C2 and hence to the actual-frequency pulses i . The outputs Q of the clocked flip-flops D5 and D6 are each connected to the input of the following clocked flip-flop D6 or D7 respectively. The output of the last flip-flop D7 is applied to the input of a following first NAND gate G28, to the other input of which there is connected the output of the first clocked flip-flop D5. The negated outputs $\bar{Q}$ of the first and last clocked flip-flops D5 and D7 are connected to the inputs of a second NAND gate G30.

The delay element 522 for producing the interference-suppressed and delayed actual-frequency pulses I from the interference-suppressed actual-frequency pulses i_1 is similar in construction to the interference-suppression and delay stage 51 and contains the clocked flip-flops D8-D11, the clock inputs C_k of which are acted upon synchronously by a third clock frequency f_3 , in this case a frequency of 256 Hz. The following arrangement is common to all three elements 51, 521 and 522: The outputs of the

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two first NAND gates G24, G26; G28, G30 are applied to the input of a third and fourth NAND Gate G25, G27; G29, G31 respectively, the other input of each of which is connected to the output of the particular other NAND gate G25 or G27, G29 or G31 respectively. The output signal V of the interference-suppression and delay stage 51, which is identical with the output signal of the NAND gate G25, is connected to the input of the following self-starting stage 8. The interference-suppressed actual-frequency pulses i_1 , which are identical with the output signal of the NAND gate G29 are connected - as already described - both to the input of the phase comparator 6 and to the input of the delay stage 522.

The phase comparator 6 contains two clocked flip-flops D14, D15, the clock inputs C_k of which are acted upon by a second clock frequency f_2 of 4096 Hz. The input of the first clocked flip-flop D14 is acted upon by desired-frequency pulses f_s of 16 Hz for example while the interference-suppressed actual-frequency pulses i_1 are applied to the input of the second clocked flip-flop D15. The outputs Q of the two clocked flip-flops D14 and D15 are each applied to the one input of a following exclusive-OR gate G39 and G40, the other inputs of which are acted upon by the desired-frequency pulses f_s and by the interference-suppressed actual-frequency pulses i_1 respectively.

The outputs of the two exclusive-OR gates G39 and G40 are each connected to the one input of a following NAND gate G41 or G42 respectively and through an inverter G43 or G44 respectively to the other input of the particular other NAND gate G42 or G41 respectively. The outputs of these two NAND gates G41 and G42 are fed, together with the second clock frequency f_2 , supplied through an inverter G45, and the change-over signal β to the phase comparator 6 comprising six J/K flip-flops J1 to J6, as well as ten OR gates G70 to G79 and two further inverters G80 and G81.

The change-over signal β is applied to the set inputs S of the J/K flip-flops J1 to J6 while the clock inputs C_k of the flip-flops J1 to J6 are connected to the inverted clock frequency f_2 . The J input of the first J/K flip-flop J1 is connected to the output of the one inverter G81 and the J inputs of the second to the sixth J/K flip-flops J2 to J6 are connected to the outputs of the OR gates G74 to G70.

The K inputs of the first five J/K flip-flops J1 to J5 are connected to the outputs of further OR gates G79 to G75 and the K input of the sixth J/K flip-flop J6 is connected to the output of the further inverter G80. Whereas the one input of the OR gates G70 to G74, connected to the J inputs at the output side, and the input of the one inverter G81 are connected to the output of the first NAND gate G41, the one inputs of the OR gates G75 to G79, connected to the K inputs, and the input of the further inverter G80 are connected to the output of the second NAND gate G42. The further input of the OR gates G70 to G74, connected to the J inputs of the J/K flip-flops, is connected to the negated output $\bar{Q}$ of the particular preceding J/K flip-flop J1 to J5. The further inputs of the OR gates G75 to G79, connected to the K inputs of the J/K flip-flops J1 to J5, are connected to the output Q of the particular following J/K flip-flop J2 to J6.

From the outputs Q of the third, fourth 35 and fifth J/K flip-flops J3 to J5, the corresponding braking or driving pulses Q_A , Q_B and Q_C respectively are delivered to the following combinational logic 10.

By means of the eight NAND gates of the combinational logic 10, the output signals I, $\bar{I}$ as well as Q_A , Q_B and Q_C of the delay stage 522 or of the phase comparator 6 as well as the negated change-over signal $\bar{\beta}$ are combined with the outputs of the particular preceding NAND gate in the following manner:

- a) Gate G52: signal I and Q_C
- b) Gate G56: signal Q_B and I
- c) Gate G53: output signal of the gate G52 and signal Q_A
- d) Gate G57: output signal of the gate G56 and signal Q_A
- e) Gate G60: change-over signal β , signal I and signal Q_C
- f) Gate G54: output signal of the gate G53 and change-over signal $\bar{\beta}$
- g) Gate G61: change-over signal $\bar{\beta}$, signal Q_B and I
- h) Gate G58: output signal of the gate G57 and change-over signal $\bar{\beta}$.

Apart from the interference-suppressed and delayed self-starting signal V , which is delivered by the interference-suppression and delay stage 51, only a single further frequency signal, namely the clock signal of the waiting-time element 7, is fed into the self-starting stage 8. The reset inputs of the two delay stages TR1 and TR2 of the waiting-time element 7 and of the T flip-flops TR3 to TR5 of the self-starting stage 8 are reset synchronously depending on the interference-suppressed and delayed self-starting signal V , likewise fed in, and the change-over signal β which is delivered by the self-starting stage 8.

In this example of embodiment, the self-starting stage 8 consists of three T flip-flops TR3 to TR5, the inputs of which are acted upon by the output Q of the preceding flip-flop and by the output signal of the waiting-time element 7 composed of two T flip-flops TR1 and TR2. The output of the last T flip-flop TR5 is applied, together with the desired-frequency pulses $f_s = 16 \text{ Hz}$, to a NAND gate G90, the output signal of which is applied, together with the output signal of the third T flip-flop TR5, to the input of a trigger stage which consists of two NAND gates G14, G15 connected to one another in known manner. The change-over signal β or the negated change-over signal $\bar{\beta}$ appears at the output of this trigger stage. The reset

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signal for the T flip-flops TR1, TR2 and TR3 to TR5 respectively of the waiting-time element 7 and of the self-starting stage 6 are delivered from the output of a NAND gate G34, to the one input of which the change-over signal β is applied and the other input of which is connected to the output of a NAND gate G33. One input of the NAND gate G33 is connected to the output of a further NAND gate G32 while the interference-suppressed and delayed self-starting signal V is applied to the other input of the NAND gate G33. The two inputs of the NAND gate G32 are connected, on the one hand to the negated output $\bar{Q}$ of the second T flip-flop TR2 of the waiting-time element 7 and on the other hand to the negated output signal $\bar{Q}$ of the second T flip-flop TR4. In this example of embodiment, the outputs Q and $\bar{Q}$ of the two T flip-flops TR1 and TR2 of the waiting-time element 7, which reduce the clock frequency fed in from 16 Hz for example to 8 Hz and 4 Hz respectively by division and so preset the frequency signals F_1 , $\bar{F}_1$, F_2 , $\bar{F}_2$, serve to preset various frequency signals.

The output signals of the self-starting stage 8 and the output signals of the logic stage 10 are combined with one another in the following control logic 9 in such a manner that they satisfy the following truth table for the control of the switches S1-S8 of the switching element 3:

Control signals						FET switches							
β	Q_C	Q_B	Q_A	I	$\bar{I}$	S1	S2	S3	S4	S5	S6	S7	S8
H	L	L	H	X	X	OFF	OFF	OFF	OFF	OFF	OFF	OFF	OFF
H	L	L	L	X	X			OFF	OFF			ON	ON
H	L	L	H	X	X			OFF	OFF			OFF	OFF
H	L	H	H	H	L			ON	OFF			ON	OFF
H	L	H	H	L	H			OFF	OFF			OFF	OFF
H	H	H	H	H	L			ON	OFF			ON	OFF
H	H	H	H	L	H	OFF	OFF	OFF	ON	OFF	OFF	OFF	ON

The mode of operation of the arrangement shown in Figure 3 will be explained in more detail in connection with the time diagram of the signals shown in Figure 4. In Figure 4, the following signals are illustrated from the top downwards:

- a) the self-starting signal V,
- b) the 16 Hz clock frequency for the waiting-time element,
- c) the reset signal for resetting the T-flip-flops of the self-starting stage and of the waiting-time element,
- d) the output signals of the T flip-flops of the self-starting stage and of the waiting-time element,
- e) the output signal Q of the waiting-time element,
- f) the output signal γ of the NAND element G90,
- g) the change-over signal β and
- h) the voltage at the windings 22 and 23 of the clock motor 2.

If the speed of rotation of the rotor 21 of the motor 2 drops below a specific value so that the output signal V no longer comes to high potential for a certain period of time, the common reset input R of the T flip-flops TR1 to TR5 of the waiting-time element 7 and of the self-starting stage 8 remains at low potential during this period of time. In this case, it is presupposed that the change-over signal β was in the state of low potential during the preceding regulation operation and at least the output signal Q of the third T flip-flop TR5, negated output signal $\bar{Q}$ of the second T flip-flop TR4 of the self-starting stage 8 was in the state of high potential. During the whole range of time here under consideration, the output signal V is in the state of low potential, for example because the rotor 21 of the motor 2 is no longer moving. With the falling self-starting signal V, the reset signal also disappears at the moment t_0 (Figure 4c). Thus the T flip-flops TR1 to TR5 are made active and reduce the clock frequency fed in of 16 Hz for example (Figure 4b) in accordance with the illustration in Figure 4d which

represents the negated outputs of the T flip-flops TR1 to TR4 and the output signal Q of the fifth T-slip-flop TR5 respectively. So long as the output signal Q of the fifth T flip-flop TR5 is at high potential, a signal γ corresponding to the clock frequency appears at the output of the gate G90. If the self-starting signal V remains at high potential for a certain period of time, the flip-flop G91 is set so that the change-over signal β is set in the state H at the moment t_1 and the negated change-over signal $\bar{\beta}$ is set in the state L. After the change-over signal β has been set in the state H and so long as the change-over signal β remains in this state, a resetting of the T flip-flops TR1 to TR5 is prevented since the reset signal for the five T flip-flops TR1 to TR5 remains in the state L because $\beta = H$. So long as the change-over signal β remains in the state H, the self-starting operation persists on the principle of a stepping motor with two windings. During this time, the two windings 22 and 23 of the clock motor 2 are acted upon by frequency signals as shown in Figure 4h which are composed, by means of the control logic, from the frequencies delivered by the first and second T flip-flops TR1 and TR2 at their outputs Q or negated outputs $\bar{Q}$ respectively. This takes place in such a manner that the switching table given above for the switches S1 to S8 is complied with. The result of this switching-on logic for the switches S1 to S8 in the range of time from the moment t_1 - t_2 is the pulse train represented in Figure 4h for the windings 22 and 23.

If the output signal Q of the fifth T flip-flop TR5 is set in the state L, then after the expiration of a further clock pulse of the frequency signal of 16 Hz for example fed in, the flip-flop G91 is set to L by the change-over signal $\bar{\beta}$ and to H by the negated change-over signal β , which means a change of the previous self-starting operation

into the nominal running operation at the moment t_2 . With this method of pulse combination, the effect is achieved that the last self-starting pulse has half the width, corresponding to the clock frequency fed in, in comparison with the preceding self-starting pulses. At the moment t_3 , a signal as shown in Figure 4e is delivered by the second T flip-flop TR2 at the negated output and leads to the reset pulse shown in Figure 4c, the falling edge of which appears at the moment t_4 . Thus the self-starting operation is terminated and during the following nominal running operation, the second winding 23 of the clock motor 2 serves as a control winding, the output signals of which lead to the signals V and I, as described above.

The detailed circuit diagram illustrated in Figure 5 elucidates the method according to the invention and the device according to the invention for regulating a clock motor and largely corresponds to the device shown in Figure 3 so that a more detailed explanation of the operation and individual elements of this device will be dispensed with. The reference numerals used in Figure 5 correspond to the reference numerals used in Figure 3 to designate like components.

In comparison with the device shown in Figure 3, however, an additional time stage 12 is provided as well as a modified interlock circuit 61 in the phase comparator 6. In addition, the control signal Q_C is formed by combining the output signal Q_5 of the shift register 62 with the output signal E of the time stage 12.

The further blocks as well as the elements of the device according to Figure 5 contained therein correspond identically to the blocks and elements contained therein of the control and regulating device according to Figure 3.

The time stage 12 contains two T flip-flops 121, 122, the reset inputs of which are acted upon by the change-over signal β for changing over from self-starting operation to the nominal running operation composed of a first and

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second portion. A frequency signal of 1 Hz is applied to the T input of the first T flip-flop 121 of the time stage 12 while the output Q of the first T flip-flop 121 is connected to the one input of a NAND gate 123, the other input of which is acted upon by the output Q of the second T flip-flop 122. The output of the NAND gate 123 is connected to the input of the second T flip-flop 122 while the Q output of the second T flip-flop 122 delivers the signal E and the $\bar{Q}$ output of the second T flip-flop 122 delivers the signal D. The negated output signal of the second T flip-flop 122 or of the time stage 12 is delivered to the interlock circuit 61 while the output signal Q, as signal E, is delivered to the one input of a NAND gate G50, the other input of which is acted upon by the output signal Q_5 of the shift register 62. The output signal γ of this NAND gate G50 supplies the control signal Q_C .

The interlock circuit 61 of the phase comparator 6 is connected to the outputs of the two D flip-flops D14 and D15 as well as to the D output signal of the time stage 12 and to the 16 Hz desired-frequency pulses f_s and the output of the interference-suppression and delay element 5. The interlock circuit 61 contains four AND gates G10 to G13, the outputs of which are each connected in pairs to the inputs of two following NOR gates G14 and G15. The outputs of the two NOR gates G14 and G15 are each connected, through a negation element G16 or G17, to the one input of a following NAND gate G18 and G19 in each case. In addition, the outputs of the two NOR gates G14 and G15 are connected crosswise to the second input of the NAND gates G18 and G19, in each case. As in the arrangement according to Figure 3, the outputs of the two NAND gates G18 and G19 are connected to the inputs of the shift register 62.

The inputs of the four AND gates G10 to G13 of the interlock circuit 61 are acted upon in the following

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manner: The inputs of the first AND gate G10 are connected both to the 16 Hz desired-frequency pulses f_s and to the Q output of the D flip-flop D14.

The 16 Hz desired-frequency pulses f_s , the negated output signal $\bar{Q}$ of the D flip-flop D14 and the D output signal of the time stage 12 are applied to the inputs of the second AND gate G11. The negated output signal $\bar{I}_1$ of the interference-suppression and delay stage and the Q output signal of the D flip-flop D15 are applied to the inputs of the third AND gate G12.

Finally, the output signal i_1 of the interference-suppression and delay stage 5, the negated output signal $\bar{Q}$ of the D flip-flop D15 and the D output signal of the time stage 12 are applied to the inputs of the fourth AND gate G13.

The mode of operation of the arrangement shown in Figure 5 will be explained in more detail below with reference to the time diagram shown in Figure 6.

In Figure 6, the actual-frequency pulse signal i , the desired-frequency pulse signal f_s and the control signal delivered to the working winding of the clock motor are illustrated in time diagrams from the top downwards.

After the expiration of the self-starting operation at the moment t_2 , that is to say when the change-over signal β assumes low potential, a period of time of 1 to 2 seconds elapses during which the output signals of the time stage 12 change over in such a manner that the output signal E goes to high potential and the output signal ν to low potential. Within this period of time, the first portion of the nominal running regulation proceeds with a 32 Hz clock pulse according to the illustration in Figure 4 in connection with the arrangement according to Figure 3 or Figure 5. After the expiration of this period of time, that is to say at the moment t_5 , with the beginning of the second portion of the nominal running regulation and with

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high potential of the output signal E and low potential of the signal D of the time stage 12, only the falling edges of the actual-frequency pulses i_1 and of the desired-frequency pulses f_s respectively are decoded in the D flip-flops D14 and D15 and in the interlock circuit 61 of the phase comparator 6 and are passed on to the shift register 62. The consequence of this is that the output signal Q_C of the NOR gate G50 remains at low potential and only positive pulses are delivered to the working winding 22 of the clock motor 2. These pulses are superimposed on the sinusoidal voltage induced in the working winding 22, during its positive half-waves, delivered to the working winding 22 as driving pulses with the falling edges of the desired-frequency pulses f_s and the falling edges of the actual-frequency pulses i at the moments t_6 and t_7 or, if the actual-frequency pulses i are in advance in relation to the desired-frequency pulses f_s , they are delivered to the working winding 22 as braking pulses in a manner not illustrated. The combination of the individual pulses of the time stage 12, of the interlock circuit 61 and of the control signal Q_C is effected in accordance with the following truth table:

Period of time	Signals		Decoded pulse edges f_s and i		Level Q_C	Driving pulses (depending on $Q_A, Q_B, Q_C, I, \bar{I}$)
	E	D	ris- ing	fall- ing		
about 1 to 2 seconds after end of the self-starting (t_2-t_5)	L	H	yes	yes	depend- ent on gate 5	positive or negative pulses depending on $Q_B, Q_C, I, \bar{I}$
unlimited $t_5 \rightarrow \infty$	H	L	no	yes	always low	only positive pulses depending on Q_B