CLAIMS

1. An electronic circuit configured to present a high-impedance load between a load point and a reference point, the electronic circuit including:

a capacitive element (C) provided between a first node (Node A) and the reference point;

a first element having a non-linear voltage-to-current relationship (D_1) connected in parallel with the capacitive element (C) between the first node (A) and the reference point;

a first switching element (S_1) provided in series between the first node (A) and a voltage source point;

a second switching element (S_2) provided between the first node (A) and a second node (Node B); and

a second element having a non-linear voltage-to-current relationship (D_2) connected between the second switching element (S_2), the load point, and the reference point; and

timing control logic configured to control the first switching element (S_1) and the second switching element (S_2) to bias the second element (D_2) to operate in at least three stages comprising:

a charging stage wherein the first switching element (S_1) is closed and the second switching element (S_2) is open for a charging duration (T_{CH}) to enable the capacitive element (C) to charge a nodal voltage $v_D(t)$ at the first node (A) to a pre-defined initial voltage threshold V_i;

a discharge stage wherein the first switching element (S_1) is open and the second switching element (S_2) is open for a discharge duration (T_{DCH}) to enable discharging of the capacitive element (C) through the first element (D_1) such that a current through the first element (D_1) reaches a pre-defined bias current (I_{BIAS}) and/or the nodal voltage $v_D(t=T_{CH}+T_{DCH})$ equals a pre-defined bias voltage (V_{BIAS}); and

a transfer stage in which the first switching element (S_1) is open and the second switching element (S_2) is closed for a transfer duration (T_{XFR}) to connect the first node (A) and the second node (B), thereby to apply or transfer the bias voltage (V_{BIAS}) to a contact of the second element (D_2) connected to the second node (B) to bias the second element (D_2) according to the bias voltage (V_{BIAS});

wherein the timing control logic is configured to open the second switching element (S_2) after the transfer stage, the second element (D_2) being biased to present the high-impedance load between the load point and the reference point.

2. The electronic circuit as claimed in claim 1, in which the first element (D_1) is a diode-connected transistor and the second element (D_2) is a transistor.

3. The electronic circuit as claimed in claim 1, in which:

the first and second elements (D_1, D_2) are MOSFETs (Metal-Oxide-Semiconductor Field-Effect Transistors);

the first and second elements (D_1, D_2) are BJTs (Bipolar Junction Transistors);

the first element (D_1) is a BJT and the second element (D_2) is a MOSFET; or

the first element (D_1) is a diode and the second element (D_2) is a BJT.

4. The electronic circuit as claimed in any one of claims 1-3, in which the first and second elements (D_1, D_2) have proportional voltage-current relationships.

5. The electronic circuit as claimed in any one of claims 1-4, in which the transfer duration T_{XFR} is calculated to transfer the voltage $V_D(t)$ between the first node (A) and the second node (B) using the second switching element (S_2) and to keep the capacitive element (C) charged to ensure that the bias point voltage on the second node (B) of the second element (D_2) remains above ground potential (0 V).

6. The electronic circuit as claimed in any one of claims 1-5, in which the timing control logic is configured to repeat the charging stage, discharging stage, and transfer stage periodically or intermittently.

7. The electronic circuit as claimed in claim 6, in which the timing control logic is configured to repeat the charging stage, discharging stage and transfer stage at a frequency depending on a load voltage v_L.

8. The electronic circuit as claimed in claim 7, in which the timing control logic is configured to keep a ratio v_L/i_L constant in order to establish a constant real impedance, wherein i_L is a load current bias point.

9. The electronic circuit as claimed in any one of claims 1-8, which is, or which forms part of, an Integrated Circuit (IC).

10. A method of generating a high-impedance load between a load point and a reference point, the method comprising:

providing an electronic circuit including:

a capacitive element (C) provided between a first node (Node A) and the reference point;

a first element having a non-linear voltage-to-current relationship (D_1) connected in parallel with the capacitive element (C) between the first node (A) and the reference point;

a first switching element (S_1) provided in series between the first node (A) and a voltage source point;

a second switching element (S_2) provided between the first node (A) and a second node (Node B); and

a second element having a non-linear voltage-to-current relationship (D_2) connected between the second switching element (S_2), the load point, and the reference point; and

timing control logic configured to actuate the first switching element (S_1) and the second switching element (S_2) to bias the second element (D_2) in at least three stages,

the method further comprising:

charging the capacitive element (C), during a charging stage wherein the first switching element (S_1) is closed and the second switching element (S_2) is open for a charging duration (T_{CH}), to a nodal voltage $v_D(t)$ at the first node (A) to a pre-defined initial voltage threshold V_i;

discharging the capacitive element (C), during a discharge stage wherein the first switching element (S_1) is open and the second switching element (S_2) is open for a discharge duration (T_{DCH}), through the first element (D_1) such that a current through the first element (D_1) reaches a pre-defined bias current (I_{BIAS}) and/or the nodal voltage $v_D(t=T_{CH}+T_{DCH})$ equals a pre-defined bias voltage (V_{BIAS});

transferring the bias voltage (V_{BIAS}), during a transfer stage in which the first switching element (S_1) is open and the second switching element (S_2) is closed for a transfer duration (T_{XFR}) to connect the first node (A) and the second node (B), to a contact of the second element (D_2) connected to the second node (B) to bias the second element (D_2) according to the bias voltage (V_{BIAS}); and

opening the second switching element (S_2) after the transfer stage, the second element (D_2) being biased to present the high-impedance load between the load point and the reference point.

11. The method as claimed in claim 10, in which the charging stage, discharging stage, and transfer stage are repeated periodically or intermittently.

12. The method as claimed in claim 11, in which the charging stage, discharging stage, and transfer stage are repeated at a frequency depending on a load voltage v_L.

13. The method as claimed in claim 12, which includes keeping a ratio v_L/i_L constant in order to establish a constant real impedance, wherein i_L is a load current bias point.