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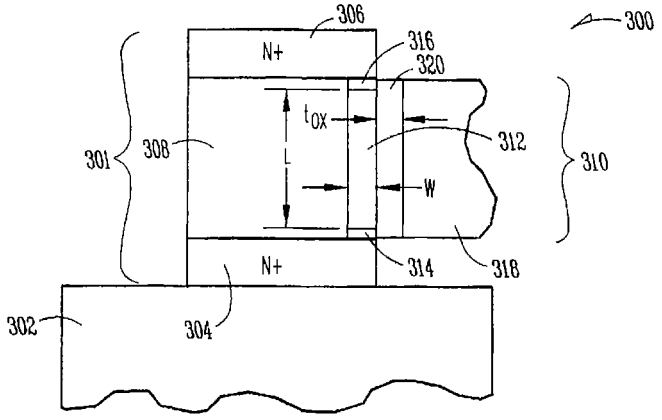
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(54) Title: FOLDED BIT LINE DRAM WITH VERTICAL ULTRA THIN BODY TRANSISTORS

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(57) Abstract: A folded bit line DRAM device is provided. The folded bit line DRAM device includes an array of memory cells. Each memory cell in the array of memory cells includes a pillar extending outwardly from a semiconductor substrate. Each pillar includes a single crystalline first contact layer and a single crystallne second contact layer separated by an oxide layer. A single crystalline vertical transistor is formed along alternating sides of the pillar within a row of pillars. The single crystalline vertical transistor includes an ultra thin single crystalline vertical first source/drain region coupled to the first contact layer, an ultra thin single crystalline vertical second source/drain region coupled to the second contact layer, and an ultra thin single crystalline vertical body region which opposes the oxide layer and couples the first and the second source/drain regions. A plurality of buried bit lines are formed of single crystalline semiconductor material and disposed below the pillars in the array memory cells for interconnecting with the first contact layer of column adjacent pillars in the array of memory cells. Further, a plurality of word lines are included. Each word line is disposed orthogonally to the plurality of buried bit lines in a trench between rows of th epillars for addressing laternating body regions of the single crystalline vertical transistors that are adjacent to the trench.

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