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(54) IMPROVEMENTS IN OR RELATING TO MEMORY DEVICES

(71) We, WESTERN ELECTRIC COMPANY, INCORPORATED, of 195, Broadway, New York City, New York State, United States of America, a Corporation organised and existing under the laws of the State of New York, United States of America, do hereby declare the invention for which we pray that a patent may be granted to us, and the method by which it is to be performed, to be particularly described in and by the following statement:—

This invention relates to memory devices. As computers become more and more sophisticated there is a tendency for their memories to increase in complexity. Thus, it is not surprising to find that each additional function that a computer is called upon to perform adds substantial cost to the machine. This added cost is offset in part by arranging the computer so that the memory is always performing some function. Accordingly, it has become standard practice to separate certain functions from the basic machine and to perform these functions in an autonomous manner, and thus buffer the central memory from routine "scratch pad" type of operations.

Such autonomous "scratch pad" memories are usually arranged to perform a number of routine and repetitive operations, such as locating certain bits of information previously stored therein or storing other bits therein. Thus, a primary factor in considering a buffer memory arrangement is the initial apparatus cost as well as the operation costs.

Another important consideration regarding buffer memories is that when communication is necessary with the central memory, such as when the buffer memory reports a certain change to the central memory, such communication takes place only at the option of the central memory. Thus, in situations where the central memory is busy processing other data,

the buffer memory must have the capability of communicating its information at some later time. In addition, the buffer memory should be arranged so that it can be shut down and restarted without a loss of stored data. This is especially important in situations where the "scratch pad" memory is only active for certain fixed periods, but must compare data received over long intervals.

Previously, memories which have been arranged as buffer memories usually have storage capability and thus inherently require some form of address retrieval system. Those autonomous "scratch pad" memories which do not require address information do not usually have a storage capability, and thus are arranged to force the central processor to accept updating information randomly and under exclusive control of the buffer memory.

According to this invention a memory device in which data bits can be represented by physical manifestations which exert a mutual influence on each other when they are proximate each other includes a first channel for carrying a sequence of data bits, a second channel for carrying a sequence of interrogation bits into proximity with said data bits, means for providing a said interrogation bit for each said data bit, means for synchronously moving said data bits and said interrogation bits along their respective channels, and means for providing an output signal dependent upon the mutual influence, if any, between each said data bit and its corresponding interrogation bit when they are proximate each other.

The said channels may be defined in a sheet of material in which single wall magnetic domains can be moved, and said means for moving may include a magnetically soft overlay adjacent a surface of said sheet, said data bits and said interrogation both comprising the presence and absence, as appro-

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appropriate, of single wall domains in said material. The means for providing an output signal may include first means operative in response to the presence of an interrogation bit domain and the absence of a corresponding data bit domain for providing a first signal, and second means operative in response to the absence of an interrogation bit domain and the presence of a corresponding data bit domain for providing a second signal. The means for providing an output signal may be operative in response to the presence of an interrogation bit domain and a corresponding data bit domain for inhibiting provision of said first and second signals.

A device in accordance with the invention may include means for providing substitution bits concurrently with said interrogation bits, and means for substituting each substitution bit in the place of the data bit corresponding thereto. There may be included means for selectively inhibiting substitution of said substitution bits. The selective inhibiting means may include means for providing auxiliary bits each corresponding with a respective one of said interrogation bits, means for comparing corresponding ones of said auxiliary and substitution bits, and means responsive to a predetermined comparison between a said auxiliary bit and its corresponding substitution bit for extinguishing the compared substitution bit.

A device in accordance with the invention may be adapted to provide signals representative of changes in detected line conditions of a plurality of telephone stations, said data bits being representative of the detected line conditions of each of said stations, and said means for providing interrogation bits being adapted to provide interrogation bits representative of subsequently detected line conditions of each of said stations. The device may include a plurality of closed loop channels for carrying data bits, and a loop readout means in each said closed loop channel for providing an output signal representative of the data bit at said readout means, said means for moving being adapted to move all said data bits around their respective closed loop channels in synchronism.

In another device in accordance with the invention the said channels may be defined in a sheet of material in which single wall magnetic domains can be moved, and said means for moving may include a magnetically soft overlay adjacent a surface of said sheet, said overlay defining said first channel and being for moving single wall domains therealong in response to a magnetic field the direction of which in the plane of said sheet changes, said overlay being such that said first channel folds back upon itself forming first, second, and third sections in such manner that said second section provides a

domain to said third section only when a domain is present in like stages of said first and second sections, said data bits and said interrogation bits comprising the presence and absence, as appropriate, of single wall domains in said material. The first and second sections may have the same number of stages. The overlay may also define a further channel like said first channel for synchronous operation therewith in response to said magnetic field. The device may be adapted to provide in the first section of each of said first and further channels first and second complementary domain patterns representative of the presence and absence of signals on a plurality of scanned lines.

The device may include first and second domain extinguishers at the end of said second sections of said first and further channels respectively. The third sections of said first and further channels may each include an output position, and said overlay may define adjacent each said output position a respective said second channel in the form of a closed loop each said second channel having the same number of stages as said number for recirculating single wall domains in response to said magnetic field, and may further define a compressor register including a first stage of each of said second channels for transferring a domain between said second channels. The overlay at the end of each of said third sections may be such as to move a domain to a domain extinguisher in the absence of a domain in the first stage of the respective second channel, and to move a domain in said third section to the corresponding output position in the presence of a domain in that first stage.

The invention will now be described by way of example with reference to the accompanying drawing, in which:

FIG. 1 is a schematic diagram showing one embodiment of the invention;

FIG. 1A is a schematic representative of a magnetic domain overlay pattern;

FIGS. 2 to 12 are schematic representations showing in greater detail the interreaction points between the shift registers;

FIG. 13 is a schematic diagram of another embodiment of the invention;

FIGS. 14, 15 and 16 are schematic representations of portions of embodiment of FIG. 13 showing magnetic overlay patterns for defining various functional areas therein; and

FIG. 17 is a block diagram of the flow of information in the embodiment of FIG. 13.

The embodiments now to be specifically described utilise the single wall magnetic domain principle.

A single wall domain is a magnetic domain encompassed by a domain wall which closes on itself in the plane of the medium in which

it moves. Such a domain is a stable, self-contained entity moveable in the plane of the medium in response to offset attracting magnetic fields.

5 Magnetic fields for moving domains may be provided by an array of conductors pulsed individually by external drivers. The shape of the conductors is dictated by the shape of the domain and by the material parameters. 10 Most materials suitable for the movement of single wall domains exhibit a preferred direction of magnetization normal to the plane of movement and are magnetically isotropic in the plane. Conductors suitable for domain movement in such materials are shaped as conductor loops providing magnetic fields in first and second directions along an axis also normal to the plane. By pulsing a succession of conductors of the array consecutively offset 20 from the position of a domain, domain movement results. In practice, the conductors are interconnected serially in three sets to provide a familiar three-phase shift register operation, e.g. as disclosed in U.K. Patent No. 1187632. 25

An alternative propagation technique involves the generation of a magnetic field of variable direction in the plane of movement of domains. Such a technique employs 30 an overlay of magnetically soft elements oriented with respect to one another to respond to such a field to generate changing magnetic pole patterns which attract domains to consecutive positions in a propagation channel.

35 The latter propagation technique is particularly useful for large capacity sequential memories because no electrical conductors are necessary except where a peculiar function is to be implemented locally. Advantage may be taken of the geometry of the magnetic overlay to achieve certain functions without conductors. For example, a domain generator which avoids the necessity for electrical conductors is described in U.K. Patent No. 1257857. U.S. Patent No. 3623034 describes a multistage shift register channel defined by overlay elements which circulate a domain locally at each stage unless a next subsequent domain is present, in which case, the circulating domain is advanced one stage due to domain interaction. When the entire channel is filled, a subsequent domain causes a domain to be expelled from the opposite end of the channel (much as an impact against the first 55 of a line of touching billard balls causes the last of the line to move). When operating in this mode, a register is called a "compressor".

Another advantage of this propagation technique is that all domain movement is caused by the pole patterns generated by the in-plane field, and, therefore, all movement is synchronous.

It will be noted that in FIGS. 2 to 12 65 a systematic designation has been employed

to illustrate the movement of domains from position to position. Thus, a domain which is in a certain position at an arbitrary starting time is shown as a solid circle. As this domain moves from position to position along a defined channel in response to a continuously changing magnetic field, broken circles are used for illustration. The letter associated with a position, such as letter "M" in FIG. 2, serves to identify the position and to identify any domain thereat. The number associated with each such letter at a specific position represents the number of that position, counting from the arbitrary selected starting position. Thus, corresponding numbers between domains in separate channels having coordinated starting positions indicate synchronous positions between the channels. The prime sign, ', is used to denote an alternative position for a domain in the associated time slot. Thus, position S3 is the position in which a domain will be three positions after a starting position S1 if no force, other than the force of the rotating magnetic field, is applied thereto. When the domain encounters some other force, such as the repulsive force of another domain, instead of moving from position S2 to position S3 it moves to the alternative position S3'. The manner in which domains are propagated along a channel will be discussed more fully later. 70 75 80 85 90 95

Referring now to FIG. 1, a buffer memory 17 is arranged with a number of individual memory loops, such as memory loop ML1, to provide status change signals to a central processor 10 which is arranged in any well-known manner to control communications between a number of telephone stations (not shown). Control data between the processor 10 and the stations via data links L1 to Ln. 100 105

The buffer memory device 17 is a magnetic domain arrangement comprising a slice of material in which magnetic domains are moveable in response to a rotating magnetic field generated by an in-plane field source 15, in a manner as fully described in U.K. Patent No. 1241235. 110

A magnetically soft overlay is juxtaposed with the domain propagation slice to provide magnetic points which attract the domains. The magnetic points define the path or channel which is followed by a domain in response to the rotating magnetic field. One such type of overlay, commonly referred to as a T and Bar overlay, is described in the above-mentioned copending application. The geometry of the overlay is constructed in such a manner that different points of the overlay become magnetically attractive to the domains during each of the four quadrants of the magnetic field rotation. 115 120 125

The overlay illustrated only schematically in FIG. 1 and FIG. 1A contains a number of separate channels or shift registers, 130

such as memory loop ML1 and interrogation channel SL1, constructed such that a domain in a given position in one shift register channel will magnetically interact with a domain in a certain coordinated position in another shift register channel. Interreaction between domains is utilized to control the device and to provide output and storage without external control in a manner to be described.

All the domains in such a device are propagated synchronously in response to the same reorienting magnetic field. Thus, the overlay may be constructed in such a manner that domains which are propagated along different paths will arrive at certain points of the overlay in a predetermined coordinated relationship.

This physical control of magnetic domains in spatial coordination coupled with the interreaction forces generated when two domains are in close relationship with each other permit consecutive logic operations to be performed between corresponding representations of different sets of information representations. If, for example, a circuit is to supply a first or a second signal indicative of the status of each of a set of lines, domain patterns representative of the signals last supplied by such a circuit can be organized to interact directly with a domain pattern representative of update information for those lines to determine the signals next supplied by the circuit. In one such operation, a domain shift register operates as a sequential memory for storing domain patterns of control signals least supplied for direct interreaction and thus updating in accordance with domain patterns representative of changed conditions in the lines.

In FIG. 1 the processor is arranged to scan each data link sequentially thereby obtaining information concerning the present on-or off-hook status of each line at each station. The actual status detecting procedure is well known in the art and in a typical situation a line transformer is pulsed to determine if current is flowing therein. Any other system may be used to generate station status information corresponding to the on-or off-hook condition of each line at each station, including any system where this information is provided to the processor upon request directly from equipment at each station.

Each scan cycle is divided into a number of time slots, each slot being associated with a particular line at a particular station. Each station has associated therewith a fixed number of time slots, which number need not be the same for all stations, but may be any number desired. Each line appearing at a station is assigned to one of the time slots and a detected off-hook or busy condition of that line at a given station is represented by a "1", while a detected on-hook condition

is represented by a "0" in the corresponding time slot.

One complete scan cycle thus produces a continuous data stream containing "1s" and "0s", the length of the stream being equal to the total number of reserved time slots. Accordingly, a fifty-station system, each station having ten reserved time slots, will generate a 500-bit data stream once each scan cycle. Comparison of any bit in the stream with the corresponding bit generated during a previous scan cycle will produce an output only when the compared bits are not the same. (See for example U.K. Patent No. 1141903).

The memory loop ML1 is constructed so as to contain the same number of domain positions therein as there are time slots in the scan cycle. Thus, each of the memory loops ML1 to MLn are constructed so as to contain 500 consecutive positions through which a domain will be propagated before being recirculated through some fixed position in the loop.

Each of the 500 positions in each loop corresponds to a unique one of the time slots of the scan cycle. The time interval of a total scan cycle is selected to be equal to the propagation time of a domain around the memory loop and is controlled by the control circuit 13 working in conjunction with the scan pulse 12 of processor 10. Thus, since a domain which is propagated around the memory loop shift register ML1 moves consecutively from position to position, any domain position may be arbitrarily selected to correspond to the first time slot and the next domain position away from the direction of propagation would then correspond to the second time slot. This direct correspondence is maintained for each memory loop position, and thus each time slot is represented in the memory loop by a domain position.

One of the memory loops ML1 is arranged to compare stored information, one bit at a time, with information currently generated in the scan cycle.

The generated bits may be thought of as interrogation data bits for determining the current (previous scan cycle) information stored in the memory. These interrogation bits are represented by domains which are generated and supplied to interrogation shift register SL1 by domain generator GA, e.g. as described in U.K. Patent No. 1257857.

The 500-bit scan cycle output is supplied, one bit at a time, to the domain generator GA such that a magnetic domain representation of the present busy-idle status of each line at each station is obtained. Thus, for example, a "1" in the first time slot generates a domain in a first domain position in the interrogation shift register SL1, while a "0" in the second time slot will allow the shift

register SL1 domain position next following to remain empty of a domain.

The domain in the interrogation loop SL1 move synchronously with the domains in the memory loop ML1 since both domains are under the influence of the same rotating magnetic field source 15 and the same bias source 16. Thus, when a domain in the interrogation shift register SL1 moves through a certain number of positions, a domain in the memory shift register ML1 moves through a corresponding number of positions. The interrogation loop SL1 is constructed to contain x number of positions before the interreaction point IP2 so that a domain, or lack of a domain, associated with the first interrogation position P0 corresponds with a domain, or lack of a domain, associated with a position Q0 in the memory loop x number of positions before the interreaction point IP2 between the two loops. It follows therefore that at some future time, corresponding to the movement of the domains through x positions, the two domain representations will interreact with each other magnetically to provide output signals controlled by their specific interreaction.

FIG. 1A shows the domain propagation paths represented by arrows. The direction of each arrow indicates the direction of domain propagation therein.

Domain channel SL1 is the interrogation channel and contains domain representations of the present status of the respective telephone stations. Domain channel ML1 is the memory channel and contains domain representations corresponding to the past status of the telephone stations. Domains in these two channels are coordinated such that when a domain representation corresponding to a certain station is present in channel SL1 at the interreaction point IP2 the domain representation in channel ML1 at that interreaction point also corresponds to that same station.

Memory loop ML1 is constructed with two alternative channels ML1—1 and ML1—2 branching out from the interreaction point IP2. Thus, as will be detailed hereinafter, a magnetic domain representation propagated in the memory channel ML1 will either follow channel ML1—2 and channel SL2—2 before reentering the memory channel ML1 at interreaction point IP5, or will follow channel ML1—1 to reenter memory channel ML1 at that same interreaction point. The total distance between interreaction point IP2 and interreaction point IP5 is the same whether a domain representation follows the first path or the second path.

The preferred path that a domain representation follows if no force other than the rotating magnetic field is applied thereto is along the channel ML1—2. Domains only enter channel ML1—1 when an interreaction

occurs between a domain in memory loop ML1 and a domain in interrogation loop SL1 at interreaction point IP2. Such an interreaction implies that a match condition between the present status and past status of the corresponding station is detected and thus no further action is to be taken.

The interreaction between the domains from channels ML1 and SL1 causes both domains to follow the nonpreferred paths of ML1—1 and SL1—3, respectively. Thus both read heads 31 and 32 are bypassed and no signal is sent to the processor.

Domains in channel SL2 are generated in parallel with domains in channel SL1 and are thus coordinated therewith with domains in channel ML1. The length of the path which consists of channels SL2, SL2—1 and SL2—2 is constructed such that this coordination is maintained at interreaction point IP5 between domain representations in channel SL2—2 and ML1—1. Thus, since a domain will only be present in channel ML1—1 at interreaction point IP5 if that domain interreacted with a domain at interreaction point IP2, a domain will also be present in channel SL2—2 at interreaction point IP5 in coordinated relationship to the domain in channel ML1—1. These domains intersect in such a manner that a domain becomes present in memory loop ML1 in the same position as would have been occupied by the domain propagated in channel ML1—1. Thus the memory loop ML1 still contains the domain representation of the past status of the corresponding station.

Under certain conditions the domain which should be present under the conditions described above in channel SL2—2 has been removed from that channel by a previous interreaction. In this situation, as will be described subsequently, a domain would be present in channel IL1—2 and this domain would also be coordinated with the domain in channel ML1—1. The interreaction point is constructed in such a manner that the domain in channel ML1—1 upon interreaction with the domain in channel IL1—2 enters memory loop ML1 at the proper position.

When a mismatch occurs at interreaction point IP2 as a result of the present status of a telephone station being different from the past status of that station, no interreaction can take place and therefore one of the domains must move past the respective read head. For example, in the event a domain is present in channel SL1 and no domain is present in channel ML1 the domain in channel SL1 moves along channel SL1—1 and past Active Read Head 31. A signal is thereby sent to the processor as an indication that an inactive to active mismatch has occurred. If, on the other hand, a mismatch occurs where a domain is present in channel ML1 that domain continues along

channel ML1—2 and past Inactive Read Head 32. Thus the active to inactive condition is reported to the processor.

Under the last-mentioned condition where the memory contains a domain and the present status of the corresponding station is inactive the domain continues along channel ML1—2 to interreaction point IP4. Since channel SL2 is coordinated with channel ML1—2 and with channel SL1 no domain is present at interreaction point IP4 when the mismatched domain in channel ML1—2 is propagated thereto. These two representations pass each other and thus channel SL2—2 contains no representation at the coordinated position. This vacant position is propagated along channel SL2—2 and enters memory loop ML1 at the coordinated location therein. Thus, the memory loop now contains a vacant position where a domain was present prior to interrogation. Accordingly, the memory has been updated in accordance with the information provided thereto by the interrogation channels.

In the situation where it is desired to prevent the memory from being updated domains are generated in channel IL1 in coordination with domains in the memory channel ML1—2 in such a manner that when a domain arrives at interreaction point IP4 in channel ML1—2 representing a mismatch condition that domain is forced to enter channel SL2—2 and thus enter the memory loop ML1 in the same position that is previously occupied. Accordingly, the memory is not updated under control of domains in auxiliary channel IL1—1.

The precise interreaction forces which are present at each of the interreaction points will now be discussed in detail with reference to FIGS 2 to 12.

Interreaction Between Channels

FIG. 2 shows a portion of the domain propagation device corresponding to Section I of FIG. 1. The interrogation channel SL1 begins with domain generator GA and ends with domain annihilation devices EA and EB associated with respective interrogation channels SL1—1 and SL1—2. The annihilation devices or "domain eaters" are arranged as described in U.S. Patent No. 3577131 to reduce any domain circulated thereto.

The memory loop ML1, as illustrated in FIG. 2, begins with the portion of the channel shown and branches out into two alternative memory loop paths ML1—1 and ML1—2. Domains in the respective channels propagate in the direction of the arrows in response to a counter clockwise rotating magnetic field.

Mismatch Between Interrogation and Memory Shift Registers (1, 0)

Assume that at an arbitrarily selected time a

domain is generated corresponding to a detected off-hook condition of a line associated with the first time slot of the first station to be scanned. Accordingly, a domain, represented as a "1", is placed at position P0 of FIG. 2 in the interrogation channel SL1. As illustrated, there are 25 positions between position P0 and P25 in the interrogation loop SL1 and there are 25 positions between positions Q0 and Q25 in the memory loop ML1. Thus, position P25 of channel SL1 is synchronously coordinated with position Q25 of channel ML1.

Remembering that the number of positions in the memory loop has been selected to correspond to the number of time slots of a complete scan cycle, it follows then that the domain, or lack of domain at position Q0 in the memory loop ML1 represents the previous status of the line associated with the time slot now represented by a domain in interrogation channel SL1 position P0. The domain representation in the next succeeding memory loop position Q—1 corresponds to the previous status condition of the line in the time slot to be scanned next in the scan cycle. Thus, it will be noted that the interrogation channel SL1 need not be so large as to contain a representation for every time slot as long as each status representation is sequentially applied thereto in fixed order.

Normally the number of positions in the interrogation channel would be selected so that the domain generation and annihilation devices are physically separated from the interreaction point IP2 and from each other so as to prevent interference therebetween and to allow for electrical connections thereto.

Inactive to Active Change

Assume that a domain is present in position P0 of the interrogation channel SL1 corresponding to an active or off-hook condition of the line assigned to the first time slot of the first station. Thus, a "1" is represented at position P0. Assume also that the previously detected status of that same line at that same station was inactive or an on-hook condition. Then position Q0 of the memory loop ML1 would be vacant, representing a "0" thereafter.

At the conclusion of the 25th positional movement (six and one-quarter field rotations) the representations will be at positions P25 and Q25, respectively. Thus position P25 contains a domain representation and position Q25 is vacant. When the field moves an additional quadrant the interrogation channel SL1 domain moves to position S1 and position M1 in the memory channel ML1 becomes vacant.

It will be noted that S1 and M1 are coordinated positions and correspond to domains moved from positions P25 and Q25, respectively. The change in the positional

counting designations is for drawing and descriptive clarity.

At the next quadrant of the field the interrogation domain moves to position S2. Memory channel ML1 position M2 is now vacant. At each successive quadrant the interrogation domain moves along the positions S3, S4, and S5. When the interrogation domain reaches position S5 the memory channel is vacant at position M5. These respective representations continue to be moved one position at a time along their respective channels. Thus the interrogation domain moves along channel SL1—1 while the coordinated vacant position moves along channel ML1—2.

Status Change Signal

At the 49th positional movement the respective domains arrive at positions P49 and Q49 over which positions a read head, such as Active Read Head 31 or Inactive Read Head 32 is associated. These read heads may be Hall-effect detectors as described in U.S. Patent No. 3609720 arranged so as to provide a signal whenever a domain is detected at a certain position. Since position Q49 is vacant, no signal is transmitted from Inactive Read Head 32. However, an output signal is transmitted to the utilization circuit 14 of processor 10 from Active Read Head 31 due to the presence at position P49 of a domain. This signal is an indication that a station is now off-hook and that the "scratch pad" memory 17 contains an on-hook representation thereof, i.e., an inactive station going active.

The identity of the station which has changed status is provided to processor 10 at this time from memory loops ML2—MLn, (FIG. 1). To be specific, the overlay defining the memory loops ML2—MLn is constructed so as to contain the same number of positions as does memory loop ML1. Utilizing the fact that domains in all loops propagate from position to position at the same rate, domains can be placed into these loops and coordinated with the respective positions of memory loop ML1 such that the binary word formed upon detecting the presence or absence of a domain under a read head at a fixed position in each loop, such as read heads 33—34, yields the station number and the line thereof of the signaling station.

Processor 10 may accept the information supplied by "scratch pad" memory 17 or it may ignore that information. If the information is accepted, the memory loop ML1 is updated under control of update pulse source 11 in the manner to be detailed hereinafter so that a domain is inserted into the previously empty memory position corresponding to the now active line. In the event the information is not accepted, such as when the processor is overloaded or not functioning properly, or when the processor is arranged to accept

information only after it has been proffered a certain fixed number of times, the memory loop ML1 is not updated and the position corresponding to the currently active line remains vacant.

When the status change information is not accepted and the active line remains active, the processor 10 again receives an off-hook signal during the next scan cycle. The precise manner in which the overlay is constructed so that memory updating and memory update inhibiting is performed will be more fully detailed hereinafter.

Returning now to FIG. 2, after a domain passes Active Read Head 31, it is moved along channel SL1—1 to annihilator EA and reduced. The number of positions between the readout head 31 and the annihilator EA is not critical and is determined by the physical characteristics of the overlay.

Match Between Interrogation and Memory Shift Registers (1, 1)

Now assume that a certain line at a certain station is detected as being off-hook. Accordingly, a domain is generated into position P0 of the interrogation shift register SL1 during the time slot associated with that line and station. Also assume that during the same time slot in a previous scan cycle an off-hook condition was detected and the memory updated in accordance therewith. Accordingly, a domain is present in the memory shift register ML1 at position Q0. As detailed above, these domains are propagated along their respective channels one position at a time until at the end of the 25th positional movement domains are present at positions P25 and Q25, respectively.

Turning now to FIG. 3, at the next quadrant of the rotating magnetic field domains are located at positions S1 and M1 in the respective shift registers. At the next quadrant the domains move to positions S2 and M2, respectively. When the domains are in this position they are relatively close to each other and exert a mutually repulsive force f1 between them. However, since at this point the overlay pattern is constructed such that neither domain has an alternative position to which it can move, they each remain in their respective positions.

At the next quadrant of the field the interrogation domain attempts to move to position S3, its next preferred position. However, because of the repulsive force f1 the interrogation domain moves instead to an alternative position S3'. Similarly, the memory domain attempts to move to position M3 but instead is repelled to position M3'. At each succeeding quadrant phase the respective domains move along the channels SL1—2 and ML1—1.

Returning again to FIG. 2, it will be seen that channel SL1—2 is a path to annihilator

EB and the interrogation domain which was diverted from interreaction point IP2 and channel SL1—1 leading to the Active Read Head 31, will be reduced. Thus, at the conclusion of the 49th positional movement, as counted from position P0, position P49 will be vacant and Active Read Head 31 will not transmit a signal to the processor 10. The memory domain, which was diverted from the interreaction point IP2 and the channel ML1—2 leading to the Inactive Read Head 32, now follows the memory channel ML1—1. The purpose of this diversion, in addition to causing position Q49 to be vacant during the 49th positional movement so as to prevent Active Read Head 31 from transmitting a status change signal to the processor at this time, will become more apparent later.

Thus when domains in corresponding positions of each of the two shift registers, SL1 and memory ML1 are propagated through an interreaction point IP2, they are each diverted along separate paths of the overlay so as to bypass the output signaling devices associated with certain fixed positions in each shift register.

Mismatch Between Interrogation and Memory Shift Registers (0, 1)

Now assume that a previous active line is detected to be inactive. Assume also that the memory has been updated in accordance with the previous condition so that the memory now contains a domain in the associated memory position. Accordingly, position P0 in shift register SL1 is vacant when the time slot associated with the line and station in question is interrogated. However, a domain is present in position Q0 of shift register ML1 at the corresponding time slot. As detailed above, at the end of the 25th positional movement thereafter position P25 is vacant and position Q25 contains a domain.

Turning now to FIG. 4, it will be seen that the domain in position Q25 moves without interference through interreaction point IP2, from position M1 to position M5 during the next five quadrants of the rotating magnetic field. Thus, the domain continues to move along the channel ML1—2 during each succeeding quadrant of the magnetic field while the corresponding positions in channels SL1—2 and SL1—1 are vacant.

Returning now to FIG. 2, at the conclusion of the 49th positional movement, as measured from position Q0 in memory loop ML1, position Q49, which position is monitored by Inactive Read Head 32, contains a domain. Accordingly, an output signal is transmitted to the processor 10, FIG. 1, at this time together with the identity, as obtained from the shift register loops ML2—MLn, of the new inactive or on-hook station.

Thus, at this time the processor 10 is

signaled that a status change has taken place at a specific station and at a specific line thereat. Again the processor may accept this indication and update the memory in accordance with the new status. Or the processor may ignore the signal, in which case the memory loop is not disturbed. The exact manner in which this memory updating and update inhibiting is accomplished will be more apparent later.

Memory Update and Update Inhibit Channels

Turning now to FIG. 5, domain generator GB is arranged to generate a domain whenever a domain is generated by domain generator GA, shown in FIG. 2. Thus, the presence or absence of a domain at position H0 in shift register SL2 corresponds to the detected busy-idle status of a line at a station in the corresponding time slot. The number of positions between position H0 and position H49 of shift register SL2 is carefully constructed to equal the number of positions between position P0 of shift register SL1, FIG. 2, and Active Read Head 31, which in this case is 49 positions. Thus, 49 represents the summation of the x and w dimensions as shown in FIG. 1.

Continuing now in FIG. 5, assume that a domain is present at position H0 at some arbitrarily selected time representing a busy condition detected during the associated time slot in the scan cycle. After the 49th positional movement the domain is present at position H49 in shift register SL2. Since this domain is moved synchronously with the domain in shift registers SL1 and ML1 and since the domain at position H0 is generated concurrently with a domain in shift register SL1, position P0, both domains reach the 59th position at the same time. It will be recalled however that the domains in shift registers SL1—1 and ML1—2, as shown in FIG. 2, only reach their respective 49th positions if they are mismatched. FIG. 1A may be helpful at this point for reference. Assuming such a condition, then processor 10 is notified of a status change in the manner described previously.

If the processor accepts the information, update pulse source 11, which pulse source has been providing pulses for the generation of domains via domain generator GC, is inhibited and a domain is not generated at the corresponding time in channel IL1. Accordingly, as shown in FIG. 5, the presence or absence of a domain in shift register IL1 at position J49 corresponds to the inhibit or update control, respectively, of the memory loop. For example, a domain in position J49 prevents the memory from being updated while the absence of a domain at position J49 is an update signal to the memory. The

precise manner in which the updating or inhibiting occurs will be detailed hereinafter.

Assuming now that a domain is present at position H49 of shift register SL2 and that a domain is also present at position J49 of shift register IL1, these domains will be propagated together so that they appear sometime later at coordinated positions B1 and A1, respectively, of interreaction point IP3. At each succeeding quadrant of the rotating magnetic field the domain in shift register IL1 will move one position down the channel and at the end of four quadrants will appear at position A5. However, because of the interreaction force f_2 between the domains, the domain in shift register SL2 moves to position B5' instead of its normally preferred position B5.

Continued rotation of the magnetic field will move the domain in shift register SL2 down the channel to annihilator EC. Thus, in the condition where the memory is not to be updated, the domain in shift register SL2 is removed therefrom by the domain generated in shift register IL1. Accordingly, for a mismatch condition where the memory is not to be updated, coordinated positions in channel SL2—1 are vacant while the corresponding positions in channel IL1—1 contain domains. The importance of this condition will be appreciated later.

Turning now to FIG. 6, in the situation where a domain is present in shift register SL2 and the processor elects to update the memory, position J49 is vacant. In this situation the domain in shift register SL2 moves through the interreaction point IP3 in the manner shown without interference. Thus for memory updating, channel SL2—1 contains a domain while channel IL1—1 is vacant.

Summarizing briefly: when an off-hook condition is detected a domain is inserted into auxiliary channel SL2 in a position coordinated with a position in the interrogation channel SL1. In the situation where the memory is to be updated in accordance with the detected condition, the domain representation is allowed to remain in the auxiliary channel. In situations where the memory is to remain unchanged, the domain in the auxiliary channel is removed therefrom by the interreaction of a domain generated under control of the processor. As will become more apparent later, the updating arrangement functions in this same manner whether a busy or idle status is detected.

Mismatch Condition—Memory Remains Unchanged

Turning now to FIG. 7, it will be recalled that when the memory contains a domain at a particular location and that location is interrogated by a vacant representation, a mismatch occurs and the memory domain continues along the channel ML1—2, FIG. 1A. A fixed

number of positions thereafter, corresponding to the y dimension shown in FIG. 1, the domain in memory shift register ML1—2 arrives at position N1, FIG. 7. Since a mismatch between the memory channel and the interrogate channel has been assumed, (the interrogation channel being vacant) and since domains are generated into the interrogate channel and channel SL2 concurrently, channel SL2 is vacant at the position coordinated with position N1 of channel ML1—2. In addition, since the total length of channels SL2 and SL2—1 is constructed to equal x plus y positions then position D1 of channel SL2—1 corresponds to position N1 of channel ML1—2. Thus at this time position N1 contains a domain and position D1 is vacant.

Since it has been assumed that the memory will not be updated at this point, channel IL1—1 contains a domain at the coordinated position C1.

Before continuing, it should be noted that channels ML1—2 and SL2—1 form a crossover pattern having the characteristic that a domain propagated in either channel will continue straight through the intersection point. A further property of such a crossover is that when domains enter the intersection simultaneously from both channels they will each pass through the intersection without interfering with each other. The construction shown in interreaction point IP4 utilizes two crossovers which interact with each other in the manner to be detailed hereinafter. It should also be noted that a domain, such as domain K1, is permanently trapped at the intersection between the channels. That domain if nothing else were to happen, would continue to recirculate in a closed loop through positions K2, K3, and K4, returning to position K1 after one complete revolution of the magnetic field. Such a crossover is described in U.S. Patent No. 3,543,255.

Continuing now in FIG. 7, it will be seen that at the arbitrarily selected starting point domains are in positions N1, K1, L1, and C1. At the next rotation of the magnetic field domain N1 moves to position N2 and domain K1 moves to position K2. At the same time domain C1 moves to position C2. Domain L1, the trapped domain, attempts to move to its next preferred position L2 but is repelled by repulsive force f_5 and moves instead to position L2'. This last-described action is the typical action of a crossover where the trapped domain continues along the channel and the incoming domain becomes the trapped domain.

At the next quadrant of the magnetic field, domain N2 moves to position N3 and domain C2 moves to position C3. Domain K2 then comes into the repulsive force f_3 of domain N3 and then attempts to move to position K3' to complete the crossover pattern. How-

ever, domain K2 is also now repulsed by force f4 from domain C3 and moves to its regulator position K3 under the influence of domain C3. Domain N2, although under a repulsive force f3 from domain K3, does not have an alternative position to which it could move during this phase of the field rotation, so it remains at position N3. Domain L2' moves to position L3'.

At the next quadrant of the field rotation domain K3 moves to position K4. Repulsive force f3 then moves domain N3 to position N4'. Domain C3 moves to position C4 while domain L3' moves to position L4'. Domain C3 becomes the trapped domain at the crossover of channels IL1—1 and IL1—3.

During the next eight quadrants of the rotating field the domains in the respective channels move along the indicated positions so that at the end of the twelfth quadrant a domain is in channel IL1—2 at position L12' and a domain is in channel SL2—2 at coordinated position N12'. It will be noted that channel IL2—2 contains a timing loop at positions L8' to L12'. The purpose of this loop is to delay the domain therein so as to maintain coordination between domains in the respective channels, IL1—2 and SL2—2. Thus, in situations where a mismatch occurs and the memory is not to be updated, a domain is in position L12' while a domain is in position N12'.

Turning now to FIG. 1, since as discussed above, a domain only enters channel ML1—1 when a domain is present in channel ML1 and is mismatched to a domain in channel SL1, it follows that for all mismatched conditions a vacant position occurs in the corresponding position of channel ML1—1. Channel ML1—1 is constructed to equal the number of positions y in channel ML1—2 plus the number of positions z in channel SL2—2. As a result of this overlay construction, respective positions of intersection point IP5, such as positions G1 and F1, FIG. 10, are coordinated positions.

Continuing now with FIG. 10, the domain pattern described above for interreaction point IP4, FIG. 7, will now be followed down the respective channels and will be described for interreaction point IP5. Thus, position G1 is vacant when the corresponding domain is propagated to interreaction point IP5. Thus, since the domains which are coordinated with position G1 are the domains in channels SL2—2 and IL1—2 from interreaction point IP4, and since a mismatch condition is assumed, then positions E1 and F1 both contain domains. Accordingly, a domain is present in each of the positions E1, F1, R1 and T1. The domains in the latter two positions are the trapped domains at the intersection points.

In the manner discussed above, repulsive forces f10 and f9 cause the trapped domains

to move down the respective channels IL1—4 and ML1 and the domains E1 and F1 then become the trapped domains. Since channel IL1—4 leads to annihilator E6, the domain therein is reduced after a number of positional movements. After the twelfth positional movement, a domain is inserted into memory channel ML1 at position T12' which position corresponds to the memory location of the previously stored domain. Accordingly, the memory ML1 remains unchanged and a domain representation corresponding to an active condition of a certain line at a certain station continues to be in the memory ML1 even though that line has now been detected as being inactive at that station.

Mismatch Condition—Memory Update

Returning to FIG. 8, another condition which could occur at interreaction point IP4 will now be detailed. Accordingly, assume that a mismatch occurs between a domain representation (active condition) in memory and a vacant representation (inactive condition) in the interrogation channel. Then a domain representing the memory domain would be at position N1 of channel ML1—2 at the time when position D1 represents an interrogation channel SL2—1 vacancy and position C1 represents an inhibit channel IL1—1 vacancy. In this situation the crossovers function in a typical manner so that the domain at position N1 moves there-through into channel IL1—3 and to annihilator ED, FIG. 7.

The positional movement through the crossovers is as follows. At the third quadrant of the field domain N1 has moved to position N3 thereby forcing domain K1 to assume position K3' via force f7. Domain L1 has also been forced to assume position L3' due to force f6 now exerted by the domain in position K3'. Thus, domain N1 replaces domain K1 as the trapped domain in the lower crossover, and domain K1 in turn replaces domain L1 as the trapped domain in the upper crossover. Domain L3', which now represents domain N1, moves toward annihilator ED, as shown in FIG. 7, and is reduced after a number of positional movements. Accordingly, after twelve field rotations, positions L12' and N12' are vacant.

Turning now to FIG. 10, positions E1 and F1, which positions correspond to the continued positional movement of positions L12' and N12', respectively, are vacant when the just described domain positions are occupied. Position G1 of channel ML1—1 must also be vacant at the coordinated time due to the assumed mismatch condition as discussed previously. Accordingly, the trapped domains remain trapped and the vacant domain position at G1 is moved on position at a time until after the 12th quadrant rotation, position T12' of memory register ML1 becomes vacant.

Thus, the memory position T12' associated with the previously recorded active condition now contains a domain representation, i.e., domain vacancy corresponding to an inactive condition. Thus, the memory has been updated in accordance with the information communicated thereto from the interrogation channel.

Turning now to FIG. 9, the situation where the memory contain a vacant position (inactive condition) and the corresponding interrogation point is detected active, will be detailed. In this situation, an inactive to active mismatch occurs and position N1 of memory channel ML1—2 is vacant. Position D1 contains a domain since the memory is to be undated. This follows since channel SL2, FIG. 5, contains a domain at position H49 which domain interreacts with a domain in position J49 when the system is in the update inhibit mode. The domain in channel SL2—1 is thus removed in the manner previously discussed when the system is prepared for memory updating. Position J49 remains vacant and a domain enters channel SL2—1.

Continuing now in FIG. 9, and assuming the system to be in the memory update inhibit mode, channels ML1—2 and SL2—1 are vacant at positions N1 and D1. Twelve positional movements later position K12' becomes vacant. This follows since the auxiliary channel domain C1 moves through the crossover to channel IL1—2 in the typical manner, and the vacant positions N1 and D1 are moved through the crossover, also in the typical manner. Thus channel SL2—2 has a vacancy at position K12'. This vacant position is propagated down channel SL2—2 to interreaction point IP5, FIG. 10. Since the coordinated position G1 of memory channel ML1—1 must now also be vacant, as discussed above for a mismatch condition, after twelve field rotations position T12' in memory register ML1 is vacant. Thus, the memory remains vacant at the proper plate therein even though an active condition has been detected at the corresponding line and station.

Again turning to FIG. 7, a further situation will now be detailed with respect to interrogation point IP4. Assume that the memory is to be updated in accordance with the detected data. A domain would then be present at each of the positions D1, K1, and L1. The domain at position D1 corresponds to a detected active condition. Position C1 is vacant because of the update condition and position N1 is vacant because of the vacant memory position. At the next quadrant of the field domain D1 moves to position D2. Domain K1 is then repelled to position K2'. Domain D2 then becomes the trapped domain while domain K2' continues along the channel SL2—2 and ten field rotations later appear at position N12'.

Digressing momentarily, it will be noted

that the positional movement of the domain through interreaction point IP4 is critical if the domain is to remain associated with the proper memory position. Thus, assuming a starting point at position D1, FIG. 7, eleven quadrants later the domain or vacancy associated with position D1 must be at position N12'. In addition, eleven quadrants after a domain is in position N1 (the coordinated position to position D1) that domain must also be at position N12'. This fact is illustrated in FIGS. 7 and 9 where position N12' corresponds to position K12'.

It should be pointed out that due to the nature of the crossover, position K1 acts as though it was position D1. Thus, a domain at position D1 advances one full cycle (four positions) with one quadrant rotation of the field. This advancing is compensated for in the timing loop detailed in FIG. 8, which loop consists of the positions K4', K5', K6', and K7'. The overlay could be constructed such that this timing loop occurs at another point prior to position K12' and even could occur in channel SL2—1.

Returning now to FIG. 9, the domain at position K12', representing a situation where the memory was vacant and was compared to domain representation in the update mode, moves down channel SL2—2 and through interreaction point IP5, FIG. 10, in the manner illustrated. This follows since position G1 of channel ML1—1 is vacant due to the mismatch condition and thus the crossover at interreaction point IP5 functions in a typical manner. Thus a domain, as rotated from position K12', arrives at position T12' of memory loop ML1 at the proper time. Accordingly, a mismatch condition, where the memory previously contained a vacant position, has been detected and the memory updated in accordance with the data bit circulated thereto so that a domain representation of that data bit now appears in the corresponding memory location T12' of memory loop ML1.

Match Condition-Memory Remains Unchanged

Two situations may exist in which a match condition occurs. Either the memory channel and the interrogation channel both contain a domain in corresponding position or they both are vacant at those positions.

In the situation where they both contain domains the domain in the memory loop ML1 will bypass the read head, FIG. 2, as discussed above and will move in channel ML1—2. Since no signal is sent to the processor a domain is generated in the auxiliary channel IL1 as discussed above. Thus, the domain in the second interrogation channel SL2 is removed therefrom as shown in FIG. 10 and as discussed above.

Turning now to FIG. 12, under the conditions just discussed, channel SL2—2 is

vacant at position F1 and channel IL1—contains a domain at position E1 when the coordinated memory domain is at position G1 of memory channel ML1—1. At the next quadrant of the field domain G1 moves to position G2 and domain E1 moves to position E2. Trapped domain R1 is then forced to assume alternative position R2' under the influence of repulsive force f15. Domain T1 moves to position T2.

At the next quadrant of the field domain R2' continues down channel IL1—4 to the annihilator EF shown in FIG. 10. Domain T2 assumes position 83 due to the repulsive force f16 and domain G2 assumes position G3. At the next quadrant of the field force f14 causes domain G3 to move to position G4' while domain T3 moves to position T4. Domain G5' is then in memory channel ML1 at the proper position as discussed above and thus the memory channel, which previously had a domain therein at that location, still contains a domain at the same location.

In the second situation where both the memory and interrogate channels contain vacancies at corresponding points, a review of FIG. 12 will show that when positions F1 and G1 are both vacant, channel ML1 would remain vacant at the associated position. Thus, the memory always remains unchanged when a match condition exists between the memory representation and the interrogation representation.

FIG. 11 illustrates a situation which does not exist in the case of the present embodiment but which could occur in an arrangement wherein a memory update signal (lack of a domain in channel IL1) is always present and a domain generated only when a mismatch occurs and only when it is desired not to update the memory and only when the mismatch is active to inactive. Under this condition where a match occurs, no domain is present in the auxiliary channel IL1 so the domain in the second intersection channel SL2 remains therein. Thus, in this situation a domain is present at positions F1 of channel SL2—2 and G1 of memory channel ML1—1. These domains bypass each other at the intersection point in the manner previously discussed so that the memory channel ML1 retains a domain at the proper position T12'.

As so far described a plurality of shift register loops have been arranged in a magnetic domain propagation device to provide status change signals to a processor in a telephone communications environment, but it is of course to be understood that this is by way of example.

In another exemplary application, the interrogation data bits which are compared to the memory data bits, instead of representing the busy-idle status of telephone lines, could represent the input word of a parity checking

device. In such an arrangement, the memory data bits could be arranged into memory words each containing a certain number of bits and each word compared, bit by bit, against the input word. The memory word then could represent a first received word and the input word then would represent a next received word. Comparison between the words would yield a parity check on the transmission. The automatic undating feature could then revise the first received word in accordance with the next received word and at the same time transmit a mismatch signal back to the transmitting station so that the corrected information may be compared again to the retransmitted data.

Another form of memory device which finds application in the scanning of the conditions of a plurality of lines will now be described with reference to FIGS. 13 to 17.

In FIG. 12 the line scanner arrangement is symmetrical about an imaginary axis represented by vertical broken line 111. Thus portions of the arrangement to the right of the axis will be designated arbitrarily by the term "information" as, for example, information present look register. The portions of the arrangement to the left of the axis similarly will be termed "complementary". For every information portion there is a complementary portion.

It is also helpful to visualize the arrangement as divided into three sections I, II, and III along the path of information flow from top to bottom as viewed in FIG. 13. This division is represented by imaginary horizontal broken lines 112 and 113. In section I, accordingly, there are input information and complementary present look registers 115 and 116, and in section II there are information and complementary last look registers 118 and 9. In section III there are information and complementary outputs 2 and 22 and information and complementary closed loop recirculating registers 123 and 124. Registers 123 and 124 are interconnected by a compressor circuit or register 125. It will become clear that section I functions as a "present look" store, section II as a "last look" store, and section III as a "corrected last look" store.

The operation of each of these sections will now be described along with the cooperation of each section one with another as well as the overlay geometry which defines the movement and interaction of domains in a juxtaposed sheet of magnetic material to achieve the operation.

Section I operates to provide complementary representations (viz., domain patterns) of the conditions of a plurality of lines in a pair of domain channels. The section comprises the input information and complementary present look registers 115 and 116 along with an arrangement for recording initially the con-

dition of n scanned lines. The recording arrangement comprises magnetically soft permalloy elements defining recording information and complementary registers 126 and 127. Domains are not moved along registers 126 and 127 but are displaced only laterally there, e.g. by pulsed electrical conductors to provide patterns in associated channels 115 and 116 as is now explained more fully.

Each of registers 115 and 116, on the other hand, is a familiar single wall domain register defined illustratively by bar and T-shaped overlay elements for moving domains therealong in response to a magnetic field rotating in the plane of a juxtaposed crystal C. The two registers 115 and 116 are physically separated by the two recording registers 126 and 127. Each of the registers 115, 116, 126 and 127 is n stages long.

In operation, a sequence of n domains is generated at G for movement in register 116 downward as viewed. A suitable generator for providing a domain for each rotation of the in-plane field is described in U.K. Patent No. 1257857.

In n rotations of the in-plane field, n domains occupy the n stages of register 116.

FIG. 14 shows the overlay geometry and conductor arrangement of the input section of FIG. 13 in detail. The figure shows the familiar T and bar-shaped elements of the overlay arrangement, each element being designated "ms" for "magnetically soft". It is to be noted that the bars of registers 115 and 116 are associated with bars similarly oriented and spaced along registers 126 and 127.

The figure also shows a number of conductor loops. The loops associated with register 126 are designated SP_n, SP (n-1), SP (n-2), . . . etc., the designation "SP" signifying "scan point". Each of these loops is discrete, associated with a different line which may be a telephone auxiliary line, and generates a magnetic field to attract domains from associated stages of register 127 when a current (i.e., off-hook) appears on the conductor.

In addition, the figure shows three conductors 130, 131, and 132, each of which includes a plurality of conductor loops which couple associated sets of magnetically soft bars. The loops of conductors 130, 131, and 132, specifically coupled the bars of register 115, register 127, and register 116, respectively. The loops of conductors 130 and 131 also can be seen to extend to encompass portions of the bars associated with registers 126 and registers 116, respectively, whereas the loops SP_n encompass portions of corresponding bars associated with register 127.

A scan operation is initiated by filling register 116 with domains as stated above and by pulsing conductor 131 thereafter to move all

the domains in register 116 to the left side of the magnetically soft bars of register 27.

Conductor 131 is pulsed when the in-plane magnetic field is directed to the left in FIG. 14 so that the domains occupy positions at the left end of the bars encompassed by the loops of conductor 131 when the conductor is pulsed.

If a current exists in any of the conductor loops SP_i, the associated domain moves to the left side of register 126 because of the attracting field associated with such current. Thereafter, both conductors 130 and 132 are pulsed. The pulse in conductor 130 operates to move domains associated with register 126 to positions to the left end of corresponding bars of register 115. Similarly, the pulse in conductor 132 operates to move domains associated with lines SP_i for which no (off-hook) currents exist to the left end of associated bars of register 116.

During the scan operation, the in-plane field remains directed to the left.

The scan operation is now complete with a domain pattern representative of the pattern of (off-hook) currents in the lines stored in the information register 115 whereas the domain pattern representative of the pattern of no (off-hook) currents in the lines is stored in the complement register 16.

FIG. 14 show the bar and T-shaped elements of registers 115 and 116 extending downward, as viewed, beyond conductors 130 and 132 into section II for an additional n stages (or positions). It is important to note that each of these extensions 118, and 119, turns on itself as is clear from FIG. 13. The overlay elements are disposed to form "decision points" designated "dp" (shown in FIG. 14 and described only for the information register 118). It is to be understood, however, that the complementary register 119 includes a similar decision point which operates synchronously and in analogous fashion.

A domain pattern formed in section I in the information register 115 (as well as the pattern formed simultaneously in complementary register 116) is advanced, at the conclusion of the scan operation, n stages, into the extension of the register(s) shown in section II. A second scan operation, identical to that described above now occurs, the in-plane field being maintained in a leftward direction as before during the operation. A new domain pattern stored at this time may be thought of as the "present look"; the previous pattern of domains now advanced into section II may be thought of as the "last look". It is appropriate therefore that section I be designated the "present look store", PL, and section II be designated the "last look store", LL.

Consider the situations where two scan periods have occurred and both the present and last look are occupied by domain patterns. The information is now advanced, consecu-

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tive representations in both the present and last look store entering decision point dp. In this context, the decision point dp can be understood to perform a logic function between consecutive representations of the conditions of each of the lines scanned. The logic is performed by taking advantage of the interaction between domains as described in copending U.S. Patent No. 3577181. For example, the overlay elements at the decision point are disposed so that if a domain occurs at both positions *a* and P1 in the extension of register 115, thus indicating a current in a given one of conductors SP_i during two consecutive scan periods, the domains interact causing the domain at *a* to follow the path *a*, *b*, *c*, *d*, *e*, as the in-plane field rotates (clockwise). The domain can be seen to move to the right as viewed along a further extension of register 115 designated '1—1'. The designation '1—1' indicates that a domain moves therealong only if a domain (a binary 1) occurs in positions P1 and *a* simultaneously. The consecutive domain positions P1, P2, P3, P4, and P5 are shown to provide an aid to the reader in relating domain position to in-plane field orientation. The field in rotating clockwise one rotation moves a domain from position P1 to position P5.

Of course, if a domain were absent in either the present or last look store when a decision is made at dp, no domain advances along '1—1'. If for example, the last look store has a domain absent (at *a*), there is no domain to advance along '1—1' regardless of whether or not a domain is present at P1 at the critical time. On the other hand, if a domain were absent at P1, no interaction would occur to direct a domain to *e*. The domain at *a*, in this latter instance, would follow the path *a*, *b*, *c*, *d*, *f*, moving upward as viewed to a familiar domain annihilator E1 where it is extinguished.

A similar analysis indicates that a domain advances along the register '0—0', on the complementary side of the arrangement only if a domain were present at positions *a'* and P1' simultaneously. In this instance, the presence of domains indicates no currents in the associated line during two consecutive scan periods. The designation '0—0' indicates such a condition.

The in-plane field is again directed to the left when a third scan period is initiated. A new pattern of domains, as well as the complement of that pattern, is stored in section I. The patterns of domains which have already advanced beyond the decision point dp, and the complements thereof, have moved synchronously along register '1—1' or '0—0', into section III of FIG. 13.

It is helpful to recognize the significance of the information which moves into section III. A domain in register '1—1' or '0—0' represents, in the first instance, a current in

a particular line (SP_i) for two consecutive scan periods and, in the second, the absence of a current in a particular line for two consecutive scan periods. Naturally, domains cannot appear in both registers '1—1' and '0—0' simultaneously in a position representative of a single line. Clearly, a change in the condition of a particular line is indicated, in this embodiment, by a domain in the associated positions of either register '1—1' or '0—0' (but not both) followed by a domain in the associated position of the other of the two registers at a later time. It is also clear that when a domain enters a first of registers '1—1' and '0—0' representing a first persistent condition of a given line, the only significant event occurring next for that line will be represented by a domain in the associated position of the second of those registers representing a second persistent condition.

In order to expedite movement of domains in registers '0—0' and '1—1', these registers operate as compressor circuits and are shown in FIG. 15 fully occupied by domains to so function.

The overlay geometry of section III is designed to respond to information representations of the form described to provide outputs at 121 or 122 of FIGS. 13 and 15 representative of the first and second changes in line conditions as described above. To be specific, section III comprises a pair of closed loop or "recirculating" information and complementary registers 123 and 124 defined by T and bar-shaped overlays to circulate information in response to a clockwise rotating in-plane magnetic field.

Each of the closed loop registers has *n* stages, one for each of the lines scanned. Accordingly, a stage of the information recirculating register 123 is associated with a corresponding stage of the complementary recirculating register 124 and those associated stages can be associated with a given one of the *n* lines scanned. Each associated pair of stages in registers 123 and 124 includes a domain—no domain pair. That is to say, only one stage of each pair of associated stages includes a domain. This is represented in FIG. 15 by the encircled plus sign (Di) representing a domain (information) and the encircled

minus sign (D̄i) representing the absence of a domain (complement).

The domain pairs associated with consecutive lines occupy the strategic positions shown in FIG. 15 consecutively. The importance of the positions is twofold. First, the positions are not only part of recirculating registers 123 and 124, they also comprise, illustratively, the terminal positions of a compressor register 125, as indicated in FIG. 13. A compressor register, it will be recalled, functions to dislodge a domain at one end

when a domain enters the other. The novel arrangement of a pair of recirculating registers each having a stage comprising the terminus of a compressor register will be seen to function to remember the previous persistent condition of each line scanned in terms of the position occupied by the absent domain of the recirculating domain—no domain pair. Since the scan operation, the propagation of domains, domain interaction, and domain pair recirculation are all synchronized by the rotating in-plane magnetic field, the representations of the last persistent condition of consecutive lines, appear consecutively at the strategic positions occupied by $\bar{D}_i$ and D_i in FIG. 15.

By the same token, the position occupied by the domain (D_i) of each domain—no domain pair signifies the next expected persistent condition, that is to say, the condition opposite to the last condition for the associated line. It is to be recalled that only two types of changes in condition are significant for a second scanned line in the illustrative arrangement.

Now it will be shown that the domain of each domain—no domain pair enables the output 121 or 122 to produce an output signal when a domain advances along the associated register '1—1' or '0—0'. The operation at this juncture is described with respect to the complementary portion of section III of FIG. 15. It is to be understood that, as before, the overlay geometry of the information portion of section III is designed to produce a like operation. Consider the condition represented

by absent domain $\bar{D}_i$ occupying position C and the associated domain D_i occupying the position shown in the figure. This condition is assumed to be followed by a new condition in which a domain D_i associated with a next subsequent line, occupies position C in FIG.

15 and the associated absent domain $\bar{D}_i$ occupies the position previously occupied by domain D_i in FIG. 15.

Broken block DPC of FIGS. 15 and 16 represents a decision point on the complementary side of section III. Register '0—0' is a compressor register of k stages designed to move information from section II to decision point DPC in one rotation of the in-plane field. If a domain $D'00'$ is so moved, and if the domain D_i of the associated domain—no domain pair, of registers 123 and 124, occupies the position C previously shown

occupied by absent domain $\bar{D}_i$ in FIG. 15, assumed to be the new condition, an interaction will occur between domains $D'00'$ and D_i .

The detailed operation of the interaction can be demonstrated if we assume the presence

of a domain $D'00'$ in section II for movement along register '0—0'. A compressor, it is recalled, is entirely occupied by domains (see the circles in '0—0' of FIG. 15). When a domain enters a compressor, the information represented by it appears at the terminal stage within one cycle of the in-plane field. We can assume, accordingly, that domain $D'00'$ in FIG. 15 occupies the position shown adjacent decision point DPC when the in-plane field is directed upward as indicated by the arrow H in the figure.

When the field next rotates 180 degrees to a downward position as viewed in FIG. 16, domain $D'00'$ moves to position P1 of deci-

sion point DPC. Absent domain $\bar{D}_i$ of FIG. 15 is moved downward to position e at this time and a domain D_i , associated with the line the condition of which is represented by $D'00'$, is moved to position a . The decision point is shown expanded in FIG. 16 to illustrate more clearly the magnetic condition when the field is directed downward as indicated by the arrow H in the figure.

When the in-plane field rotates 90 degrees further to a leftward orientation, domain $D'00'$ and domain D_i move to positions P2 and b of FIG. 16 respectively. As the in-plane field rotates further, however, domain interaction forces domains $D'00'$ and D_i to follow the paths P2', P3', P4', P5' and b , c , d , e , respectively. The former becomes an output at 122 while the latter becomes an input to compressor 125.

The position occupied by the domain D_i of the domain—no domain pair, associated with the line the condition of which was represented by domain $D'00'$ of FIGS. 15 and 16, is now switched via the compressor to its alternative position occupied by domain D_i in FIG. 15. The arrangement, accordingly, will now respond only to a persistent off-hook indication (viz., a domain in register '1—1') for that line, at which time this procedure is reversed.

Of course, if a domain $D'00'$ advances in register '0—0' at a time when a domain D_i of FIG. 16 is absent, no interaction occurs, no output appears, and the domain $D'00'$ advances along path P1, P2, P3, P4, and P5 to an annihilator E4 shown in FIG. 15. If, on the other hand, no domain $D'00'$ is advanced and a domain D_i is present, again no interaction occurs, no output occurs, and domain D_i follows the path a , b , c , d , e , and f in FIG. 16.

It is helpful to recapitulate that operation in terms of the line diagram of FIG. 13 and to represent the various functions performed by conventional symbols in the scanning art. Once this is accomplished, a truth diagram and a flow diagram of that operation can be established.

Consider the function of section III of

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FIG. 13. The two registers 123 and 124, each, have n stages associated with the n lines scanned. A domain is stored in only one of the like stages of registers 123 and 124 associated with each of the lines. That domain indicates the last condition which persisted for two scan periods for the associated line.

Section I of FIG. 13 functions to store the set of line conditions during a given scan period. Section II function to store the line conditions of section I which are advanced to it prior to a subsequent scan period.

A logic operation occurs between consecutive representations of line conditions for each line as the information is advanced. This logic operation generates a domain for movement into section III of FIG. 13 only when a like (persistent) condition is identified for a particular line for two consecutive scan periods. Two kinds of like conditions are identified. The first comprises off-hook indications in two consecutive scan periods. This persistent condition is represented by a domain in register 1—1 in section II of FIG. 13. The second comprises on-hook conditions for a particular line for two consecutive scan periods. This is represented by a domain in register 0—0 in section II of FIG. 13.

The domains representing the persistent condition, in each instance, are applied to section III of FIGS. 13 and 15 at the intersection points DPC where the representation is compared with the associated information in registers 123 or 124. When a match occurs (viz., a domain in register 1—1 and a domain in register 123 in the associated position) a change in the persistent condition for a line is indicated. Consequently, an output occurs and the domain in register 123 is moved to its complementary position in register 124.

It is clear then that a persistent condition provides an output and updates or "corrects" the position of the domain in register 123 to the associated position in register 124. Therefore, a domain in a position in register 124 indicates the last persistent condition for the associated line which produced an output—the "previous" (persistent) state (store) PS for that line.

Section I of FIG. 13 can be thought of as a present look store PL and section II can be thought of as the last look store LL

as stated hereinbefore. The fact that a complementary representation is employed introduces a complication in the notation. Consider only the arrangement to the right of vertical line 11 in FIG. 13—section I is designated PL and section II is designated LL. To the left of line 111, the complementary

arrangement is designated $\overline{\text{PL}}$ and $\overline{\text{LL}}$. In section II of the arrangement, the described operation indicates that the opposite station is in order. That is, that register 124 to the left of line III should be designated PS (previous store) since it records the last persistent conditions in register 1—1 whereas

register 123 should be designated $\overline{\text{PS}}$ similarly.

The operation of section III may be understood in these terms simply as a comparison of each persistent indication in a register LL with the complement (in register 123) of the previous persistent condition for a given line. This comparison occurs at DPC in FIG. 15 and results not only in an output indicative of a change in persistent condition but in updating of the previous persistent condition indication, designation CLL (for Corrected Last Look) herein, which entails the movement of a domain from register 123 to the associated position in register 124.

Section III of FIG. 13, at this juncture, indicates that the last persistent signal for the line of interest was a persistent off-hook signal and that the arrangement will next provide a signal (at 122) for that line only when a persistent on-hook signal next appears for that line on register 0—0 for comparison.

We can represent the overall operation of the arrangement of FIG. 13 by the flow diagram of FIG. 17 familiar in the scanning art. The transfer of a domain between registers 123 and 124 was designated CLL. All described logic operations are represented by a block entitled "scan logic" from which the outputs appear. Sections I, II, and III of FIG. 13 are represented in FIG. 17 by blocks entitled "present look", "last look" and "previous state" registers with information flowing between the blocks as indicated by the arrows.

In this context, the table below summarizes the described operation in terms familiar in the art.

Time	PL	LL	PS	CLL	State (Persistent)	Change of State
On-hook	0	0	0	0	0	0
Δ to off-hook	1	0	0	0	0	0
	1	1	0	1	1	1
	1	1	1	1	1	0
Δ to on-hook	0	1	1	1	1	0
	0	0	1	0	0	1
	0	1	0	0	0	0
Δ to off-hook	1	0	1	1	1	0

The table follows directly from a recognition that the organization to the right of line III in FIG. 13 operates as the present look store PL, last look store LL, and the com-

plement of the previous state PS for sections I, II, and III as shown in the figure, whereas to the left of line III the organization operates as the complement of the present store

PL, the complement of the last look LL, and the previous state PS. The table omits

redundant information PL, LL, PS, et cetera because the values would be opposite to those of PL, LL, and PS shown. If we read across the top line of the table, for example, a zero in both the PL and LL columns indicates the absence of a domain in the 1-1 register of FIG. 13.

A zero in the PS column signifies a domain in register 123 of FIG. 13. Under these conditions, there is no updating of registers 123 and 124, which means CLL is zero, the persistent state of the line represented is zero, and (a zero in the change of state column indicates) that no signal is provided at 121 in FIG. 13.

An off-hook condition is next initiated as represented in the second line of the table by the "1" in the PL column. During the next scan, the "1" persists in the PL column and appears also in the LL column as shown in the third line of the table. A correction of the PS registers (123 and 124) occurs at this juncture, the persistent state of the line is changed, and an output occurs. These results are indicated in the third line of the table by a "1" in each of the columns CLL, STATE, and CHANGE OF STATE. Similar changes occur as shown in the table in response to further changes in line condition

to on-hook and then to off-hook conditions as indicated to the left of the table.

A decision point of FIG. 14 between present and last look stores operates to pass a domain to an annihilator for extinction. This need not be the case. Alternatively, recirculating channels may be defined by overlay elements to connect the positions occupied by annihilators E1 and E2 and generator G in FIG. 14. In this instance, neither the annihilators nor the generator are employed and domains are merely recirculated. The complementary organization of the scanner is particularly well suited for such operation.

It may be recognized further that changes in line conditions (0-1 or 1-0) are indicated by domains being annihilated at E2 or E1 respectively. Detectors at these positions instead of annihilators would, of course, register these changes. However, spurious signals also generate such change indications and the illustrative circuit is designed to ignore them.

The various overlay geometries for achieving the functions organized to implement the scanner operations are familiar in the art. For example, the propagation of and interaction between domains via T and bar-shaped overlays are well understood. Also, domain generation, annihilation, and domain detection, as would occur at 121 or 122, are well known. Accordingly, the overlay geometry has only been discussed generally.

Similarly, an in-plane field source, a bias field source for generating a bias field to constrict domains, and a source of periodic scan pulses for achieving the operation described, as well as utilization circuitry are well understood in the art and are not described in detail but merely represented in FIG. 13 by blocks 140, 141, 142, and 143, respectively.

The various circuits operate under the control of a control circuit 145.

It may be recognized that the circuit of FIG. 15 is initialized by filling the compressors '0-0', '1-1' and 125 and one of the registers 123 or 124 with domains. Normal scan operations as described will result in the filling of registers '1-1' and '0-0', although no outputs occur at 121 or 122 of FIG. 13 until the registers are filled. Scan operations occur at a relatively fast rate (millisecond rate) and, therefore, the lack of outputs for a few scan operations is a negligible inconvenience at worst.

Registers 125 and 124 are not filled in this manner. A temporary domain generator of the type G shown in FIG. 13 may be employed during manufacture to fill register 124 in conventional fashion, however. As this is being done, consecutive domains generated at G of FIG. 13 and advanced in the complementary side of the arrangement fills compressor 125 and register '0-0' in a number of in-plane field rotations equal to the combined number of stages in register '0-0' and compressor 125 or n , whichever is greater. The temporary generator may be removed or left in situ but deactivated by known techniques. Thereafter, normal operation will result in the filling of register '1-1' with the possibility of spurious outputs on 122 during the first few scan cycles.

It is contemplated that similar arrangements can be achieved with other than magnetic domain techniques. For example, the various functions described in connection with FIGS. 14 and 15 can be achieved with integrated circuits employing AND gates at input, interaction, and output points. Similarly, semiconductor charge couple or charge transfer devices could be employed to this end as long as means were incorporated to periodically refurbish the information.

WHAT WE CLAIM IS:—

1. A memory device in which data bits can be represented by physical manifestations which exert a mutual influence on each other when they are proximate each other, said device including a first channel for carrying a sequence of data bits, a second channel for carrying a sequence of interrogation bits into proximity with said data bits, means for providing a said interrogation bit for each said data bit, means for synchronously moving said data bits and said interrogation bits along their respective channels, and means for providing an output signal dependent upon the mutual influence, if any, between each said data bit and its corresponding interrogation bit when they are proximate each other.

2. A device as claimed in claim 1 wherein said channels are defined in a sheet of material in which single wall magnetic domains can be moved, and said means for moving includes

a magnetically soft overlay adjacent a surface of said data bits and said interrogation bits comprising the presence and absence, as appropriate, of single wall domain in said material.

3. A device as claimed in claim 2 wherein said means for providing an output signal includes first means operative in response to the presence of an interrogation bit domain and the absence of a corresponding data bit domain for providing a first signal, and second means operative in response to the absence of an interrogation bit domain and the presence of a corresponding data bit domain for providing a second signal.

4. A device as claimed in claim 3 wherein said means for providing an output signal is operative in response to the presence of an interrogation bit domain and a corresponding data bit domain for inhibiting provision of said first and second signals.

5. A device as claimed in any one preceding claim includes means for providing substitution bits concurrently with said interrogation bits, and means for substituting each substitution bit in the place of the data bit corresponding thereto.

6. A device as claimed in claim 5 including means for selectively inhibiting substitution of said substitution bits.

7. A device as claimed in claim 6 wherein said selective inhibiting means includes means for providing auxiliary bits each corresponding with a respective one of said interrogation bits, means for comparing corresponding ones of said auxiliary and substitution bits, and means responsive to a predetermined comparison between a said auxiliary bit and its corresponding substitution bit for extinguishing the compared substitution bit.

8. A device as claimed in any one preceding claim and adapted to provide signals representative of changes in detected line conditions of a plurality of telephone stations, said data bits each representative of the detected line conditions of each of said stations, and said means for providing interrogation bits being adapted to provide interrogation bits representative of subsequently detected line conditions of each of said stations.

9. A device as claimed in claim 8 including a plurality of closed loop channels for carrying data bits, and a loop readout means in each said loop channel for providing an output signal representative of the data bit at said readout means, said means for moving being adapted to move all said data bits around their respective closed loop channels in synchronism.

10. A device as claimed in claim 1 wherein said channels are defined in a sheet of material in which single wall magnetic domains can be moved, and said means for moving includes a magnetically soft overlay adjacent a sur-

The various circuits operate under the control of a control circuit 145.

It may be recognized that the circuit of FIG. 15 is initialized by filling the compressors '0-0', '1-1' and 125 and one of the registers 123 or 124 with domains. Normal scan operations as described will result in the filling of registers '1-1' and '0-0', although no outputs occur at 121 or 122 of FIG. 13 until the registers are filled. Scan operations occur at a relatively fast rate (millisecond rate) and, therefore, the lack of outputs for a few scan operations is a negligible inconvenience at worst.

Registers 125 and 124 are not filled in this manner. A temporary domain generator of the type G shown in FIG. 13 may be employed during manufacture to fill register 124 in conventional fashion, however. As this is being done, consecutive domains generated at G of FIG. 13 and advanced in the complementary side of the arrangement fills compressor 125 and register '0-0' in a number of in-plane field rotations equal to the combined number of stages in register '0-0' and compressor 125 or n , whichever is greater. The temporary generator may be removed or left in situ but deactivated by known techniques. Thereafter, normal operation will result in the filling of register '1-1' with the possibility of spurious outputs on 122 during the first few scan cycles.

It is contemplated that similar arrangements can be achieved with other than magnetic domain techniques. For example, the various functions described in connection with FIGS. 14 and 15 can be achieved with integrated circuits employing AND gates at input, interaction, and output points. Similarly, semiconductor charge couple or charge transfer devices could be employed to this end as long as means were incorporated to periodically refurbish the information.

WHAT WE CLAIM IS:—

1. A memory device in which data bits can be represented by physical manifestations which exert a mutual influence on each other when they are proximate each other, said device including a first channel for carrying a sequence of data bits, a second channel for carrying a sequence of interrogation bits into proximity with said data bits, means for providing a said interrogation bit for each said data bit, means for synchronously moving said data bits and said interrogation bits along their respective channels, and means for providing an output signal dependent upon the mutual influence, if any, between each said data bit and its corresponding interrogation bit when they are proximate each other.

2. A device as claimed in claim 1 wherein said channels are defined in a sheet of material in which single wall magnetic domains can be moved, and said means for moving includes

a magnetically soft overlay adjacent a surface of said data bits and said interrogation bits comprising the presence and absence, as appropriate, of single wall domain in said material.

3. A device as claimed in claim 2 wherein said means for providing an output signal includes first means operative in response to the presence of an interrogation bit domain and the absence of a corresponding data bit domain for providing a first signal, and second means operative in response to the absence of an interrogation bit domain and the presence of a corresponding data bit domain for providing a second signal.

4. A device as claimed in claim 3 wherein said means for providing an output signal is operative in response to the presence of an interrogation bit domain and a corresponding data bit domain for inhibiting provision of said first and second signals.

5. A device as claimed in any one preceding claim includes means for providing substitution bits concurrently with said interrogation bits, and means for substituting each substitution bit in the place of the data bit corresponding thereto.

6. A device as claimed in claim 5 including means for selectively inhibiting substitution of said substitution bits.

7. A device as claimed in claim 6 wherein said selective inhibiting means includes means for providing auxiliary bits each corresponding with a respective one of said interrogation bits, means for comparing corresponding ones of said auxiliary and substitution bits, and means responsive to a predetermined comparison between a said auxiliary bit and its corresponding substitution bit for extinguishing the compared substitution bit.

8. A device as claimed in any one preceding claim and adapted to provide signals representative of changes in detected line conditions of a plurality of telephone stations, said data bits each representative of the detected line conditions of each of said stations, and said means for providing interrogation bits being adapted to provide interrogation bits representative of subsequently detected line conditions of each of said stations.

9. A device as claimed in claim 8 including a plurality of closed loop channels for carrying data bits, and a loop readout means in each said loop channel for providing an output signal representative of the data bit at said readout means, said means for moving being adapted to move all said data bits around their respective closed loop channels in synchronism.

10. A device as claimed in claim 1 wherein said channels are defined in a sheet of material in which single wall magnetic domains can be moved, and said means for moving includes a magnetically soft overlay adjacent a sur-



face of said sheet, said overlay defining said first channel and being for moving single wall domains therealong in response to a magnetic field the direction of which in the plane of said sheet changes, said overlay being such that said first channel folds back upon itself forming first, second, and third sections in such manner that said second section provides a domain to said third section only when a domain is present in like stages of said first and second sections, said data bits and said interrogation bits comprising the presence and absence, as appropriate, of single wall domains in said material.

11. A device as claimed in claim 10 wherein said first and second sections have the same number of stages.

12. A device as claimed in claim 11 wherein said overlay also defines a further channel like said first channel for synchronous operation therewith in response to said magnetic field.

13. A device as claimed in claim 12 adapted to provide in the first section of each of said first and further channels first and second complementary domain patterns representative of the presence and absence of signals on a plurality of scanned lines.

14. A device as claimed in claim 12 or 13 including first and second domain extinguishers at the end of said second sections of said first and further channels respectively.

15. A device as claimed in claim 14 wherein said third sections of said first and further

channels each include an output position, and said overlay defines adjacent each said output position a respective said second channel in the form of a closed loop each said second channel having the same number of stages as said number for recirculating single wall domains in response to said magnetic field, and further defines a compressor register including a first stage of each of said second channels for transferring a domain between said second channels.

16. A device as claimed in claim 15 wherein said overlay at the end of each of said third sections is such as to move a domain to a domain extinguisher in the absence of a domain in the first stage of the respective second channel, and to move a domain in said third section to the corresponding output position in the presence of a domain in that first stage.

17. A memory device arranged and adapted to operate substantially as herein described with reference to FIGS. 1 to 12 of the accompanying drawing.

18. A memory device arranged and adapted to operate substantially as herein described with reference to FIGS. 13 to 17 of the accompanying drawing.

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