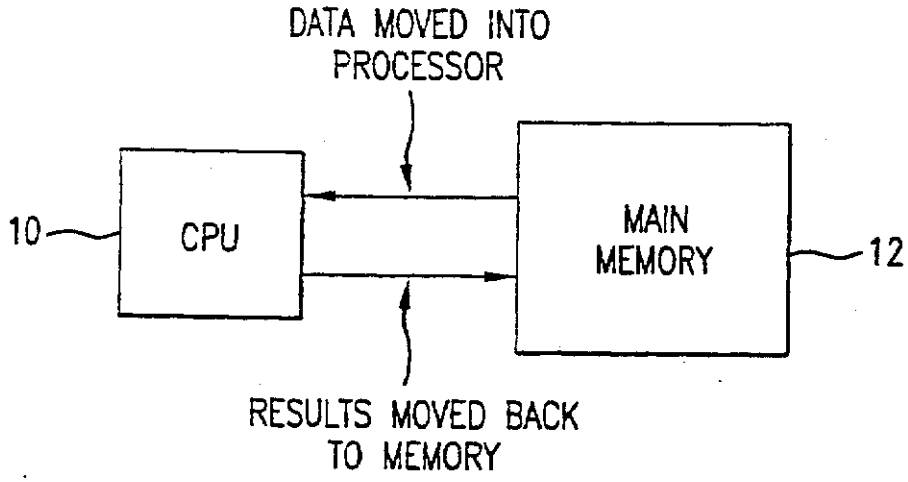


FIG. 1
PRIOR ART

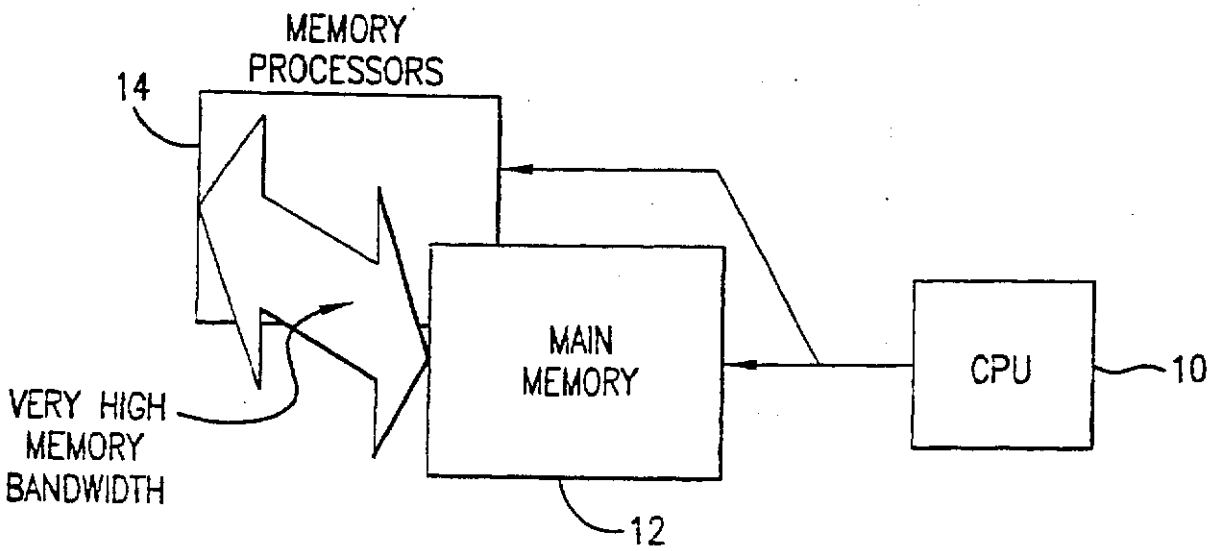


FIG. 2
PRIOR ART

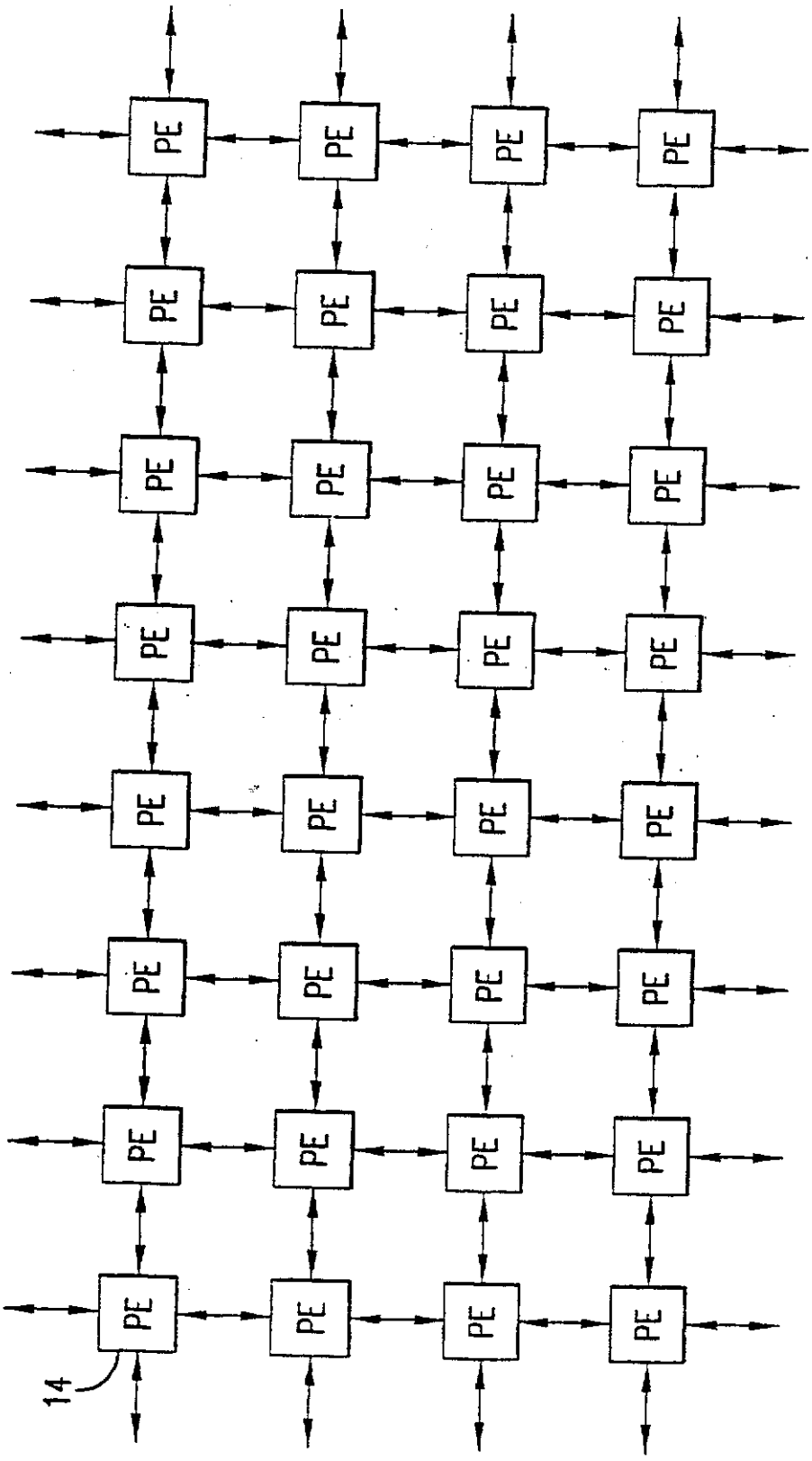


FIG. 3
PRIOR ART

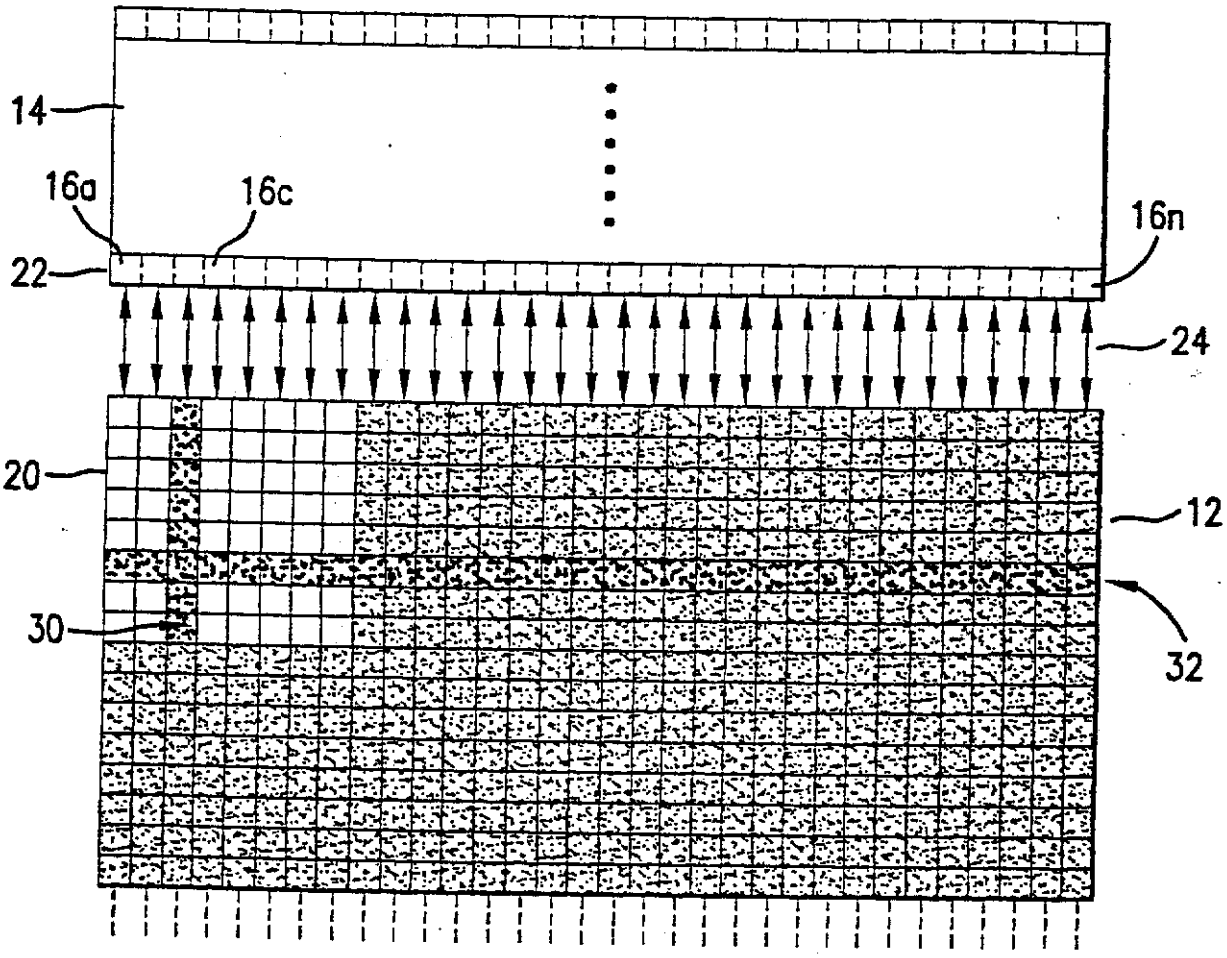


FIG. 4

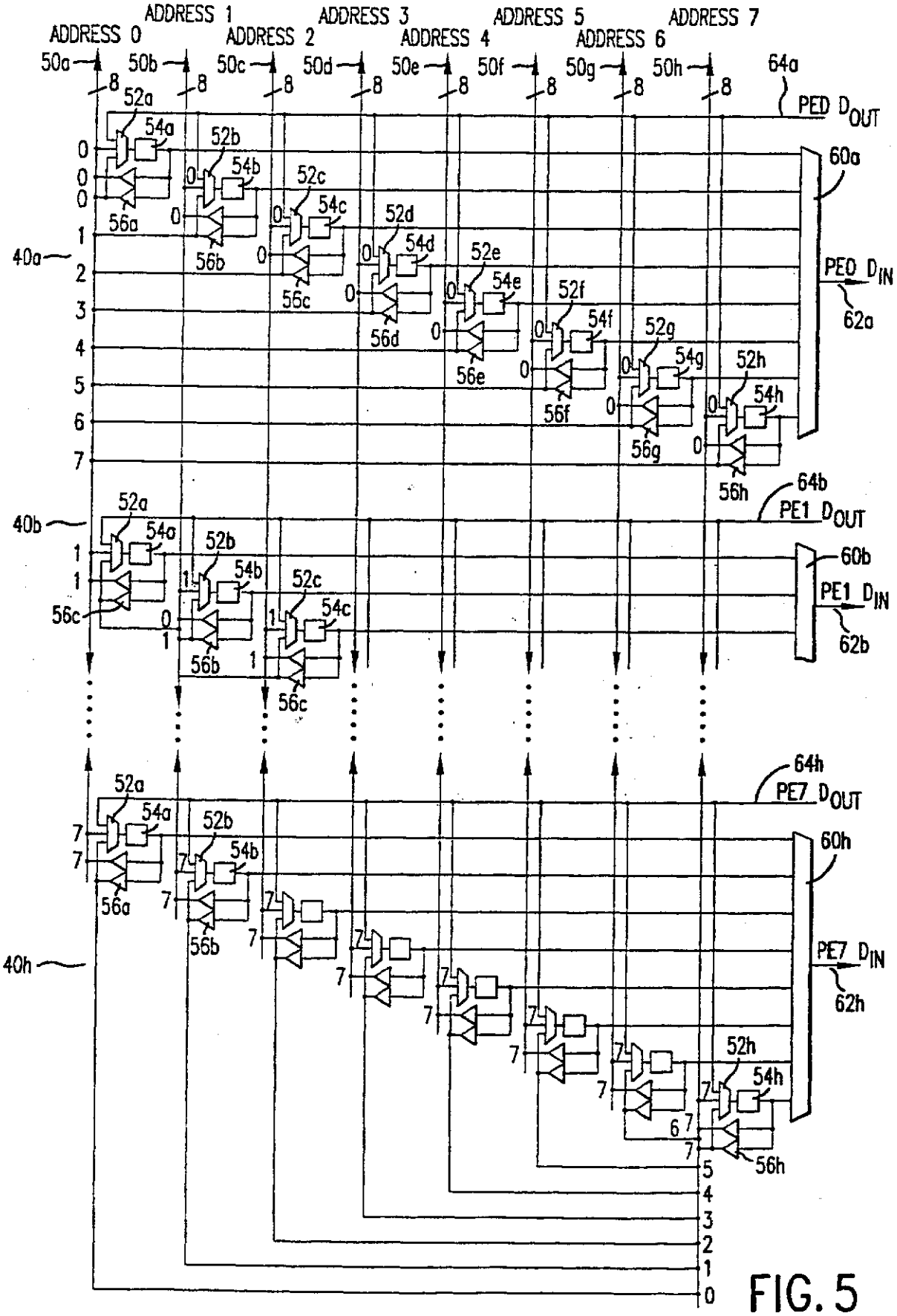

ADDRESS 0
ADDRESS 1
ADDRESS 2
ADDRESS 3
ADDRESS 4
ADDRESS 5
ADDRESS 6
ADDRESS 7
50a
50b
50c
50d
50e
50f
50g
50h
64a
PE0 D_{OUT}
60a
PE0 D_{IN}
62a
40a
40b
40h
52a
54a
52b
54b
52c
54c
52d
54d
52e
54e
52f
54f
52g
54g
52h
54h
56a
56b
56c
56d
56e
56f
56g
56h
64b
PE1 D_{OUT}
60b
PE1 D_{IN}
62b
64h
PE7 D_{OUT}
60h
PE7 D_{IN}
62h

FIG. 5

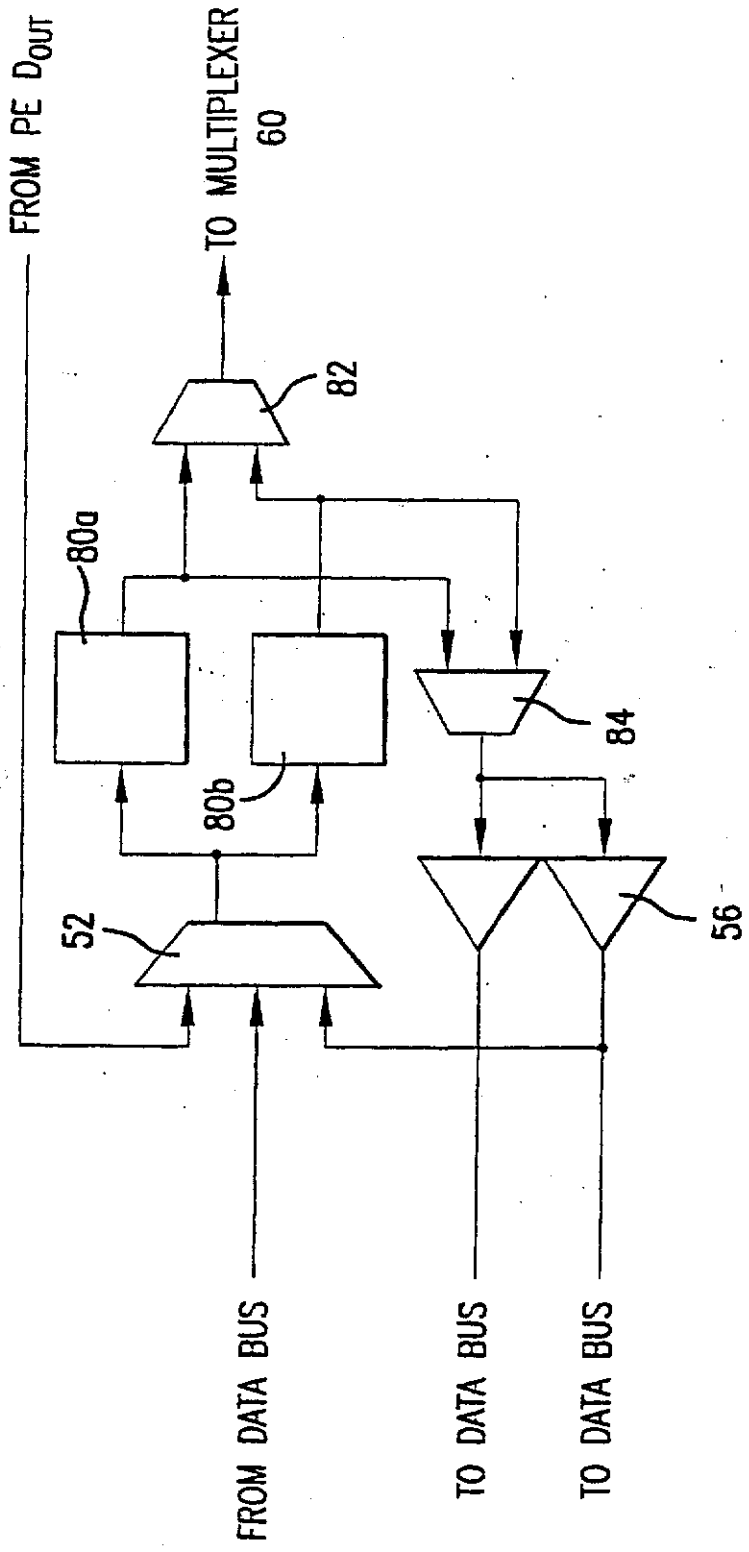

FROM PE D_{OUT}
TO MULTIPLEXER 60
82
80a
80b
84
52
56
FROM DATA BUS
TO DATA BUS
TO DATA BUS

FIG. 6

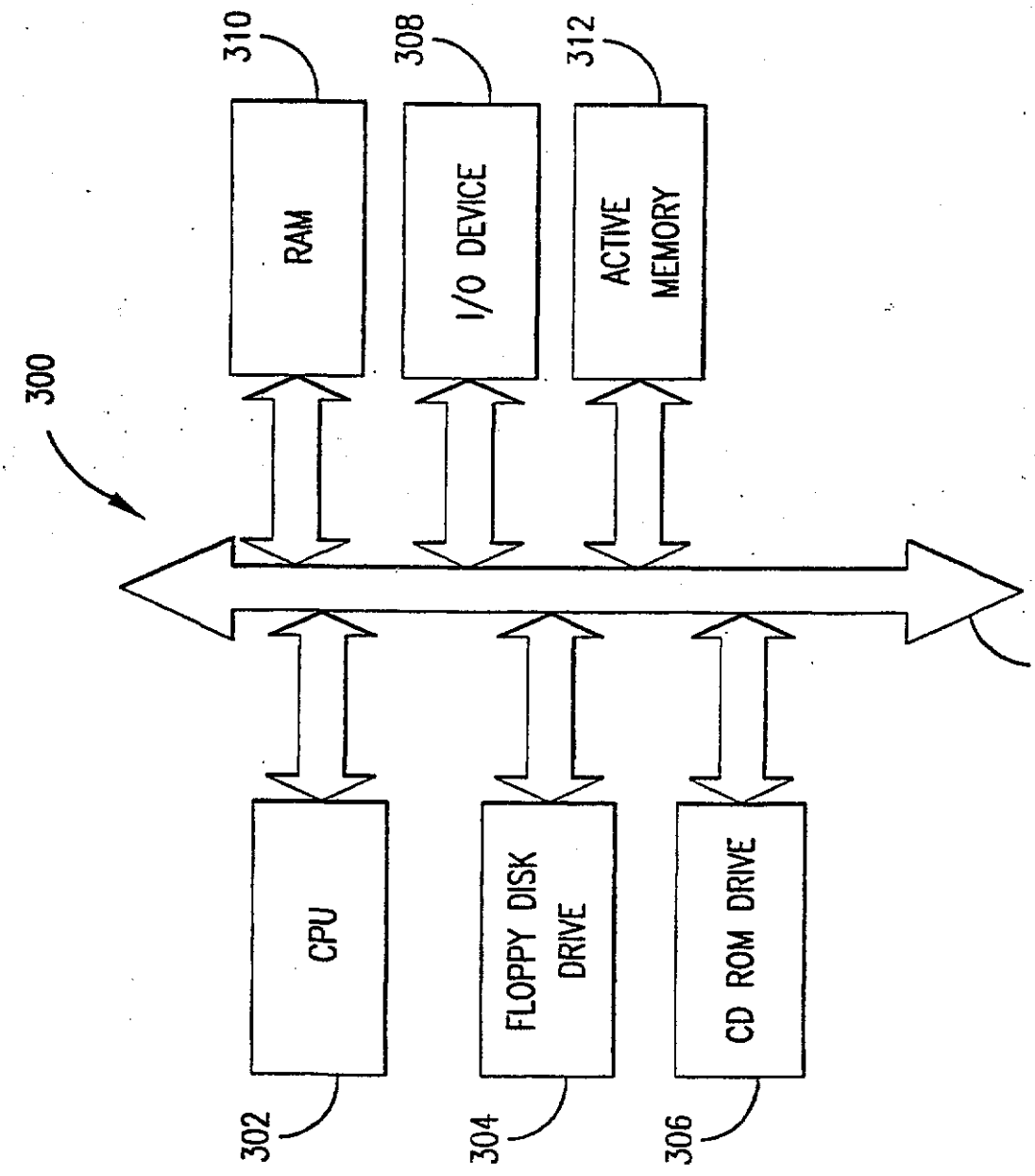

300
310
RAM
308
I/O DEVICE
312
ACTIVE MEMORY
320
302
CPU
304
FLOPPY DISK DRIVE
306
CD ROM DRIVE

FIG. 7