METHOD OF FABRICATING A STACKED POLY-POLY AND MOS CAPACITOR USING A SiGe INTEGRATION SCHEME

ABSTRACT

A stacked Poly-Poly/MOS capacitor useful as a component in a BiCMOS device comprising a semiconductor substrate (10) having a region of a first conductivity-type (12) formed in a surface thereof; a gate oxide (16) formed on said semiconductor substrate (10) overlaying said region of first conductivity-type (12); a first polysilicon layer (18) being doped with an N or P-type dopant; a dielectric layer (20) formed on said first polysilicon layer (18); and a second polysilicon layer (22) formed on said dielectric layer (20), said second polysilicon layer (22) being doped with the same or different dopant as the first polysilicon layer (18).

Fig. 4