CLAIMS

1. A semiconductor device comprising:

a first conductor;

a metal oxide over the first conductor;

a second conductor over the metal oxide;

a first insulator;

a second insulator over the first insulator; and

a third conductor over the second insulator,

wherein the metal oxide comprises a region overlapping with the first conductor,

wherein the metal oxide comprises a first opening;

wherein the second conductor comprises a second opening;

wherein the first opening and the second opening overlap with each other,

wherein the first insulator is on an inner side of each of the first opening and the second opening,

wherein the second insulator is in a depressed portion of the first insulator, and

wherein the third conductor is in a depressed portion of the second insulator.

2. The semiconductor device according to claim 1,

wherein the metal oxide and the second conductor each have a hollow cylindrical shape.

3. The semiconductor device according to claim 2,

wherein a center of the first conductor is not aligned with a center of the hollow cylindrical shape of the metal oxide in a top view.

4. The semiconductor device according to claim 1,

wherein a side surface of the first opening and a side surface of the second opening each have a tapered shape in a cross-sectional view.

5. The semiconductor device according to claim 1,

wherein an uppermost portion of the second insulator is level or substantially level with an uppermost portion of the first insulator.

6. The semiconductor device according to claim 1,

wherein the first insulator comprises a region having a smaller thickness than the second insulator.

7. A storage device comprising the semiconductor device according to claim 1, and a capacitor,

wherein the semiconductor device is above the capacitor.

8. A semiconductor device comprising:

a first insulator;

a first conductor embedded in the first insulator;

a metal oxide over the first conductor;

a second conductor over the metal oxide;

a third conductor over the second conductor;

a second insulator;

a third insulator over the second insulator;

a fourth conductor over the third insulator; and

a fifth conductor over the fourth conductor,

wherein the metal oxide comprises a region overlapping with the first conductor,

wherein the metal oxide comprises a first opening;

wherein the second conductor comprises a second opening;

wherein the first opening and the second opening overlap with each other,

wherein the second insulator is on an inner side of each of the first opening and the second opening,

wherein the third insulator is in a depressed portion of the second insulator,

wherein the fourth conductor is in a depressed portion of the third insulator,

wherein the third conductor is in contact with at least part of a top surface of the second conductor,

wherein the fifth conductor is in contact with a top surface of the fourth conductor, and

wherein the third conductor and the fifth conductor do not overlap with each other in a top view.

9. The semiconductor device according to claim 8,

wherein a fourth insulator is between the second insulator and the fifth conductor and between the third insulator and the fifth conductor,

wherein the fourth insulator comprises a region in contact with a bottom surface of the fifth conductor, and

wherein a top surface of the third conductor is between a bottom surface and a top surface of the fourth insulator.

10. The semiconductor device according to claim 8,

wherein the metal oxide and the second conductor each have a hollow cylindrical shape.

11. The semiconductor device according to claim 10,

wherein a center of the first conductor is not aligned with a center of the hollow cylindrical shape of the metal oxide in a top view.

12. The semiconductor device according to claim 8,

wherein a side surface of the first opening and a side surface of the second opening each have a tapered shape in a cross-sectional view.

13. The semiconductor device according to claim 8,

wherein an uppermost portion of the third insulator is level or substantially level with an uppermost portion of the second insulator.

14. The semiconductor device according to claim 8,

wherein the second insulator comprises a region having a smaller thickness than the third insulator.

15. The semiconductor device according to claim 8,

wherein a direction in which the fifth conductor extends is orthogonal to a direction in which the third conductor extends.

16. A storage device comprising the semiconductor device according to claim 8, and a capacitor,

wherein the semiconductor device is above the capacitor.