METHODS OF FORMING A PLURALITY OF CAPACITORS

TECHNICAL FIELD

Embodiments disclosed herein pertain to methods of forming a plurality of capacitors.

BACKGROUND

Capacitors are one type of component commonly used in the fabrication of integrated circuits, for example in DRAM circuitry. A capacitor is comprised of two conductive electrodes separated by a non-conducting dielectric region. As integrated circuitry density has increased, there is a continuing challenge to maintain sufficiently high storage capacitance despite typical decreasing capacitor area. The increase in density of integrated circuitry has typically resulted in greater reduction in the horizontal dimension of capacitors as compared to the vertical dimension. In many instances, the vertical dimension of capacitors has increased.

One manner of fabricating capacitors is to initially form an insulative material within which a capacitor storage node electrode is formed. For example, an array of capacitor electrode openings for individual capacitors may be fabricated in such insulative capacitor electrode-forming material, with an example insulative electrode-forming material being silicon dioxide doped with one or both of phosphorus and boron. The capacitor electrode openings may be formed by etching. It can be difficult to etch the capacitor electrode openings within the insulative material, particularly where the openings are deep.

Further and regardless, it is often desirable to etch away most if not all of the capacitor electrode-forming material after individual capacitor electrodes have been formed within the openings. Such enables outer sidewall surfaces of the electrodes to provide increased area and thereby increased capacitance for the capacitors being formed. However, the capacitor electrodes formed in deep openings are often correspondingly much taller than they are wide. This can lead to toppling of the capacitor electrodes, either during the etch to expose the outer sidewalls surfaces, during transport of the substrate, and/or during deposition of the capacitor dielectric layer or outer capacitor electrode layer.

Our U.S. Patent No. 6,667,502 teaches the provision of a brace or retaining structure intended to alleviate such toppling. Other aspects associated in the formation of a plurality of capacitors, some of which include bracing structures, are also disclosed and are:

U.S. Published Application No. 2005/0051822;
U.S. Published Application No. 2005/0054159;
U.S. Published Application No. 2005/0158949;
U.S. Published Application No. 2005/0287780;
U.S. Published Application No. 2006/0014344;
U.S. Published Application No. 2006/0051918;
U.S. Published Application No. 2006/0046420;
U.S. Published Application No. 2006/0121672;
U.S. Published Application No. 2006/0211211;
U.S. Published Application No. 2006/0263968;
U.S. Published Application No. 2006/0261440;
U.S. Published Application No. 2007/0032014;
U.S. Published Application No. 2006/0063344;
U.S. Published Application No. 2006/0063345;

Fabrication of capacitors in memory circuitry may form an array of capacitors within a capacitor array area. Control or other circuitry area is often displaced from the capacitor array area, with the substrate including an intervening area between the capacitor array area and the control or other circuitry area. In some instances, a trench is formed in the intervening area between the capacitor array area and the other circuitry area. Such trench can be formed commensurate with the fabrication of the openings within the capacitor array area within which the isolated capacitor electrodes will be received.

BRIEF DESCRIPTION OF THE DRAWINGS

Fig. 1 is a diagrammatic top plan view of substrate fragment in process in accordance with an embodiment of the invention.

Fig. 2 is an enlarged diagrammatic top plan view of a small portion of the Fig. 1 substrate fragment.

Fig. 3 is a section view taken through line 3-3 in Fig. 2.

Fig. 4 is a diagrammatic top plan view of the substrate fragment of Fig. 2 at a processing step subsequent to that shown by Fig. 2.

Fig. 5 is a section view taken through line 5-5 in Fig. 4.

Fig. 6 is a diagrammatic top plan view of the substrate fragment of Fig. 4 at a processing step subsequent to that shown by Fig. 4.

Fig. 7 is a section view taken through line 7-7 in Fig. 6.

Fig. 8 is a diagrammatic top plan view of the substrate fragment of Fig. 6 at a processing step subsequent to that shown by Fig. 6.

Fig. 9 is a section view taken through line 9-9 in Fig. 8.

Fig. 10 is a section view taken through line 10-10 in Fig. 8.

Fig. 11 is a diagrammatic top plan view of the substrate fragment of Fig. 8 at a processing step subsequent to that shown by Fig. 8.

Fig. 12 is a section view taken through line 12-12 in Fig. 11.

Fig. 13 is a section view taken through line 13-13 in Fig. 11.

Fig. 14 is a section view taken through line 14-14 in Fig. 11.

Fig. 15 is a diagrammatic top plan view of the substrate fragment of Fig. 11 at a processing step subsequent to that shown by Fig. 11.

Fig. 16 is a section view taken through line 16-16 in Fig. 15.

Fig. 17 is a section view taken through line 17-17 in Fig. 15.

Fig. 18 is a view of the Fig. 16 substrate fragment subsequent to that shown by Fig. 16.

Fig. 19 is a view of the Fig. 17 substrate fragment subsequent to that shown by Fig. 17.

Fig. 20 is a diagrammatic top plan view of the substrate fragment of Fig. 15 at a processing step subsequent to that shown by Figs. 18 and 19.

Fig. 21 is a section view taken through line 21-21 in Fig. 20.

Fig. 22 is a section view taken through line 22-22 in Fig. 20.

Fig. 23 is a section view taken through line 23-23 in Fig. 20.

Fig. 24 is a diagrammatic top plan view of the substrate fragment of Fig. 20 at a processing step subsequent to that shown by Fig. 20.

Fig. 25 is a section view taken through line 25-25 in Fig. 24.

Fig. 26 is a section view taken through line 26-26 in Fig. 24.

Fig. 27 is a section view taken through line 27-27 in Fig. 24.

Fig. 28 is a diagrammatic top plan view of the substrate fragment of Fig. 24 at a processing step subsequent to that shown by Fig. 24.

Fig. 29 is a section view taken through line 29-29 in Fig. 28.

Fig. 30 is a section view taken through line 30-30 in Fig. 28.

Fig. 31 is a section view taken through line 31-31 in Fig. 28.

Fig. 32 is a diagrammatic view of a DRAM cell.

Fig. 33 is a diagrammatic top plan view of an alternate embodiment substrate fragment in process in accordance with an embodiment of the invention.

Fig. 34 is a section view taken through line 34-34 in Fig. 33.

Fig. 35 is a diagrammatic top plan view of the substrate fragment of Fig. 33 at a processing step subsequent to that shown by Fig. 33.

Fig. 36 is a section view taken through line 36-36 in Fig. 35.

Fig. 37 is a section view taken through line 37-37 in Fig. 35.

Fig. 38 is a diagrammatic top plan view of the substrate fragment of Fig. 35 at a processing step subsequent to that shown by Fig. 35.

Fig. 39 is a section view taken through line 39-39 in Fig. 38.

Fig. 40 is a diagrammatic top plan view of the substrate fragment of Fig. 38 at a processing step subsequent to that shown by Fig. 38.

Fig. 41 is a section view taken through line 41-41 in Fig. 40.

Fig. 42 is a section view taken through line 42-42 in Fig. 40.

Fig. 43 is a section view taken through line 43-43 in Fig. 40.

Fig. 44 is a diagrammatic top plan view of an alternate embodiment substrate fragment in process in accordance with an embodiment of the invention.

Fig. 45 is a section view taken through line 45-45 in Fig. 44.

Fig. 46 is a diagrammatic top plan view of the substrate fragment of Fig. 44 at a processing step subsequent to that shown by Fig. 44.

Fig. 47 is a section view taken through line 47-47 in Fig. 46.

Fig. 48 is a section view taken through line 48-48 in Fig. 46.

Fig. 49 is a section view taken through line 49-49 in Fig. 46.

Fig. 50 is a diagrammatic top plan view of an alternate embodiment substrate fragment in process in accordance with an embodiment of the invention.

DETAILED DESCRIPTION OF EXAMPLE EMBODIMENTS

Example methods of forming pluralities of capacitors are described with reference to Figs. 1-50. Referring initially to Figs. 1-3, a substrate, for example a semiconductor substrate, is indicated generally with reference numeral 10. In the context of this document, the term "semiconductor substrate" or "semiconductive substrate" is defined to mean any construction comprising semiconductive material, including, but not limited to, bulk semiconductive materials such as a semiconductive wafer (either alone or in assemblies comprising other materials thereon), and semiconductive material layers (either alone or in assemblies comprising other materials). The term "substrate" refers to any supporting structure, including, but not limited to, the semiconductive substrates described above. Accordingly, and by way of example only, substrate 10 might comprise a bulk semiconductor material (not shown), for example bulk monocrystalline, and/or comprise semiconductor-on-insulator layers.

Substrate 10 can be considered as comprising a capacitor array area 625, a circuitry area 675 other than capacitor array area 625, and an intervening area 650 between capacitor array area 625 and circuitry area 675. In the depicted example embodiment, intervening area 650 completely surrounds and encircles capacitor array area 625 (Fig. 1), and circuitry area 675 comprises a peripheral circuitry area to that of capacitor array area 625. Alternate constructions are contemplated, of course, for example whereby neither intervening area 650 nor circuitry area 675 completely or partially encircles a capacitor array area 625.

Fig. 3 depicts an insulative material 12 having electrically conductive storage node pillars 14 formed there-through. Materials 12 and 14 may be fabricated over some suitable underlying material, for example bulk monocrystalline and/or underlying circuitry. Example insulative materials 12 include doped and undoped silicon dioxides, for example silicon dioxide deposited by the decomposition of tetraethylorthosilicate (TEOS) and/or borophosphosilicate glass (BPSG) and/or silicon nitride. Alternately by way of example only, material 12 might comprise anisotropically etched insulative sidewall spacers, for example formed about transistor gate lines (not shown). An example material 14 is conductively doped polysilicon. Conductive material 14 can be considered as comprising or defining a plurality of capacitor storage node locations/contacts on substrate 10, and which have been designated with

numerals 15, 16, 17, 18, 19, 20, 21, and 22 in three example rows in Fig. 4. Storage node contacts 15, 16, 17, 18, 19, 20, 21, and 22 are examples only and, regardless, may be conductive at this point in the process, or made conductive subsequently.

A first material 23 is formed over the array of storage node contacts, including over storage node contacts 15, 16, 17, 18, 19, 20, 21, and 22. Such may be homogenous or non-homogenous, for example comprising multiple different and/or alternating composition regions and/or layers. In the example embodiment, first material 23 is depicted as comprising materials 24, 25, 26, 27, 28 and 29. Example respective thicknesses for each are 275 Angstroms, 1,000 Angstroms, 10,000 Angstroms, 2,000 Angstroms, 10,000 Angstroms, and 3,000 Angstroms. Some or all of first material 23 may or may not remain as part of a finished circuitry construction incorporating the plurality of capacitors. Such may be insulative, conductive, or semiconductive. If insulative, example compositions for material 24 comprise silicon nitride and/or undoped silicon dioxide. Material 24 may be included to provide an etch stop, or other function. In one embodiment, materials 25, 27 and 29 are of the same composition, for example undoped silicon dioxide. In one embodiment, materials 26 and 28 are of the same composition, for example doped silicon dioxide such as borophosphosilicate glass, borosilicate glass, or phosphosilicate glass. In one example embodiment, first material 23 comprises at least first and second etchably different materials. In one example, and where materials 26 and 28 are the same composition, such can be considered as a first material which is etchably different from that of a second material comprised of the composition of the material 25, 27 and 29 (when such are of the same composition). Further, of course, fewer or more alternating or different composition layers could also of course be provided for material 23. Also, "first" and "second" are used for convenience only with respect to differentiating various materials, with such being interchangeable independent of order provided over the substrate and independent of whether other such materials are provided therebelow or thereover.

Referring to Figs. 2 and 3, a mask 30 has been formed over first material 23. An example for mask 30 includes 8,000 Angstroms of transparent carbon having a 320 Angstrom anti-reflective coating (i.e., DARC) deposited thereover.

An array of openings 32 has been formed in mask 30 (i.e., using photolithographic of other processing).

Referring to Figs. 4 and 5, an array of first openings 34 has been formed into first material 23 over the storage node contacts, for example using openings 32 (not shown) in mask 30 (not shown) and which has been subsequently removed. Individual of first openings 34 are formed over at least two of the storage node contacts. In one embodiment, individual of the first openings are formed over four or less of the storage node contacts, with the embodiments of Figs. 4 and 5 showing first openings 34 being individually formed over four, and only four, storage node contacts. In one embodiment, individual of first openings 34 are quadrilateral in shape in at least one horizontal cross section through the substrate, in one embodiment comprise parallelograms, and in one embodiment comprise rectangles, for example as shown. Other shapes and/or sub-plurality collections of storage node contacts are also of course contemplated. Further, first openings 34 may or may not extend entirely to the storage node contacts which such overlie at this point of processing. In the depicted example Figs. 4 and 5 embodiment, formation of first openings 34 may occur by using any suitable anisotropic etching chemistries to ultimately etch selectively to and stop upon material 24 as shown. In the context of this document, a selective etch defines an etch rate of one material relative another of at least 2:1. For purposes of the continuing discussion, individual first openings 34 can be considered as comprising surrounding sidewalls 35.

Referring to Figs. 6 and 7, masking material 36 has been deposited within first openings 34 and which is received over the storage node contacts within individual of such openings. An example masking material comprises polysilicon. Alternate example masking materials include carbon or other organic materials. Ideally, masking material 26 is capable of conformal deposition, for example at 70% to 100% step coverage. In the first depicted example embodiment, masking material 36 has been deposited to line surrounding first openings sidewalls 35 and to less than fill such first openings 34. In one example where the widest open dimension of first openings 34 are about 1,650 by 1900 Angstroms, an example deposition thickness for masking material 36 is 600 Angstroms to leave a center gap or open dimensions of about 450 Angstroms by 700 Angstroms. Figs. 6 and 7 depict such center volume as

having been subsequently filled with another material 37 (for example photoresist), with materials 36 and 37 then having been collectively planarized back at least to an outermost surface of first material 23. In one embodiment, the act of lining to form masking material 36 within first openings 34 is conducted to provide a lateral thickness of material 36 within first openings 34 which is no greater than forty percent of a minimum horizontal cross sectional open dimension at outermost portions of individual first openings 34 within first material 23.

Referring to Figs. 8-10, material 37 (not shown) has been removed, and second material 38 has been formed to within first openings 34 adjacent masking material 36. An example second material 38 is undoped silicon dioxide, for example deposited using tetraethyl orthosilicate. Example seams 39 from such deposition may or may not form. In one embodiment and as shown, second material 38 is deposited to be received elevationally over first material 23, for example by a thickness of about 500 Angstroms. Alternately by way of example only, such might not be provided to be received elevationally over any of first masking material 23. Further as an alternative in such instance, deposition of material 37 as shown in Figs. 6 and 7 might be eliminated, and substituted with deposition of example second material 38, followed by etch-back or planarize polishing of masking material 36 and second material 38 in a common etch-back or polishing step.

Further, a mask 40 has been formed as part of substrate 10. Mask 40 may be of the same composition as that of mask 30 described above. An array of second openings 42 has been formed as part of mask 40. Such are received partially over and partially offset from the array of first openings 34. Individual of second openings 42 are formed over at least two storage node contacts that are received under different and adjacent of first openings 34. In one embodiment, individual of the second openings are formed over four or less of the storage node contacts. In the depicted example embodiment, individual of second openings 42 are formed over four storage node contacts that are received under different and adjacent of first openings 34, with the overlapping portions of the first and second openings being received over the storage node contacts. In one embodiment, second openings 42 are individually quadrilateral in shape in at least one horizontal cross section, in one embodiment parallelogram in

shape in at least one horizontal cross section, and in one embodiment rectangular in shape in at least one horizontal cross section as is shown. In one embodiment, first openings 34 and second openings 42 are all of the same size and shape in at least one horizontal cross section, and regardless of whether such size and shape in at least one horizontal cross section is quadrilateral. If quadrilateral, the first and second openings might individually comprise parallelogram shapes in at least one horizontal cross section independent of whether all are of the same size and shape, with first openings 34 and second openings 42 in the depicted embodiment being of the same size and shape and being rectangular in at least one horizontal cross section.

Referring to Figs. 11-14, masking material 36 has been etched through second openings 42 in mask 40 to remove masking material 36 from being received over the storage node contacts within first openings 34. Ideally, such etching is conducted selectively relative to second material 38 and first material 23. Fig. 13 also depicts removal of material 24 subsequent to etching of masking material 36 effective to expose the depicted array of storage node contacts. Further, Figs. 11-14 depict material of mask 40 (not shown) outwardly of second material 38 as having been removed.

Referring to Figs. 15-17, conductive material 50 has been formed within first openings 34 in electrical connection with the respective storage node contacts, and comprise individual capacitor electrodes 52. By way of example only, an example material is titanium nitride. More than one conductive material might, of course, also be utilized, as well as materials other than titanium nitride. The depicted conductive material 50 has been etched back at least to first material 23 to form isolated individual capacitor electrodes 52. Such may also etch some of first material 23. Figs. 18 and 19 depict some subsequent removal of first masking material 23, and particularly some of material 29, to provide a more planar outer surface configuration relative material 29, if desired.

Individual capacitor electrodes 52 are ultimately incorporated into a plurality of capacitors. Such may comprise etching some or all of remaining of masking material 36 and/or some or all remaining of second material 38 from first openings 34. For example and with reference to Figs. 20-23, such depict etching of all remaining of masking material 36 (not shown) from first openings

34, and etching of all remaining of second material 38 (not shown) from first openings 34.

In one embodiment, some form of a lattice retaining structure might be formed to be received externally among the individual capacitor electrodes. For example and by way of example only, Figs. 24-27 depict but one example manner by which such a lattice retaining structure might be formed. Specifically, second etchably different material 26, 28 (not shown) has been etched selectively relative to first etchably different material 25, 27 and 29, thereby forming a lattice retaining structure 55 comprised of first etchably different material 25, 27, 29 that is received externally among individual capacitor electrodes 52.

Referring to Figs. 28-31, a capacitor dielectric 56 and a cell capacitor electrode 58 have been deposited as part of substrate 10. Example capacitor dielectric materials include one or more of silicon dioxide, silicon nitride, a composite of silicon dioxide and silicon nitride, or any suitable high k dielectric, and whether existing or yet-to-be developed. By way of example only, high k dielectrics include Ta_2O_5 and barium strontium titanate. An example outer capacitor electrode layer comprises conductively doped polysilicon. Such thereby defines individual capacitors 60. Such are depicted as comprising a common cell capacitor plate to all of the depicted capacitors, for example as might be utilized in DRAM or other circuitry. For example and by way of example only, Fig. 32 depicts an example DRAM cell incorporating a capacitor 60. Such comprises an example transistor gate word line 62 having insulative sidewall spacers, an insulative cap and a conductive region under the cap such as a silicide, a conductive polysilicon region under the silicide, and gate dielectric region under the polysilicon. Source/drain regions 64 are shown formed within semiconductive material operatively proximate word line 62. One of such electrically connects with capacitor 60, and another of such electrically connects with a bit line 66.

The above-described embodiments depict examples where deposition of masking material 36 to within first openings 34 only partially fills remaining volume of first openings 34, for example lining the depicted surrounding first opening sidewalls 35 with such masking material. However, embodiments of the invention also include forming masking material to completely fill such first

openings. For example, Figs. 33-43 depict such an alternate example embodiment with respect to a substrate fragment 10a. Like numerals from the first-described embodiments have been utilized where appropriate, with differences being indicated with the suffix "a" or with different numerals.

Referring to Figs. 33, 34, 35, 36 and 37, such correspond in sequence to the above-depicted Figs. 6, 7, 8, 9, and 10, respectively, of the first-described embodiment. Except here, masking material 36a has been deposited to completely fill first openings 34. Accordingly, there is no internal volume within which a second material 38 (not shown) is available for deposition.

Referring to Figs. 38 and 39, masking material 36a has been etched through second openings 42 in mask 40 to remove masking material 36a from being received over the respective storage node contacts within first openings 34. Figs. 38 and 39 correspond in sequence to those of Figs. 11 and 13, respectively.

Referring to Figs. 40-43, such correspond in sequence to those of Figs. 28-31, respectively, of the first-described embodiment. Accordingly, subsequent processing has been conducted to form individual capacitor electrodes 52, followed by removal of all remaining of masking material 36a (not shown) to ultimately form capacitors 60 essentially that same as in Figs. 28-31.

The above example embodiments depict implementations wherein conductive material 50 is deposited to form individual capacitor electrodes 52 to comprise singular, essentially fully solid, pillars. However, aspects of the invention also contemplate forming such conductive material to be deposited to form individual capacitor electrodes to comprise open container shapes, or other shapes. For example, Figs. 44 and 45 depict an alternate example substrate fragment 10b in comparison to substrate fragment 10a referred to above. Like numerals from the substrate 10a embodiment have been utilized where appropriate, with differences being indicated with the suffix "b" or with different numerals. Figs. 44 and 45 depict deposition of conductive material 50b to less than fill the void created by removal of masking material 36b over the individual storage node contacts. Figs. 46-49 depict subsequent corresponding processing having been conducted to form capacitors 60b wherein the individual inner capacitor electrodes 52b comprise open container shapes.

Embodiments as described herein encompass a method of forming a plurality of capacitors which comprises forming a plurality of individual capacitor electrodes comprising using two masking steps. An earlier of the two masking steps is used to form an array of first openings (i.e., first openings 34) over a plurality of storage node contacts. A later of the two masking steps is used to form an array of second openings (i.e., second openings 42) received partially over and partially offset from the array of first openings. Overlapping portions of the first and second openings are received over the storage node contacts. Masking steps might also be added before and after the stated earlier and later masking steps in fabrication of a plurality of individual capacitor electrodes.

After both of the two stated masking steps, conductive material of the individual capacitor electrodes is deposited into the overlapping portions of each of the first and second openings. The individual capacitor electrodes are ultimately incorporated into a plurality of capacitors. In some embodiments, the overlapping portions of the first and second openings have the same horizontal cross sectional size and shape as that of individual of the storage node contacts in at least one horizontal cross section, for example and by way of example only as is depicted in each of the above depicted embodiments. However, the overlapping portions might everywhere have different horizontal cross sectional size and shape to that of individual of the storage node contacts.

In some embodiments, at least the individual first openings within which the masking material is deposited are no greater than 3.5F X 5.5F in horizontal size, where "F" is the minimum feature size measured orthogonally that is obtained using lithography to pattern features in fabrication of the plurality of capacitors. Each of the above-depicted Figs. 1-49 embodiments may, for example, be utilized in fabricating individual first openings to have such a horizontal size which is less than or equal to 3.5F X 5.5F.

Fig. 50 diagrammatically depicts in top view an alternate example embodiment wherein each of individual first openings 34c and each of individual second openings 42c have respective horizontal sizes which are 3.5F X 5.5F. Fig. 50 diagrammatically depicts a top view of a substrate fragment 10c. Like numerals from the above-described embodiments have been utilized where appropriate, with differences being indicated with the suffix "c" or with

different numerals. By way of example only, each of first openings 34c and second openings 42c are quadrilateral in shape, yet of different shape. Further by way of example only, the different shapes of openings 34c and 42c are each parallelograms. Further in one example embodiment and as shown, substrate fragment 10c is depicted as comprising overlapping portions 70 of first openings 34c and second openings 42c which are quadrilateral in shape, and in one embodiment yet which are not of a parallelogram shape. Further by way of example only, such depicts an example wherein overlapping portions 70 have different horizontal cross sectional size and shape from that of individual of the storage node contacts, where for example such were fabricated to be square or rectangular as in the above-depicted example Figs. 1-49 embodiments, for example which could also may be incorporated in the Fig. 50 embodiment.

In some embodiments, at least the individual first openings within which the masking material may be deposited are no greater than F X F in horizontal size, where "F" is the minimum feature size measured orthogonally that is obtained using lithography to pattern features in fabrication of the plurality of capacitors.

CLAIMS:

1. A method of forming a plurality of capacitors, comprising:

forming a plurality of individual capacitor electrodes comprising using two masking steps, an earlier of the two masking steps being used to form an array of first openings over a plurality of storage node contacts, a later of the two masking steps being used to form an array of second openings received partially over and partially offset from the array of first openings, overlapping portions of the first and second openings being received over the storage node contacts;

after both of the two masking steps, depositing conductive material of the individual capacitor electrodes into the overlapping portions of each of the first and second openings; and

incorporating the individual capacitor electrodes into a plurality of capacitors.

2. The method of claim 1 wherein the conductive material is deposited to form the individual capacitor electrodes to comprise an open container shape.

3. The method of claim 1 wherein the conductive material is deposited to form the individual capacitor electrodes to comprise a singular pillar.

4. The method of claim 1 wherein the overlapping portions have the same horizontal cross sectional size and shape as that of individual of the storage node contacts in at least one horizontal cross section.

5. The method of claim 1 wherein the overlapping portions everywhere have different horizontal cross sectional size and shape as that of individual of the storage node contacts.

6. A method of forming a plurality of capacitors, comprising:

forming first material over an array of storage node contacts;

forming an array of first openings into the first material over the storage node contacts, individual of the first openings being formed over at least two of the storage node contacts;

depositing masking material within the first openings and which is received over the storage node contacts;

forming an array of second openings in a mask, the array of second openings being received partially over and partially offset from the array of first openings, individual of the second openings being formed over at least two storage node contacts that are received under different and adjacent of the first openings;

etching the masking material through the second openings in the mask to remove the masking material from being received over the storage node contacts within the first openings;

after the etching, forming conductive material within the first openings in electrical connection with the storage node contacts and to comprise individual capacitor electrodes; and

incorporating the individual capacitor electrodes into a plurality of capacitors.

7. The method of claim 6 wherein the individual first openings within which the masking material is deposited are no greater than 3.5F X 5.5F in horizontal size, where "F" is the minimum feature size measured orthogonally that is obtained using lithography to pattern features in fabrication of the plurality of capacitors.

8. The method of claim 7 wherein the horizontal size is 3.5F X 5.5F.

9. The method of claim 7 wherein the horizontal size is less than 3.5F X 5.5F.

10. The method of claim 6 wherein the individual first openings within which the masking material is deposited are no greater than 5F X 5F in horizontal size, where "F" is the minimum feature size measured orthogonally that is obtained using lithography to pattern features in fabrication of the plurality of capacitors.

11. The method of claim 6 wherein the individual of the first openings are formed over four or less of the storage node contacts.

12. The method of claim 6 wherein the first and second openings are all of the same size and shape in at least one horizontal cross section.

13. The method of claim 6 wherein the first and second openings are of different size and shape in at least one horizontal cross section.

14. The method of claim 13 wherein the different shapes are each parallelograms in the at least one horizontal cross section.

15. The method of claim 6 wherein the individual of the first openings are formed over only four of the storage node contacts, and the individual of the second openings are formed over only four of the storage node contacts.

16. The method of claim 15 wherein the first and second openings individually comprise parallelogram shapes in at least one horizontal cross section.

17. A method of forming a plurality of capacitors, comprising:

forming first material over an array of storage node contacts;

forming an array of first openings into the first material over the storage node contacts, individual of the first openings being formed over at least two of the storage node contacts and comprising surrounding sidewalls;

lining the surrounding first opening sidewalls with masking material which less than fills the first openings and is received over the storage node contacts;

forming second material to within the first openings adjacent the masking material;

forming an array of second openings in a mask, the array of second openings being received partially over and partially offset from the array of first openings, individual of the second openings being formed over at least two storage node contacts that are received under different and adjacent of the first openings;

etching the masking material selectively relative to the second material through the second openings in the mask to remove the masking material from being received over the storage node contacts within the first openings;

after the etching, forming conductive material within the first openings in electrical connection with the storage node contacts and to comprise individual capacitor electrodes; and

incorporating the individual capacitor electrodes into a plurality of capacitors.

18. The method of claim 17 wherein the etching is conducted selectively relative to the first material.

19. The method of claim 17 wherein the first material comprises at least first and second etchably different materials, and further comprising etching the second etchably different material selectively relative to the first etchably different material to form a lattice retaining structure comprised of the first etchably different material that is received externally among the individual capacitor electrodes.

20. The method of claim 17 wherein the individual of the first openings are formed over four or less of the storage node contacts.

21. The method of claim 17 wherein the first openings within which the masking material is received do not extend to the storage node contacts.

22. The method of claim 17 wherein said lining comprises forming the masking material to have a lateral thickness within the first openings which is no greater than 40% of a minimum horizontal cross sectional open dimension at outermost portions of the individual first openings.

23. The method of claim 17 wherein the individual of the second openings are formed over four or less of the storage node contacts.

24. The method of claim 17 wherein the individual of the first openings are formed over only four of the storage node contacts, and the individual of the second openings are formed over only four of the storage node contacts.

25. The method of claim 24 wherein the first and second openings individually comprise parallelogram shapes in at least one horizontal cross section.

26. The method of claim 17 comprising after forming the conductive material, etching all remaining of said masking material from the first openings.

27. The method of claim 17 comprising after forming the conductive material, etching all remaining of said second material from the first openings.

28. A method of forming a plurality of capacitors, comprising:

forming first material over an array of storage node contacts;

forming an array of first openings into the first material over the storage node contacts, individual of the first openings being formed over at least two of the storage node contacts;

forming masking material to completely fill the first openings;

forming an array of second openings in a mask, the array of second openings being received partially over and partially offset from the array of first openings, individual of the second openings being formed over at least two storage node contacts that are received under different and adjacent of the first openings;

etching the masking material through the second openings in the mask to remove the masking material from being received over the storage node contacts within the first openings;

after the etching, forming conductive material within the first openings in electrical connection with the storage node contacts and to comprise individual capacitor electrodes; and

incorporating the individual capacitor electrodes into a plurality of capacitors.

29. A method of forming a plurality of capacitors, comprising:

forming first material over an array of storage node contacts;

forming an array of first openings into the first material over the storage node contacts, individual of the first openings being formed over four of the storage node contacts;

depositing masking material within the first openings and which is received over the storage node contacts;

forming an array of second openings in a mask, the array of second openings being received partially over and partially offset from the array of first openings, overlapping portions of the first and second openings being received over the storage node contacts, individual of the second openings being formed over four of the storage node contacts that are received under different and adjacent of the first openings, the first and second openings individually being quadrilateral in shape in at least one horizontal cross section;

etching the masking material through the second openings in the mask to remove the masking material from being received over the storage node contacts within the first openings;

after the etching, forming conductive material within the first openings in electrical connection with the storage node contacts and to comprise individual capacitor electrodes; and

incorporating the individual capacitor electrodes into a plurality of capacitors.

30. The method of claim 29 wherein the quadrilateral shapes of the first openings in the at least one cross section and the quadrilateral shapes of the second openings in the at least one cross sections comprise parallelograms.

31. The method of claim 29 wherein the quadrilateral shapes of the first openings in the at least one cross section and the quadrilateral shapes of the second openings in the at least one cross sections are of the same shape.

32. The method of claim 29 wherein the quadrilateral shapes of the first openings in the at least one cross section and the quadrilateral shapes of the second openings in the at least one cross sections are of different shape.

33. The method of claim 32 wherein the different shapes are each parallelograms.

34. The method of claim 29 wherein the overlapping portions are in quadrilateral shapes in at least one horizontal cross section.

35. The method of claim 34 wherein the quadrilateral shapes of the overlapping portions are not parallelograms.