Claims

What is claimed:

1. A semiconductor device, comprising:

a wafer-level carrier;

a first insulating layer formed over an entire surface of the wafer-level carrier;

a first interconnect structure formed in contact with the first insulating layer, the first interconnect structure including,

(a) a second insulating layer including fiber or cloth material, and

(b) a first conductive layer formed over the second insulating layer, wherein the first interconnect structure is completely separated from the wafer-level carrier by the first insulating layer;

a semiconductor die disposed over the first interconnect structure;

a vertical interconnect structure formed over the first interconnect structure and around the semiconductor die;

an encapsulant deposited over the semiconductor die and first interconnect structure and around the vertical interconnect structure;

a second interconnect structure formed over the vertical interconnect structure and in contact with a surface of the encapsulant opposite the first interconnect structure and extending across the wafer-level carrier, the second interconnect structure including,

(a) a third insulating layer, and

(b) a second conductive layer formed over the third

insulating layer; and

a polymer protective layer disposed around the vertical interconnect structure between the first interconnect structure and second interconnect structure.

2. The semiconductor device of claim 1, wherein the vertical interconnect structure is electrically connected to the second interconnect structure.

3. The semiconductor device of claim 1, wherein the vertical interconnect structure includes a plurality of bumps or stud bumps.

4. The semiconductor device of claim 1, wherein the semiconductor die is a known good semiconductor die.

5. The semiconductor device of claim 1, further including a discrete device embedded in the encapsulant.

6. A semiconductor device, comprising:

a wafer-level carrier;

a first insulating layer formed over an entire surface of the wafer-level carrier;

a first interconnect structure formed in contact with the first insulating layer, the first interconnect structure including,

(a) a second insulating layer, and

(b) a first conductive layer formed over the second insulating layer, wherein the first interconnect structure is completely separated from the wafer-level carrier by the first insulating layer;

a semiconductor die disposed over the first interconnect structure;

an encapsulant deposited over the semiconductor die and first interconnect structure;

a second interconnect structure formed over a surface of the encapsulant opposite the first interconnect structure and extending across the first interconnect structure, wherein the second interconnect structure includes,

(a) a third insulating layer, and

(b) a second conductive layer formed over the third insulating layer with the encapsulant deposited on side surfaces of the third insulating layer and second conductive layer; and

a vertical interconnect structure disposed between the first interconnect structure and second interconnect structure.

7. The semiconductor device of claim 6, further including a polymer protective layer disposed around the vertical interconnect structure between the first interconnect structure and second interconnect structure.

8. The semiconductor device of claim 6, wherein the vertical interconnect structure includes a plurality of bumps or stud bumps.

9. The semiconductor device of claim 6, wherein the semiconductor die is a known good semiconductor die.

10. The semiconductor device of claim 6, further including a discrete device embedded in the encapsulant.

11. The semiconductor device of claim 6, wherein an active surface of the semiconductor die is oriented toward the first interconnect structure.

12. The semiconductor device of claim 6, wherein an active surface of the semiconductor die is oriented toward the second interconnect structure.

13. A semiconductor device, comprising:

a wafer-level carrier;

a first insulating layer formed over an entire surface of the wafer-level carrier;

a first interconnect structure formed over the first insulating layer, the first interconnect structure including,

(a) a second insulating layer, and

(b) a first conductive layer formed over the second insulating layer;

a second interconnect structure disposed over the first interconnect structure, the second interconnect structure including,

(a) a third insulating layer, and

(b) a second conductive layer formed over the third insulating layer;

a semiconductor die disposed between the first interconnect structure and second interconnect structure;

an encapsulant deposited between the first interconnect structure and second interconnect structure and around the semiconductor die and second interconnect structure; and

a vertical interconnect structure extending from the first interconnect structure to the second interconnect structure.

14. The semiconductor device of claim 13, further including a protective layer disposed around the vertical interconnect structure.

15. The semiconductor device of claim 13, wherein the vertical interconnect structure includes a plurality of bumps or stud bumps.

16. The semiconductor device of claim 13, wherein the semiconductor die is a known good semiconductor die.

17. The semiconductor device of claim 13, further including a discrete device embedded in the encapsulant.

18. The semiconductor device of claim 13, wherein an active surface of the semiconductor die is oriented toward the first interconnect structure or the second interconnect structure.