STACKED LDD HIGH FREQUENCY LDMOSFET

FIELD OF THE INVENTION

The invention relates to the general field of high frequency power devices with particular reference to reducing on-resistance while increasing breakdown voltage.

BACKGROUND OF THE INVENTION

High frequency power devices, have become an indispensable part of modern personal communication systems. Among the various power devices, the LDMOSFET (Lateral Double-diffused metal oxide field effect transistor) is becoming more popular than its bipolar and GaAs counterparts. The desirable characteristics of RF LDMOSFET are a high frequency performance, a low on-state voltage drop, and a high blocking voltage.

The device structure of a conventional RF LDMOS is shown in FIG. 1. Heavily doped p+ sinker 11 is used to connect the source 12 to the substrate 10. This enables the source to be led out from the bottom, saving the source bond wire and minimizing the

common lead inductance thus offering a better RF performance. An N-LDD (Lightly Doped Drain) region 19 with a shallow junction is used as the drift region. The on-resistance of the conventional high voltage power LDMOS is mainly dominated by the resistance of the voltage sustaining LDD region. The LDMOS blocking capability is mainly determined by the LDD length and doping concentration.

Also shown in FIG. 1 are polysilicon gate 15, gate oxide 14, epitaxially formed P-body 17, diffusion formed P- body 13, drain region 18, and drain contact 16. Additionally, the output capacitance of the device is schematically shown as capacitor 99.

Because the doping concentration in the drift region is severely restricted by the blocking voltage, a trade-off exists between high breakdown voltage and low on-state resistance. This trade-off also limits the achievable application frequency of a high voltage RF LDMOSFET. Several approaches to improving the on-state resistance/breakdown voltage tradeoff have been proposed such as, for example, Der-Gao Lin et al. in "A novel LDMOS structure with a step gate oxide" IEDM 1995, pp. 38.2.1-38.2.2. With this approach the length of the drift region can be reduced so that the resistance is lowered without affecting the breakdown voltage.

For high voltage RF LDMOS, in which the drift region constitutes the major source of on-resistance, the main emphasis in improving the transistor performance must be

directed towards reducing the LDD resistance. In the present invention a novel RF LDMOS with a stacked LDD structure using existing multiple implant technology is disclosed. Without the need of extra masks, the device was implemented using standard RF LDMOS processing technology.

A routine search of the prior art was performed with the following references of interest being found:

Der-Goa Lin, et al. "A novel LDMOS Structure with a step gate oxide", IEDM, 1995- pp. 963 to 966. US 5,585,294(Smayuling et al.) shows a DD LDMOS with multiple LDD's. US 5,869,875(Herbert) shows a LDMOS with a trench source contact and sinker. US 6,087,232(Kim et al.), US 6,144,070(Devore et al.) and US 6,118,152(Yamaguchi et al.) show related LDMOS devices and methods.

SUMMARY OF THE INVENTION

It has been an object of the present invention to provide a LDMOSFET with both higher breakdown voltage and lower on-state resistance than comparable devices of the prior art.

Another object of the invention has been to provide a LDMOSFET with improved high frequency characteristics relative to comparable devices of the prior art.

Still another object has been to provide a process for the manufacture of said improved LDMOSFET.

A further object has been that said manufacturing process be made up of processing steps already in regular use.

These objects have been achieved by changing the composition of the conventional LDD structure that lies between the gate and the drain from a single layer of N type material to a stack of three layers. These are upper and lower N type layers with a P type layer between them. The upper N type layer is heavily doped to reduce the on-resistance of the device, while the lower N type layer is lightly doped to reduce the output capacitance, thereby improving the high frequency performance. The middle P layer is heavily doped which allows it to bring about pinch-off of the two N layers, thereby raising the device's breakdown voltage.

BRIEF DESCRIPTION OF THE DRAWINGS

FIG. I is a cross-sectional view of an RF LDMOS structure of the prior art.

FIG. 2 is a cross-sectional view of the stacked LDD RF LDMOS structure.

FIG. 3a is a schematic representation a conventional LDD structure with arrows indicating spreading directions of depletion edges and dotted lines showing the depletion edge.

FIG. 3b is similar to FIG. 3a except it is for a stacked LDD RF LDMOS device.

FIG. 4 shows plots of Ids vs. Vds for both prior art and the present invention.

FIG. 5 shows plots of Gm(mS) and Ids as a function of Vgs for both the prior art and the present invention.

FIG. 6: plots fT-Vgs characteristics for both a prior art and a stacked LDD RF LDMOS device.

DESCRIPTION OF THE PREFERRED EMBODIMENTS

The LDMOS structure of the present invention is shown in FIG. 2. The key difference between the invention and the prior art structure shown in FIG. 1 lies in the LDD portion of the device. As can be seen, the single N type layer 19 of the prior art structure has been replaced by a stacked LDD comprising three layers --- N type layer 21, P type layer 22, and N type layer 23.

This modification of the prior art structure minimizes the drift region resistance while at the same time maintaining a high blocking voltage. Layer 21 (LDD1) has a high doping concentration and junction depth that is sufficient to reduce the on-resistance of the device, while layer 23 (LDD3) has a low doping concentration and a deeper junction depth that serves to reduce the output capacitance . Layer 22 (LDD2) has high P doping, which introduces additional negative charges that can cause pinch-off of the LDD1 and LDD3 regions. The totally depleted drift region supports the device breakdown voltage.

Shown in FIGs. 3a and 3b is a schematic comparison between a conventional LDD structure, such as the device of FIG. 1, and the stacked LDD structure of the present invention. FIG. 3a shows a single layer LDD of the prior art having a single depletion layer 31 that extends into it from P- body 13. FIG. 3b shows how LDD2 helps to deplete LDD1 and LDD3 while it itself is also being depleted at the same time. This is possible because

a reverse-biased voltage across the LDD2/LDD1 and LDD2/LDD3 junctions exists. This in turn is because LDD2 is connected to P- body 13, which is grounded, while LDD1 and LDD3 are connected to N+ drain 18 which has a high applied positive bias.

Thus, in addition to a depletion layer due to the P- body (prior art case), LDD1 and LDD3 are depleted in both the lateral and vertical directions due to the existence of LDD2. Assuming the doping levels and the junction depths are properly selected, it becomes possible to deplete all of the stacked LDD regions. Thus the increase in the LDD1 doping level (which can be much higher than in a prior art device) will reduce the on-state resistance of the device. Therefore, the device current handling capability is improved. As a result, the Ron of the stacked structure will be much lower than that of a conventional structure having the same Bvds (breakdown voltage source-to-drain).

The process of the present invention uses conventional LDMOS process steps in a novel manner in order to form the structure of the present invention. Referring once again to FIG. 2, the process begins with the provision of a starting wafer 10 of P+ silicon. and depositing thereon epitaxial layer, of P- silicon, 17. Then P+ sinker region 11 that extends downwards from the top surface, through the P- epitaxial layer 17 into the P+ substrate 10 is formed by means of ion implantation through a mask. This is followed by a drive-in diffusion.

Next, a layer of gate oxide 14 is grown on the top surface and a layer of phosphorus doped polysilicon 15 is deposited over it to a sheet resistance of about I 0 ohms per square. The polysilicon is patterned and etched to form gate pedestal 15. By P-body implant through a P-body mask, followed by a P-body diffusion process and N+ source implant through a N+ source mask, followed by an N+ diffusion process (LDMOS double diffusion), N+ source region 12 is formed on one side of the gate pedestal (on its left in this example) as well as P- body 13. The latter extends outwards from source region 12 and emerges at the top surface underneath gate oxide 14. By ion implantation through a mask, drain region 18 is then formed on the opposite side of the gate, there being a separation region between gate 15 and drain region 18 for the LDD with a blank LDD implant. This separation region has a length of between about 2 and 40 microns.

Now follows a key feature of the invention. By ion implantation (60keV arsenic at $7x10^{12}$ per sq. cm), N type layer 21 (LDD1) is formed in the separation region. This is followed by the formation of P type layer 22 (LDD2) using 45keV boron at $7x10^{12}$ per sq. cm located immediately below LDD1. N type layer 23 (LDD3) was placed immediately below LDD2 by using 200keV phosphorus at $2.5x10^{12}$ per sq. cm. Use of the above ion energies and fluences resulted in the LDD1 layer having a resistivity between about 0.002 and 0.02 ohm cm and a thickness between about 300 and 2,000 Angstroms. For LDD2, the resistivity was between about 0.007 and 0.05 ohm cm for a thickness of between about 1,000 and 3,000 Angstroms while for LDD3 the resistivity was between about 0.03 and 0.2

ohm cm and its thickness was between about 1,000 and 6,000 Angstroms.

Provided the thicknesses and resistivities of the three layers fall within the ranges cited above, devices made this way (i.e. the stacked LDMOSFET of the present invention) have breakdown voltages greater than about 70 volts, an on-resistance less than about 0.05 ohms per micron in the linear region, and a peak frequency response greater than 7 GHz.

Experimental confirmation:

FIG. 4 compares experimental I-V characteristics of the prior art with those of a stacked LDD RF LDMOSFET made according to the teachings of the present invention. It can be seen that at Vgs=20V, for the same current level of 70mA, the on-state voltage drop was 5.1V for the conventional RF LDMOSFET (curve family 41) while it is reduced to only 3V (curve family 42) for the stacked LDD device, indicating an improvement of 70% for Von. At the same Vgs of 20V, the saturation current of the prior art and stacked LDD devices is 105mA and 175mA, respectively, with a 67% improvement in Idsat. The measured breakdown voltage of the prior art and stacked structures were approximately 64V and 74V, respectively. Thus, when compared to a device of the prior art, the stacked

LDD structure provides a 16% improvement in the off-state performance.

DC-measurements of fabricated transistors produced the transfer characteristics shown in FIG. 5. An outstanding attribute of the stacked LDD device is the wide plateau of high transconductance between Vgs=3V and Vgs=10V. The on-state resistance of a LDMOS mainly consists of channel resistance Rch and drift region resistance Rdrift. The total on-state resistance decreases with increasing gate bias. At a low gate bias, the value of the channel resistance is comparable to the drift resistance, and the drain current increases linearly with gate bias. At a high gate bias, due to the channel resistance being much lower than the drift resistance, the drain current is only affected by the drift resistance, and the gate easily loses its current control capability. The lower the drift region resistance, the stronger the gate control capability.

This performance is very important for RF LDMOS used in large signal power amplifiers. From FIG. 4, it can be seen that, at a high gate bias, the stacked LDD structure has a much higher gate control capability compared with that of the prior art RF LDMOS. This strong gate control capability is also shown in FIG. 5 in which a wide and flat transconductance vs. Vgs curve is obtained. At a gate voltage of I0V, the transconductance in the stacked LDD structure is 13.7mS (arrow 52) while it is 5.6mS in the prior art device (arrow 51). Thus, the transconductance of the stacked LDD is approximately 2.4 times higher than that of the prior art RF LDMOS. This means that the stacked

LDD device has a lower inter-modulation distortion and higher power gain. Thus, the upper limit of the usable output power is much higher for the stacked LDD device.

In order to characterize the RF behaviors of the conventional and stacked LDD devices, on-wafer S-parameters were measured in the range from 0.5GHz to 10.05GHz using a HP 8510C network analyzer. The operating point of the device was varied between Vgs=3V and Vgs=15V at a fixed Vds of 20V. The gate bias dependence of f_T at Vds=20V in both the prior art and stacked LDD devices were obtained.

Referring now to FIG. 6, corresponding to the Gm behaviors in FIG. 5, the cut-off frequency of the stacked LDD device (curve 62) reaches its maximum of 7GHz at Vgs=5V, keeps its high level up to Vgs=10V, and then decrease continuously. At a gate voltage of 10V, the stacked LDD structure still has a 5 GHz cut-off frequency --- a 108 % improvement over the prior art RF LDMOS which is shown as curve 61.

While the invention has been particularly shown and described with reference to the preferred embodiments thereof, it will be understood by those skilled in the art that various changes in form and details may be made without departing from the spirit and scope of the invention.

What is claimed is:

* C L M S *

CLAIMS

1. A multi-layer lateral double diffused structure, comprising:

a topmost layer of N type silicon;

a middle layer of P type silicon; and

a bottommost layer of N type silicon,

said structure being part of a power MOSFET that has a gate and a drain; and

said structure being located between said gate and said drain.

2. The structure described in claim 1 wherein said topmost layer of N type silicon has a resistivity between about 0.002 and 0.02 ohm cm.

3. The structure described in claim 1 wherein said topmost layer of N type silicon has a thickness between about 300 and 2,000 Angstroms.

4. The structure described in claim 1 wherein said middle layer of P type silicon has a resistivity between about 0.007 and 0.05 ohm cm.

5. The structure described in claim 1 wherein said middle layer of P type silicon has a thickness between about 1,000 and 3,000 Angstroms.

6. The structure described in claim 1 wherein said bottommost layer of N type silicon has a resistivity between about 0.03 and 0.2 ohm cm.

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7. The structure described in claim 1 wherein said bottommost layer of N type silicon has a thickness between about 1,000 and 6,000 Angstroms.

8. A stacked high frequency LDMOSFET, comprising:

a P+ silicon substrate on which has been deposited an epitaxial layer of P- silicon having an upper surface;

a P+ sinker region that extends downwards from said upper surface through the P- epitaxial layer into the P+ substrate;

a polysilicon gate pedestal over said upper surface, there being a layer of gate oxide between the pedestal and the upper surface;

an N+ source region on a first side of said gate pedestal and a P- body under the gate extending into said source region;

a drain region on an opposing second side of the gate there being a separation region between the gate and the drain region;

in said separation region, a first N type LDD layer that extends downward from said upper surface to a first interface;

in said separation region, a P type LDD layer that extends downward from said first interface to a second interface; and

in said separation region, a second N type LDD layer that extends downward from said second interface to a third interface.

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9. The stacked LDMOSFET described in claim 8 wherein said first N type LDD layer has a resistivity between about 0.002 and 0.02 ohm cm.

10. The stacked LDMOSFET described in claim 8 wherein said first N type LDD layer has a thickness between about 300 and 2,000 Angstroms.

11. The stacked LDMOSFET described in claim 8 wherein said P type LDD layer has a resistivity between about 0.007 and 0.05 ohm cm.

12. The stacked LDMOSFET described in claim 8 wherein said P type LDD layer has a thickness between about 1,000 and 3,000 Angstroms.

13. The stacked LDMOSFET described in claim 8 wherein said second N type LDD layer has a resistivity between about 0.03 and 0.2 ohm cm.

14. The stacked LDMOSFET described in claim 8 wherein said second N type LDD layer has a thickness between about 1,000 and 6,000 Angstroms.

15. The stacked LDMOSFET described in claim 8 wherein said stacked LDMOSFET has breakdown voltage greater than about 70 volts and an on resistance less than about 0.05 ohms per micron where response is linear.

16. A process for manufacturing an LDMOSFET, comprising:

providing a P+ silicon substrate and depositing thereon an epitaxial layer of P- silicon having an upper surface;

forming a P+ sinker region that extends downwards from said upper surface through the P- epitaxial layer into the P+ substrate, by means of ion implantation through a mask, followed by a drive-in diffusion;

growing a layer of gate oxide on said upper surface and then depositing thereon a layer of phosphorus doped polysilicon;

patterning and etching said polysilicon layer to form a gate pedestal and then removing all gate oxide not under said gate pedestal;

by means of double diffusion through a mask, forming an N+ source region on a first side of said gate pedestal and a P- body under the gate and extending into said source region;

by ion implantation through a mask, forming a drain region on an opposing second side of the gate there being a separation region between the gate and the drain region;

in said separation region, forming, by ion implantation, a first N type LDD layer that extends downward from said upper surface to a first interface;

in said separation region, forming, by ion implantation, a P type LDD layer that extends downward from said first interface to a second interface; and

in said separation region, forming, by ion implantation, a second N type LDD layer that extends downward from said second interface to a third interface.

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17. The process described in claim 16 wherein said first N type LDD layer has a resistivity between about 0.002 and 0.02 ohm cm.

18. The process described in claim 16 wherein said first N type LDD layer has a thickness between about 300 and 2,000 Angstroms.

19. The process described in claim 16 wherein said P type LDD layer has a resistivity between about 0.007 and 0.05 ohm cm.

20. The process described in claim 16 wherein said P type LDD layer has a thickness between about 1,000 and 3,000 Angstroms.

21. The process described in claim 16 wherein said second N type LDD layer has a resistivity between about 0.03 and 0.2 ohm cm.

22. The process described in claim 16 wherein said second N type LDD layer has a thickness between about 1,000 and 6,000 Angstroms.

23. The process described in claim 16 wherein said stacked LDMOSFET has breakdown voltage greater than about 70 volts and an on resistance less than about 0.05 ohms per micron where response is linear.