CLAIMS

1. A method for manufacturing a semiconductor structure, comprising:

providing a base, and forming a plurality of active layers spaced apart from each other in a first direction in the base; and

forming a plurality of bit lines spaced apart from each other in the first direction, wherein the plurality of bit lines extend in a second direction, a first portion of each of the plurality of bit lines covers side surfaces of respective active layers of the plurality of active layers, and a second portion of each of the plurality of bit lines is located in the respective active layers; and wherein the first direction and the second direction are parallel to a surface of the base, and the first direction intersects with the second direction;

wherein forming the plurality of bit lines comprises:

forming a plurality of first conductive structures extending in the second direction, wherein the plurality of first conductive structures are located on the side surfaces of the plurality of active layers spaced apart from each other in the first direction; and

forming a plurality of second conductive structures, wherein the plurality of second conductive structures are located in the plurality of active layers, and each the plurality of second conductive structures is at least located between two first conductive structures of the plurality of first conductive structures, and is in contact with and electrically connected to the two first conductive structures;

wherein forming the plurality of first conductive structures comprises:

providing the base;

patterning the base, to form the plurality of active layers spaced apart from each other in the first direction;

forming a first isolation layer, wherein the first isolation layer is located between adjacent active layers of the plurality of active layers, and a top surface of the first isolation layer is lower than a top surface of each of the plurality of active layers; and

forming the plurality of first conductive structures above the first isolation layer.

2. The method for manufacturing the semiconductor structure of claim 1, wherein forming the first isolation layer comprises: forming a first mask layer on the surface of the base, and etching the first mask layer and the base to form a plurality of first trenches extending in the second direction, wherein the first trenches are located between the adjacent active layers; and

completely filling the plurality of first trenches with an insulation material, and removing part of the insulation material, to form the first isolation layer in the plurality of first trenches.

3. The method for manufacturing the semiconductor structure of claim 2, wherein forming the plurality of first conductive structures above the first isolation layer comprises:

forming a second mask layer, wherein the second mask layer is located above the first isolation layer and covers a sidewall of each of the plurality of active layers;

removing part of the first isolation layer and part of the sidewall of each of the

plurality of active layers under the second mask layer, to form a first groove; and

depositing a first conductive material in the first groove, and patterning the first conductive material, to form the plurality of first conductive structures spaced apart from each other.

4. The method for manufacturing the semiconductor structure of claim 3, wherein forming the plurality of second conductive structures comprises:

etching the plurality of active layers to form a plurality of second trenches extending in the first direction, wherein bottom surfaces of the plurality of second trenches are higher than top surfaces of the plurality of first conductive structures;

forming a plurality of third mask layers in the plurality of second trenches, wherein the plurality of third mask layers cover sidewalls of the plurality of second trenches; and

depositing a second conductive material at bottoms of the plurality of second trenches, and performing rapid thermal process on the second conductive material to form the plurality of second conductive structures.

5. The method for manufacturing the semiconductor structure of claim 4, wherein the second conductive material comprises a metal material, wherein during the rapid thermal process, the metal material is dispersed into the plurality of active layers to form metal silicide, and the metal silicide is at least located between the two first conductive structures, to form the plurality of second conductive structures.

6. The method for manufacturing the semiconductor structure of claim 4, wherein a

temperature for the rapid thermal process ranges from 400℃ to 800℃.

7. The method for manufacturing the semiconductor structure of claim 1, wherein the plurality of second conductive structures located between the two first conductive structures are connected to each other, and extend through the plurality of active layers in the second direction.

8. A semiconductor structure, manufactured by the method according to any one of claims 1-7, comprising:

a substrate; a plurality of active layers, wherein the plurality of active layers are arranged on the substrate and spaced apart from each other; and

a plurality of bit lines, wherein the plurality of bit lines are spaced apart from each other in a first direction and extend in a second direction, wherein a first portion of each of the plurality of bit lines covers side surfaces of respective active layers of the plurality of active layers, and a second portion of each of the plurality of bit lines is located in the respective active layers; and wherein the first direction and the second direction are parallel to a surface of the substrate, and the first direction intersects with the second direction.

9. The semiconductor structure of claim 8, wherein the first portion comprises two first conductive structures that are spaced apart from each other and extend in the second direction, the second portion comprises a plurality of second conductive structures, and the plurality of second conductive structures are located in the respective active layers, wherein each of the plurality of second conductive structures is at least located between the two first conductive structures, and each of the plurality

of second conductive structures is in contact with and electrically connected to the two first conductive structures.

10. The semiconductor structure of claim 9, wherein the plurality of second conductive structures are connected together in an extending direction of each of the plurality of bit lines, and extend through the respective active layers.

11. The semiconductor structure of claim 9 or 10, wherein a material of the plurality of second conductive structures comprises metal silicide, and a material of the two first conductive structures comprises conductive metal.

12. The semiconductor structure of claim 9, wherein a thickness of each of the two first conductive structures in the first direction ranges from 1 nm to 3 nm.

13. The semiconductor structure of claim 9, wherein a height of an overlapping portion of a projection of each of the plurality of second conductive structures and a projection of each of the two first conductive structures in a plane perpendicular to the substrate is 0.5 to 1 times a height of the projection of each of the plurality of second conductive structures in the plane perpendicular to the substrate.