

PATENT SPECIFICATION

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(54) MANUFACTURE OF SEMICONDUCTOR DEVICES

(71) We, PHILIPS ELECTRONIC AND ASSOCIATED INDUSTRIES LIMITED, of Abacus House, 33 Gutter Lane, London, E.C.2, a British Company, do hereby declare the invention, for which we pray that a patent may be granted to us, and the method by which it is to be performed, to be particularly described in and by the following statement:—

10 This invention relates to methods of manufacturing semiconductor devices, and further relates to such semiconductor devices.

15 In our British Patent No. 1,208,576 there is described and claimed a method of manufacturing a semiconductor device comprising semiconductor circuit elements electrically insulated from each other, in which a silicon layer on a substrate is subjected to an oxidizing treatment while selected portions of the surface of the silicon layer are masked against oxidation by means of an insulating masking layer comprising masking material other than silicon oxide and so causing an oxide of silicon to grow into the silicon at the unmasked portions until the grown oxide forms a layer which is sunk throughout the entire thickness of the silicon layer to divide the silicon layer into isolated regions separated from each other by the sunken grown oxide, whereafter a circuit element is provided in each of a plurality of the isolated silicon regions.

35 Such a silicon layer may be in the form of an epitaxial silicon layer of one conductivity type which is provided on a semiconductor substrate of the opposite conductivity type. The oxidation treatment to provide the layer pattern of silicon oxide is continued until the pattern extends throughout the thickness of the epitaxial silicon layer to the substrate material of the opposite conductivity type.

45 It has been found that conductive channels adjoining the oxide layer pattern can occur in the semiconductor substrate

and interconnect the parts of the epitaxial layer separated from each other by the layer pattern. A possible explanation for the formation of such conductive channels is that during the provision of the layer pattern of silicon oxide, the impurity which determines the conductivity type of the epitaxial layer diffuses from the epitaxial layer into the substrate ahead of the oxide and forms at the area below the pattern a region of the same conductivity type as the epitaxial layer.

In our co-pending British Patent Application No. 21902/71 (Serial No. 1,349,573) it has already been stated that such channels can be avoided by using a substrate which is more highly doped than the epitaxial layer. However, it is desirable to provide an improvement which avoids such channels and which offers a wider choice both as regards impurities and their concentration and as regards the device structure to be obtained.

According to one aspect of the present invention there is provided a method of manufacturing a semiconductor device comprising providing a silicon epitaxial layer on a semiconductor substrate to form a semiconductor body, and subjecting the epitaxial layer to an oxidation treatment while locally masking the surface of the epitaxial layer against oxidation and so causing an oxide of silicon to grow into the unmasked silicon until the grown oxide forms a layer pattern which is sunk over at least part of its thickness in the semiconductor body and extends across the thickness of the epitaxial layer so as to mutually separate parts of the epitaxial layer for forming islands in which regions of one or more semiconductor circuit elements are to be or are provided, the separate islands being electrically isolated from an underlying substrate part by $p-n$ junction isolation, in which method a zone of the same conductivity type as, but a higher doping than, said substrate part is locally provided at least partly in the said substrate part to adjoin the

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sunken oxide layer pattern, which zone has such a high doping concentration that formation in the substrate part of undesirable channels adjoining the sunken oxide layer pattern and connecting regions of adjacent islands is prevented.

Using such a method in accordance with the present invention it is possible, for example, to adapt the doping or the resistivity of the substrate to the requirements imposed on the semiconductor device to be manufactured. For example, in the case in which the capacitance between the epitaxial layer and the substrate must be low, the doping of the substrate can be kept low substantially arbitrarily, provided that the doping of the said zone adjoining the sunken oxide layer pattern is sufficiently high.

The epitaxial layer provided may be of one conductivity type and both the said substrate part and the said zone may be of the opposite conductivity type.

In certain cases, the said zone may be provided, after providing the epitaxial layer of the one conductivity type, by disposing, at the area of the sunken oxide layer pattern to be provided, a surface zone of the opposite conductivity type in the epitaxial layer by diffusion, said zone diffusing, during the oxidation treatment, into the substrate and forming there the said zone which adjoins the oxide.

However, in a preferred form, prior to providing the epitaxial layer, the substrate is provided with the said zone as a surface zone, and, after providing the epitaxial layer, the sunken oxide layer pattern is obtained by an oxidation treatment which is continued until the layer pattern extends throughout the thickness of the epitaxial layer and up to this surface zone in the substrate. An accurate determination of the place of the said zone is possible by providing the zone prior to the epitaxial layer. Furthermore, the dimensions of the zone can be chosen with greater flexibility.

The said zone may comprise parts which, viewed in a direction transverse to the epitaxial layer, extend beside the sunken oxide layer pattern and which may diffuse in the epitaxial layer partly during the oxidation treatment. However, this may be undesirable in some cases, for example, in cases in which very thin epitaxial layers are used. Thus, in one preferred form, the said zone has dimensions such that after providing the sunken oxide layer pattern the layer pattern entirely overlaps the said zone, viewed in a direction transverse to the epitaxial layer.

According to a second aspect of the invention, there is provided a semiconductor device having a semiconductor body comprising a silicon epitaxial layer on a surface of a semiconductor substrate, regions of

one or more semiconductor circuit elements being present in separate semiconductor islands comprising parts of the epitaxial layer which are separated laterally in the layer by oxidized parts of the epitaxial layer, which oxidized parts form parts of an oxide layer pattern sunk over at least part of its thickness in the semiconductor body and extending across the thickness of the epitaxial layer, the islands being electrically isolated from an underlying substrate part by $p-n$ junction isolation, and a zone being locally present at least partly in the said substrate part and adjoining the sunken oxide layer pattern, which zone is of the same conductivity type as the said substrate part and has such a high doping concentration to prevent the formation in the substrate part of undesirable channels adjoining the sunken oxide layer pattern and connecting regions of adjacent islands.

Embodiments of the first and second aspects of the invention will now be described, by way of example, with reference to the accompanying diagrammatic drawings, in which:—

Figure 1 is a plan view of part of one semiconductor device;

Figure 2 is a cross-sectional view taken on the line II—II of Figure 1; and

Figures 3 to 5 are cross-sectional views corresponding to that shown in Figure 2 and taken at three stages during the manufacture of the semiconductor device of Figures 1 and 2 using a method in accordance with the present invention.

The semiconductor device shown in Figures 1 and 2, comprises a semiconductor body of silicon in the form of a silicon epitaxial layer 1 on a surface of a semiconductor substrate 8. Regions 2, 3, 4 and 25 of one or more semiconductor circuit elements 2, 3, 4 are present in separate semiconductor parts or islands 9 to 17 of the epitaxial layer 1. These islands 9 to 17 are separated laterally in the layer by oxidized parts 5 of the epitaxial layer. These oxidized parts 5 form parts of an oxide layer pattern 5 sunk over its thickness in the semiconductor body. At least a portion 51 of the substrate 8 adjacent the said surface is of opposite conductivity type to the epitaxial layer 1. The separate semiconductor parts 9 to 17 are electrically isolated from the substrate 8 by $p-n$ junction isolation. A zone 52 is locally present in the substrate 8 and adjoining the sunken oxide layer pattern 5. This zone 52 is of the same conductivity type as the portion 51 of the substrate 8 adjacent the said surface and has such a high doping concentration to prevent the formation in the substrate of undesirable channels adjoining the sunken oxide layer pattern 5 and connecting regions of adjacent separate semiconductor parts of the epitaxial layer.

It is to be noted that for simplicity Figures 1 and 2 show only a part of the semiconductor device which part comprises only one whole separate part 9 of the epitaxial layer 1. This part 9 comprises a transistor having an emitter zone 2, a base zone 3 and a collector zone 4.

In one form of the present embodiment the substrate 8 is a *p*-type semiconductor body of silicon having a resistivity of approximately from 2 to 5 ohm-cm.

The semiconductor body 8 used as the starting material has a thickness of approximately 250 micron, while the remaining dimensions are chosen to be large enough so as to be able to obtain the desirable number of parts of the epitaxial layer 1 to be provided which parts are insulated from each other.

As shown in Figure 3, a highly doped zone 52 is provided in the surface 53 of the substrate 8, for example, by diffusion of boron. The surface zone 52 is provided prior to the provision of the epitaxial layer as a result of which an accurate determination of the location of the surface zone is possible. The surface concentration of the surface zone 52 is approximately from 10^{19} to 10^{20} boron atoms per ccm.

After the boron diffusion, an *n*-type epitaxial layer 1 having, for example, a thickness of approximately $2\ \mu$ and a resistivity of approximately 0.2 ohm-cm is provided on the surface 53 of the *p*-type substrate 8. The epitaxial layer 1 can be obtained in a manner conventionally used in semiconductor technology by vapour-depositing semiconductor material on the substrate 8. The oxide layer pattern 5 is then provided by means of an oxidation treatment which is continued until the substantially flat oxide layer 5 extends throughout the thickness of the epitaxial layer and down to the surface zone 52 in the substrate 8.

The dimensions and the location of the surface zone 52 have been chosen to be such that after providing the pattern 5 the layer pattern 5 of silicon oxide overlaps the surface zone 52 on all sides viewed in a direction transverse to the epitaxial layer 1, see the plan view of Figure 1. As a result of this the situation is avoided in which parts of the surface zone 52 diffuse in the epitaxial layer 1 beside the layer pattern 5, for example, during the oxidation treatment; such a situation may be undesirable, for example, from a point of view of space saving.

For the oxidation treatment to form the pattern 5, the epitaxial layer 1 is provided with a masking layer 7 (see Figures 4 and 5) which masks against oxidation. In the present embodiment the masking layer 7 consists of silicon nitride, but may also consist, for example, of a double layer of silicon-

oxide and silicon-nitride. The silicon-nitride layer 7 is provided in normal manner, for example, by heating the body (1,8) at a temperature of approximately 1000°C in a gas mixture of SiH_4 and NH_3 , and has a thickness of approximately $0.2\ \mu\text{m}$, which thickness is considerably smaller than that of the pattern 5 to be provided.

By means of a photolithographic process a part of the layer 7 above the surface zone 52 is removed, as is shown in Figure 4, so as to be able to provide the pattern 5.

In order to obtain a pattern 5 which is inset substantially throughout its thickness in the silicon layer 1, the layer 7 masking against oxidation is used as an etching mask, prior to starting the oxidation treatment to remove the silicon layer 1 locally over approximately half its thickness by etching. The grooves 21 are obtained. Etching is carried out in a conventional manner (see Figure 4).

By passing steam at a pressure of approximately 1 atmosphere and at a temperature of approximately 1000°C , the pattern 5 is obtained by oxidation of the layer 1. The oxidation treatment is continued until the resulting pattern 5 reaches at least down to the substrate 8 and the surface zone 52 (see Figure 5).

The epitaxial layer 1 is thus divided in a simple and efficacious manner into parts 9 to 17 which are insulated and separated from each other by the pattern 5. Since the pattern 5 is inset substantially throughout its thickness in the layer 1, the resulting configuration can be treated further by means of planar methods; in addition the pattern 5 consists of silicon oxide of a good quality. Moreover, a highly doped zone 52 preventing channel formation is obtained below the pattern 5.

In a modified form of the method the oxidation treatment may be interrupted and during this interruption the silicon oxide layer already obtained may be removed at least over part of its thickness by etching, the layer 7 being used as an etching mask. An etching treatment preceding the oxidation treatment is not necessary in this case. It is also possible to use no etching treatment at all. In that case, however, a pattern 5 is obtained which projects above the surface of the epitaxial layer 7. Particularly in the case of very thin epitaxial layers, this simplification of the method may be used without any objection. In other cases, the part of the pattern projecting above the epitaxial layer 1 may also be removed by an etching treatment afterwards, the layer 7 serving as an etching mask. It is possible for the pattern 5 to project slightly above the surface of the epitaxial layer 1 or to remain slightly below said surface.

The separate semiconductor parts 9 to 17

of the epitaxial layer 1 are isolated from the substrate 8 by the p - n junction which the n -type layer 1 forms with the p -type substrate 8.

5 The base zone 3 may be provided in normal manner by diffusion of an impurity. The silicon nitride layer 7 may be used as a diffusion mask. In the present embodiment, however, the nitride layer 7 is first removed and replaced by the silicon oxide layer 20 which is used as a diffusion mask in normal manner. The p -type base zone 3 which is obtained, for example, by diffusion of boron, has a thickness of approximately $0.6\ \mu\text{m}$ and adjoins the surface 23 of the insulated part 9.

15 The n -type emitter zone 2, approximately $0.3\ \mu$ thick, which adjoins the surface 23 of the insulated part 9 is then provided in the base zone 3, for example, by diffusion of phosphorus.

20 The collector zone 4 of the transistor (2, 3, 4) is formed by the part 4 which adjoins the base zone 3 of the insulated part 9.

25 It is to be noted that the vertical part 24 of the p - n junction between the base zone 3 and the collector zone 4 is comparatively small so that the capacitance between the base zone 3 and the collector zone 4 is also comparatively small.

30 The collector zone 4 is provided with a contact zone 25 which adjoins the surface 23 of the insulated part 9. This contact zone 25 is of the same conductivity type as and has a higher doping than the collector zone 4. The contact zone 25 may be provided simultaneously with the emitter zone 2 by diffusion of phosphorus.

35 The silicon oxide 20 is provided with apertures 26, 27 and 28, for contacting the zones 2, 3, and 25. For simplicity the contacts are not shown but they may be provided in normal manner and extend in the form of metal layer to cover the insulating layer 20 and the pattern 5.

40 If desirable, a buried layer of the same conductivity type as but of a higher doping than the collector zone 4 may be provided in normal manner. Such a buried layer 30 is shown in broken lines in Figure 2, and forms part of an island with the epi-layer part 9.

45 The dimensions of the epitaxial-layer part 9 and of the zones 2, 3 and 25 in the plan view shown in Figure 1, are not critical in this method and are chosen in accordance with the desirable properties of the transistor.

50 The pattern 5 preferably has approximately the same thickness as the epitaxial layer 1, so that a substantially flat surface can be obtained. For that purpose, the epitaxial layer 1 preferably is not thicker than approximately 2.5 to $3\ \mu\text{m}$ because a

pattern 5 of this thickness and of a good quality can be provided in a reasonable oxidation time.

65 In the form described, the semiconductor body 8 used as the starting material was entirely of the opposite conductivity type. However, it is also possible to use a semiconductor body of which only a surface layer is of the opposite conductivity type and adjoins the supporting surface 53. For example, the semiconductor body 8 may comprise a surface layer 51 of the opposite conductivity type, while an adjoining part 54 is of the one conductivity type and may be connected, for example, to earth for screening purpose and/or may be used as a supply line. The interface between the parts 51 and 54 is diagrammatically denoted by the broken lines 55 in Figures 2 to 5.

70 It will be obvious that many variations are possible within the scope of this invention as defined in the appended Claims. For example, the conductivity types of all the mentioned parts of the semiconductor device described may simultaneously be changed from p -type conductivity into n -type conductivity, and conversely.

75 In addition to transistors, other circuit elements, for example, diodes, resistors or capacitors, can be manufactured in the epitaxial layer.

80 Furthermore, in the case in which the semiconductor body used as the starting material comprises a component layer of the same conductivity type as the epitaxial layer, said component layer may serve as an earth plate or supply line for the semiconductor device in which, for example, a circuit element in the epitaxial layer is connected to the said component layer. This connection may comprise, for example, a connection zone of the one conductivity type provided in the support.

85 Instead of diffusion, various zoned in the semiconductor device may be provided by ion implantation.

90 It is also possible to provide the highly doped surface zone which prevents the formation of channels after providing the epitaxial layer, for example, at the area of the layer pattern to be provided, a surface zone of the opposite conductivity type being formed by diffusion or ion implantation in the epitaxial layer, which zone diffuses into the semiconductor body during the oxidation treatment and forms there the highly doped surface zone adjoining the oxide. This surface zone may be provided, for example, after etching the grooves 21. By ion implantation, the highly doped surface zone can also be provided through the oxide of the layer pattern.

95 WHAT WE CLAIM IS:—

1. A method of manufacturing a semicon-



of the epitaxial layer 1 are isolated from the substrate 8 by the p - n junction which the n -type layer 1 forms with the p -type substrate 8.

5 The base zone 3 may be provided in normal manner by diffusion of an impurity. The silicon nitride layer 7 may be used as a diffusion mask. In the present embodiment, however, the nitride layer 7 is first removed and replaced by the silicon oxide layer 20
10 which is used as a diffusion mask in normal manner. The p -type base zone 3 which is obtained, for example, by diffusion of boron, has a thickness of approximately $0.6\text{ }\mu\text{m}$ and adjoins the surface 23 of the insulated part 9.

15 The n -type emitter zone 2, approximately $0.3\text{ }\mu$ thick, which adjoins the surface 23 of the insulated part 9 is then provided in the base zone 3, for example, by diffusion of phosphorus.

20 The collector zone 4 of the transistor (2, 3, 4) is formed by the part 4 which adjoins the base zone 3 of the insulated part 9.

25 It is to be noted that the vertical part 24 of the p - n junction between the base zone 3 and the collector zone 4 is comparatively small so that the capacitance between the base zone 3 and the collector zone 4 is also comparatively small.

30 The collector zone 4 is provided with a contact zone 25 which adjoins the surface 23 of the insulated part 9. This contact zone 25 is of the same conductivity type as and has a higher doping than the collector zone 4. The contact zone 25 may be provided simultaneously with the emitter zone 2 by diffusion of phosphorus.

35 The silicon oxide 20 is provided with apertures 26, 27 and 28, for contacting the zones 2, 3, and 25. For simplicity the contacts are not shown but they may be provided in normal manner and extend in the form of metal layer to cover the insulating layer 20 and the pattern 5.

40 If desirable, a buried layer of the same conductivity type as but of a higher doping than the collector zone 4 may be provided in normal manner. Such a buried layer 30 is shown in broken lines in Figure 2, and forms part of an island with the epi-layer part 9.

45 The dimensions of the epitaxial-layer part 9 and of the zones 2, 3 and 25 in the plan view shown in Figure 1, are not critical in this method and are chosen in accordance with the desirable properties of the transistor.

50 The pattern 5 preferably has approximately the same thickness as the epitaxial layer 1, so that a substantially flat surface can be obtained. For that purpose, the epitaxial layer 1 preferably is not thicker than approximately $2.5\text{ to }3\text{ }\mu\text{m}$ because a

65 pattern 5 of this thickness and of a good quality can be provided in a reasonable oxidation time.

70 In the form described, the semiconductor body 8 used as the starting material was entirely of the opposite conductivity type. However, it is also possible to use a semiconductor body of which only a surface layer is of the opposite conductivity type and adjoins the supporting surface 53. For example, the semiconductor body 8 may
75 comprise a surface layer 51 of the opposite conductivity type, while an adjoining part 54 is of the one conductivity type and may be connected, for example, to earth for screening purpose and/or may be used as a supply line. The interface between the parts 51 and 54 is diagrammatically denoted by the broken lines 55 in Figures 2 to 5.

80 It will be obvious that many variations are possible within the scope of this invention as defined in the appended Claims. For example, the conductivity types of all the mentioned parts of the semiconductor device described may simultaneously be changed from p -type conductivity into n -type conductivity, and conversely.

85 In addition to transistors, other circuit elements, for example, diodes, resistors or capacitors, can be manufactured in the epitaxial layer.

90 Furthermore, in the case in which the semiconductor body used as the starting material comprises a component layer of the same conductivity type as the epitaxial layer, said component layer may serve as an earth plate or supply line for the semiconductor device in which, for example, a circuit element in the epitaxial layer is connected to the said component layer. This connection may comprise, for example, a connection zone of the one conductivity type provided in the support.

95 Instead of diffusion, various zoned in the semiconductor device may be provided by ion implantation.

100 It is also possible to provide the highly doped surface zone which prevents the formation of channels after providing the epitaxial layer, for example, at the area of the layer pattern to be provided, a surface zone of the opposite conductivity type being formed by diffusion or ion implantation in the epitaxial layer, which zone diffuses into the semiconductor body during the oxidation treatment and forms there the highly doped surface zone adjoining the oxide. This surface zone may be provided, for example, after etching the grooves 21. By ion implantation, the highly doped surface zone can also be provided through the oxide of the layer pattern.

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WHAT WE CLAIM IS:—

1. A method of manufacturing a semicon-



ductor device comprising providing a silicon epitaxial layer on a semiconductor substrate to form a semiconductor body, and subjecting the epitaxial layer to an oxidation treatment while locally masking the surface of the epitaxial layer against oxidation and so causing an oxide of silicon to grow into the unmasked silicon until the grown oxide forms a layer pattern which is sunk over at least part of its thickness in the semiconductor body and extends across the thickness of the epitaxial layer so as to mutually separate parts of the epitaxial layer for forming islands in which regions of one or more semiconductor circuit elements are to be or are provided, the separate islands being electrically isolated from an underlying substrate part by $p-n$ junction isolation, in which method a zone of the same conductivity type as, but a higher doping than, said substrate part is locally provided at least partly in the said substrate part to adjoin the sunken oxide layer pattern, which zone has such a high doping concentration that the formation in the substrate part of undesirable channels adjoining the sunken oxide layer pattern and connecting regions of adjacent islands is prevented.

2. A method as claimed in Claim 1, in which the epitaxial layer provided is of one conductivity type and both the said substrate part and the said zone are of the opposite conductivity type.

3. A method as claimed in Claim 1 or Claim 2, in which the said zone is provided in the form of a grid pattern to adjoin and lie beneath the sunken oxide layer pattern and to be fully overlapped by the sunken oxide layer pattern, viewed in the direction of thickness of the epitaxial layer.

4. A method as claimed in any of the preceding Claims, in which prior to the provision of the epitaxial layer on a surface of the substrate, impurity introduction is effected into this surface of the substrate for forming the said zone, and the subsequent oxidation treatment is continued until the sunken oxide layer pattern extends to the said zone.

5. A method of manufacturing a semiconductor device, substantially as herein described with reference to Figures 1 to 5 of the accompanying drawings.

6. A semiconductor device manufactured by a method claimed in any of the preceding Claims.

7. A semiconductor device having a semiconductor body comprising a silicon epitaxial layer on a surface of a semiconductor substrate, regions of one or more semiconductor circuit elements being present in separate semiconductor islands comprising parts of the epitaxial layer which are separated laterally in the layer by oxidized parts of the epitaxial layer, which oxidized parts form parts of an oxide layer pattern sunk over at least part of its thickness in the semiconductor body and extending across the thickness of the epitaxial layer, the islands being electrically isolated from an underlying substrate part by $p-n$ junction isolation, and a zone being locally present at least partly in the said substrate part and adjoining the sunken oxide layer pattern, which zone is of the same conductivity type as the said substrate part and has such a high doping concentration to prevent the formation in the substrate part of undesirable channels adjoining the sunken oxide layer pattern and connecting regions of adjacent islands.

8. A semiconductor device as claimed in Claim 7, in which the epitaxial layer is of one conductivity type and both the said substrate part and the said zone are of the opposite conductivity type.

9. A semiconductor device as claimed in Claim 7 or Claim 8, in which the said zone is in the form of a grid pattern which adjoins and lies beneath the sunken oxide layer pattern and is fully overlapped by the sunken oxide layer pattern, viewed in the direction of thickness of the epitaxial layer.

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