

CLAIMS

What is claimed is:

1. A method comprising:
 - establishing, by a processing device, a target value of programmed bits for each programming distribution of a set of programming distributions of a memory sub-system;
 - applying a read voltage level to determine a measured value of programmed bits in one or more programming distributions of the set of programming distributions;
 - comparing the target value of programmed bits to the measured value of programmed bits to determine a comparison result; and
 - executing an action in view of the comparison result.
2. The method of claim 1, wherein the comparison result indicates the measured value of programmed bits is substantially equal to the target value of programmed bits; and wherein the action comprises executing a read operation using the read voltage level.
3. The method of claim 1, wherein the comparison result indicates the measured value of programmed bits is greater than the target value of programmed bits; and wherein the action comprises decreasing the read voltage level to an adjusted read voltage level.
4. The method of claim 3, further comprising:
 - applying the adjusted read voltage level to determine an updated measured value of programmed bits;
 - comparing the updated measure value of programmed bits to the target value of programmed bits to determine an updated comparison result, wherein the updated comparison result indicates the updated measured value of programmed bits is substantially equal to the target value of programmed bits; and
 - executing a subsequent action in view of the updated comparison result, wherein the subsequent action comprises executing the read operation using the adjusted read voltage level.
5. The method of claim 1, wherein the comparison result indicates the measured value of programmed bits is less than the target value of programmed bits; and wherein the action comprises increasing the read voltage level to an adjusted read voltage level.

6. The method of claim 5, further comprising:
applying the adjusted read voltage level to determine an updated measured value of programmed bits;
comparing the updated measure value of programmed bits to the target value of programmed bits to determine an updated comparison result, wherein the updated comparison result indicates the updated measured value of programmed bits is substantially equal to the target value of programmed bits; and
executing a subsequent action in view of the updated comparison result, wherein the subsequent action comprises executing the read operation using the adjusted read voltage level.
7. The method of claim 1, wherein the target value of programmed bits for a first programming distribution comprises a target ratio of a first number of programmed bits in the first programming distribution to a second number of erased bits.
8. The method of claim 1, wherein a summation function is executed to determine a count of programmed bits corresponding to the one or more programming distributions in view of the read voltage level.
9. A non-transitory computer readable medium comprising instructions, which when executed by a processing device, cause the processing device to perform operations comprising:
establishing, by a processing device, a target value of programmed bits for a set of programming distributions of a memory sub-system, wherein the target value of programmed bits comprises an equal number of programmed bits for each programming distribution of the set of programming distributions;
applying a first read voltage level to a word line portion of the memory sub-system;
executing a summation function to determine a cumulative count of programmed bits in one or more programming distributions corresponding to the first read voltage level;
determining a measured value of programmed bits in view of the cumulative count of programmed bits;
comparing the target value of programmed bits to the measured value of programmed bits to determine a comparison result;
setting an adjusted read voltage level in view of the comparison result; and

applying the adjusted read voltage level to the word line portion of the memory sub-system.

10. The non-transitory computer readable medium of claim 9, wherein the adjusted read voltage level is generated by decreasing the first read voltage level in response to the comparison result indicating the measured value of programmed bits is greater than the target value of programmed bits.

11. The non-transitory computer readable medium of claim 9, wherein the adjusted read voltage level is generated by increasing the first read voltage level in response to the comparison result indicating the measured value of programmed bits is less than the target value of programmed bits.

12. The non-transitory computer readable medium of claim 9, the operation further comprising:

determining an updated measured ratio of programmed bits to erased bits in view of an updated cumulative count of programmed bits corresponding to the adjusted read voltage level; and

executing a read operation in response to determining the updated measured ratio of programmed bits to erased bits is substantially equal to the target ratio of programmed bits to erased bits.

13. The non-transitory computer readable medium of claim 9, wherein the target value of programmed bits for a first programming distribution comprises a target ratio of a first number of programmed bits in the first programming distribution to a second number of erased bits.

14. A system comprising:

a memory device; and

a processing device, operatively coupled with the memory device, to perform operations comprising:

establishing a target value of programmed bits for each programming distribution of a set of programming distributions of a memory sub-system;

applying a read voltage level to determine a measured value of programmed bits in one or more programming distributions of the set of programming distributions;

comparing the target value of programmed bits to the measured value of programmed bits to determine a comparison result; and
executing an action in view of the comparison result.

15. The system of claim 14, wherein the comparison result indicates the measured value of programmed bits is substantially equal to the target value of programmed bits; and wherein the action comprises executing a read operation using the read voltage level.

16. The system of claim 14, wherein the comparison result indicates the measured value of programmed bits is greater than the target value of programmed bits; and wherein the action comprises decreasing the read voltage level to an adjusted read voltage level.

17. The system of claim 16, the operations further comprising:

applying the adjusted read voltage level to determine an updated measured value of programmed bits;

comparing the updated measure value of programmed bits to the target value of programmed bits to determine an updated comparison result, wherein the updated comparison result indicates the updated measured value of programmed bits is substantially equal to the target value of programmed bits; and

executing a subsequent action in view of the updated comparison result, wherein the subsequent action comprises executing the read operation using the adjusted read voltage level.

18. The system of claim 14, wherein the comparison result indicates the measured value of programmed bits is less than the target value of programmed bits; and wherein the action comprises increasing the read voltage level to an adjusted read voltage level.

19. The system of claim 18, the operations further comprising:

applying the adjusted read voltage level to determine an updated measured value of programmed bits;

comparing the updated measure value of programmed bits to the target value of programmed bits to determine an updated comparison result, wherein the updated comparison result indicates the updated measured value of programmed bits is substantially equal to the target value of programmed bits; and

executing a subsequent action in view of the updated comparison result, wherein the subsequent action comprises executing the read operation using the adjusted read voltage level.

20. The system of claim 14, wherein the target value of programmed bits for a first programming distribution comprises a target ratio of a first number of programmed bits in the first programming distribution to a second number of erased bits.