

(19) World Intellectual Property
Organization
International Bureau



(43) International Publication Date
22 January 2004 (22.01.2004)

PCT

(10) International Publication Number
WO 2004/007798 A1

- (51) International Patent Classification⁷: **C23C 18/42**
- (21) International Application Number:
PCT/EP2002/009997
- (22) International Filing Date:
6 September 2002 (06.09.2002)
- (25) Filing Language: English
- (26) Publication Language: English
- (30) Priority Data:
02090262.3 17 July 2002 (17.07.2002) EP
- (71) Applicant (*for all designated States except US*):
ATOTECH DEUTSCHLAND GMBH [DE/DE];
Erasmusstrasse 20, 10553 Berlin (DE).
- (72) Inventors; and
- (75) Inventors/Applicants (*for US only*): **SCHREIER, Hans-Jürgen** [DE/DE]; Beethovenweg 12, 16727 Velten (DE). **MAHLKOW, Hartmut** [DE/DE]; Handjerystrasse 85, 12159 Berlin (DE).
- (74) Agent: **EFFERT, BRESSEL UND KOLLEGEN**;
Radickestrasse 48, 12489 Berlin (DE).
- (81) Designated States (*national*): AE, AG, AL, AM, AT, AU, AZ, BA, BB, BG, BR, BY, BZ, CA, CH, CN, CO, CR, CU, CZ, DE, DK, DM, DZ, EC, EE, ES, FI, GB, GD, GE, GH, GM, HR, HU, ID, IL, IN, IS, JP, KE, KG, KP, KR, KZ, LC, LK, LR, LS, LT, LU, LV, MA, MD, MG, MK, MN, MW, MX, MZ, NO, NZ, OM, PH, PL, PT, RO, RU, SD, SE, SG, SI, SK, SL, TJ, TM, TN, TR, TT, TZ, UA, UG, US, UZ, VC, VN, YU, ZA, ZM, ZW.
- (84) Designated States (*regional*): ARIPO patent (GH, GM, KE, LS, MW, MZ, SD, SL, SZ, TZ, UG, ZM, ZW), Eurasian patent (AM, AZ, BY, KG, KZ, MD, RU, TJ, TM), European patent (AT, BE, BG, CH, CY, CZ, DE, DK, EE, ES, FI, FR, GB, GR, IE, IT, LU, MC, NL, PT, SE, SK, TR), OAPI patent (BF, BJ, CF, CG, CI, CM, GA, GN, GQ, GW, ML, MR, NE, SN, TD, TG).
- Published:**
— *with international search report*
- For two-letter codes and other abbreviations, refer to the "Guidance Notes on Codes and Abbreviations" appearing at the beginning of each regular issue of the PCT Gazette.*

(54) Title: IMMERSION PLATING OF SILVER

(57) **Abstract:** The problem in forming solderable and bondable layers on printed circuit boards is that the surfaces tarnish after storage of the boards prior to further processing (mounting of the electrical components), thus affecting solderability and bondability. In order to overcome this problem it is suggested to deposit, in a first method step, a first metal which is more noble than copper to the printed circuit board and to plate silver in a second method step with the proviso that the first metal be deposited at a rate that is at most half the rate of plating of silver in the second method step when the first metal is silver.

WO 2004/007798 A1