CLAIMS

We claim:

1. A tunneling field effect transistor (TFET), comprising:

a substrate;

a doped first region, disposed above the substrate, having p-type material selected from a group consisting of Group III-V, IV-IV, and IV of a periodic table;

a doped second region, disposed above the substrate, having transparent or semi-transparent oxide n-type semiconductor material; and

a gate stack coupled to the doped first and second regions.

2. The TFET of claim 1, wherein the transparent or semi-transparent oxide n-type semiconductor material is selected from a group consisting of α-Ga_2-O_3, β-Ga_2-O_3, In_2O_3, and SnO_2.

3. The TFET of claim 1, wherein the TFET is a FinFET, Tri-Gate, or square nano-wire based device.

4. The TFET of claim 1 further comprises a lightly doped n-type material coupled to the gate stack, the lightly doped n-type material separating the first and second doped regions from one another.

5. The TFET of claim 1 further comprises a lightly doped p-type material coupled to the gate stack, the lightly doped p-type material separating the first and second doped regions from one another.

6. The TFET of claim 1, wherein the doped first region is a source region, and wherein the doped second region is a drain region.

7. A tunneling field effect transistor (TFET), comprising:

a substrate;

a doped first region, disposed above the substrate, having p-type organic semiconductor material;

a doped second region, disposed above the substrate, having n-type transparent or semi-transparent oxide semiconductor material; and

a gate stack coupled to the doped source and drain regions.

8. The TFET of claim 7, wherein the p-type organic semiconductor material is selected from a group consisting of P3HT, MDMO-PPV, PEFOT:PSS, CoPc, and CuPc.

9. The TFET of claim 7, wherein the n-type transparent or semi-transparent oxide semiconductor material is selected from a group consisting of α-Ga_2-$O3$, β-Ga_2-O_3, In_2O_3, and SnO_2.

10. The TFET of claim 7, wherein the TFET is a FinFET, Tri-Gate, or square nano-wire based device.

11. The TFET of claim 7 further comprises a lightly doped n-type material coupled to the gate stack, the lightly doped n-type material separating the doped first and second regions from one another.

12. The TFET of claim 7 further comprises a lightly doped p-type material coupled to the gate stack, the lightly doped p-type material separating the doped first and second regions from one another.

13. The TFET of claim 12, wherein the lightly doped p-type material is undoped P3HT, or CuPc or CoPc material.

14. The TFET of claim 7, wherein the doped first region is a source region, and wherein the doped second region is a drain region.

15. A tunneling field effect transistor (TFET), comprising:

a substrate;

a doped first region, disposed above the substrate, having p-type organic semiconductor material;

a doped second region, disposed above the substrate, having n-type organic semiconductor material; and

a gate stack coupled to the doped source and drain regions.

16. The TFET of claim 15, wherein the p-type organic semiconductor material is selected from a group consisting of P3HT, MDMO-PPV, and PEDOT:PSS, CuPc, and CoPc .

17. The TFET of claim 15, wherein the n-type organic semiconductor material is one of F16CuPc or $SnCl_2Pc$.

18. The TFET of claim 15, wherein the TFET is a FinFet, Tri-Gate, or square nano-wire based device.

19. The TFET of claim 15 further comprises a lightly doped n-type organic semiconductor material coupled to the gate stack, the lightly doped n-type material separating the doped first and second regions from one another.

20. The TFET of claim 15 further comprises a lightly doped p-type organic semiconductor material coupled to the gate stack, the lightly doped p-type material separating the doped first and second regions from one another.

21. The TFET of claim 21, wherein the lightly doped p-type material is undoped PFHT material.

22. The TFET of claim 15, wherein the doped first region is a source region, and wherein the doped second region is a drain region.

23. A system comprising:

a memory;

a processor coupled to the memory, the processor having TFETs according to any one of TFET claims 1 to 6; and

a wireless antenna for allowing the processor to communicate with another device.

24. A system comprising:

a memory;

a processor coupled to the memory, the processor having TFETs according to any one of TFET claims 7 to 14; and

a wireless antenna for allowing the processor to communicate with another device.

25. A system comprising:

a memory;

a processor coupled to the memory, the processor having TFETs according to any one of TFET claims 15 to 22; and

a wireless antenna for allowing the processor to communicate with another device.

CLAIMS

We claim:

1. A tunneling field effect transistor (TFET), comprising:

a substrate;

a doped first region, disposed above the substrate, having p-type material selected from a group consisting of Group III-V, IV-IV, and IV of a periodic table;

a doped second region, disposed above the substrate, having transparent or semi-transparent oxide n-type semiconductor material; and

a gate stack coupled to the doped first and second regions.

2. The TFET of claim 1, wherein the transparent or semi-transparent oxide n-type semiconductor material is selected from a group consisting of α-Ga_2-O_3, β-Ga_2-O_3, In_2O_3, and SnO_2.

3. The TFET of claim 1, wherein the TFET is a FinFET, Tri-Gate, or square nano-wire based device.

4. The TFET of claim 1 further comprises a lightly doped n-type material coupled to the gate stack, the lightly doped n-type material separating the first and second doped regions from one another.

5. The TFET of claim 1 further comprises a lightly doped p-type material coupled to the gate stack, the lightly doped p-type material separating the first and second doped regions from one another.

6. The TFET of claim 1, wherein the doped first region is a source region, and wherein the doped second region is a drain region.

7. A tunneling field effect transistor (TFET), comprising:

a substrate;

a doped first region, disposed above the substrate, having p-type organic semiconductor material;

a doped second region, disposed above the substrate, having n-type transparent or semi-transparent oxide semiconductor material; and

a gate stack coupled to the doped source and drain regions.

8. The TFET of claim 7, wherein the p-type organic semiconductor material is selected from a group consisting of P3HT, MDMO-PPV, PEFOT:PSS, CoPc, and CuPc.

9. The TFET of claim 7, wherein the n-type transparent or semi-transparent oxide semiconductor material is selected from a group consisting of α-Ga_2-O3, β-Ga_2-O_3, In_2O_3, and SnO_2.

10. The TFET of claim 7, wherein the TFET is a FinFET, Tri-Gate, or square nano-wire based device.

11. The TFET of claim 7 further comprises a lightly doped n-type material coupled to the gate stack, the lightly doped n-type material separating the doped first and second regions from one another.

12. The TFET of claim 7 further comprises a lightly doped p-type material coupled to the gate stack, the lightly doped p-type material separating the doped first and second regions from one another.

13. The TFET of claim 12, wherein the lightly doped p-type material is undoped P3HT, or CuPc or CoPc material.

14. The TFET of claim 7, wherein the doped first region is a source region, and wherein the doped second region is a drain region.

15. A tunneling field effect transistor (TFET), comprising:

a substrate;

a doped first region, disposed above the substrate, having p-type organic semiconductor material;

a doped second region, disposed above the substrate, having n-type organic semiconductor material; and

a gate stack coupled to the doped source and drain regions.

16. The TFET of claim 15, wherein the p-type organic semiconductor material is selected from a group consisting of P3HT, MDMO-PPV, and PEDOT:PSS, CuPc, and CoPc .

17. The TFET of claim 15, wherein the n-type organic semiconductor material is one of F16CuPc or $SnCl_2Pc$.

18. The TFET of claim 15, wherein the TFET is a FinFet, Tri-Gate, or square nano-wire based device.

19. The TFET of claim 15 further comprises a lightly doped n-type organic semiconductor material coupled to the gate stack, the lightly doped n-type material separating the doped first and second regions from one another.

20. The TFET of claim 15 further comprises a lightly doped p-type organic semiconductor material coupled to the gate stack, the lightly doped p-type material separating the doped first and second regions from one another, wherein the lightly doped p-type material is undoped PFHT material.