CLAIMS

1. A method of accessing memory cells in parallel in a cross-point array comprising:

accessing in parallel a first memory cell disposed between a first selected column and a first selected row, and a second memory cell disposed between a second selected column different from the first selected column and a second selected row different from the first selected row, wherein accessing in parallel includes writing, erasing or reading by simultaneously applying a first access bias between the first selected column and the first selected row during a duration when a first voltage of the first memory cell is reduced to a threshold voltage and applying a second access bias between the second selected column and the second selected row during the duration when a second voltage of the second memory cell is reduced to the threshold voltage.

2. A method of accessing memory cells in parallel in a cross-point array comprising:

accessing in parallel a first memory cell disposed between a first selected column and a first selected row, and a second memory cell, disposed between a second selected column different from the first selected column and a second selected row different from the first selected row, wherein accessing in parallel includes simultaneously applying a first access bias between the first selected column and the first selected row and applying a second access bias between the second selected column and the second selected row;

prior to accessing the first memory cell, thresholding the first memory cell by applying a first threshold bias between the first selected column and the first selected row; and

prior to accessing the second memory cell, thresholding the second memory cell by applying a second threshold bias between the second selected column and the second selected row.

3. The method of Claim 2, wherein accessing in parallel includes applying the first and second access biases lower in magnitude than the first and second threshold biases.

4. The method of Claim 2, wherein accessing in parallel includes applying the first and second access biases that are less than about one third of the first and second threshold biases in magnitude.

5. The method of Claim 2, further comprising, prior to thresholding the second memory cell, releasing the first memory cell from a hold condition by reducing a bias across the first memory cell below a hold voltage and/or reducing a current across the first memory cell below a hold current.

6. The method of Claim 5, further comprising, after releasing the first memory cell from the hold condition, refreshing the first memory cell by applying a refresh bias to the first memory cell.

7. The method of claim 2, wherein thresholding the second memory cell includes thresholding the second memory cell within a recovery period after thresholding the first memory cell.

8. The method of claim 6, wherein thresholding the second memory cell includes thresholding the second memory cell within a recovery period after refreshing the first memory cell.

9. The method of Claim 2, further comprising, prior to thresholding the second memory cell, holding the first memory cell in a thresholded condition by keeping a bias across the first memory cell at or above a hold voltage and/or keeping a current across the first memory cell at or above a hold current.

10. The method of Claim 9, wherein thresholding the second memory cell includes thresholding the second memory cell while holding the first memory cell in a thresholded condition.

11. The method of Claim 2, wherein thresholding the first memory cell includes inhibiting a plurality of first inhibited memory cells by applying a first inhibit bias between the first selected column and a plurality of inhibited rows.

12. The method of Claim 11, wherein thresholding the first memory cell further includes inhibiting a plurality of second inhibited memory cells by applying a second inhibit bias between the first selected row and a plurality of inhibited columns.

13. The method of Claim 12, wherein the second inhibit bias is different from the first inhibit bias.

14. The method of Claim 13, wherein thresholding the first memory cell includes inhibiting a plurality of third inhibited memory cells by applying a third inhibit bias between the inhibited columns and the inhibited rows, wherein the third inhibit bias is different from the first inhibit bias and the second inhibit bias.

15. The method of Claim 14, wherein thresholding the second memory cell includes thresholding the second memory cell chosen from one of the third inhibited memory cells.

16. The method of Claim 12, wherein accessing in parallel includes applying the first access bias that is less than the first inhibit bias and less than the second inhibit bias in voltage.

17. The method of Claim 1, wherein accessing in parallel includes one of simultaneously SET-accessing the first and second memory cells, simultaneously RESET-accessing the first and second memory cells, and simultaneously READ-accessing the first and second memory cells.

18. The method of Claim 1, wherein the first and second memory cells comprise at least one of a selector element and a memory element comprising a chalcogenide material.

19. The method of Claim 18, wherein the first and second memory cells each include the selector element in the form of an ovonic threshold switch.

20. The method of Claim 1, wherein the first access bias includes one of a post-threshold SET access bias, a post-threshold RESET access bias, and a post-threshold READ access bias, and wherein the second access bias includes a different one of a post-threshold SET access bias, a post-threshold RESET access bias, and a post-threshold READ access bias.

21. A memory device configured to access memory cells in parallel in a cross-point array comprising:

a memory controller configured to write, erase or read in parallel a first memory cell, the first memory cell disposed between a first selected column and a first selected row, and a second memory cell, the second memory cell disposed between a second selected column different from the first selected column and a second selected row different from the first selected row, wherein the memory controller is configured to simultaneously apply a first access bias between the first selected column and the first selected row during a duration when a first voltage of the first memory cell is reduced to a threshold voltage and to apply a second access bias between the second selected column and the second selected row during the duration when a second voltage of the second memory cell is reduced to the threshold voltage.

22. A memory device configured to access memory cells in parallel in a cross-point array comprising:

a memory controller configured to access in parallel a first memory cell, the first memory cell disposed between a first selected column and a first selected row, and a second memory cell, the second memory cell disposed between a second selected column different from the first selected column and a second selected row different from the first selected row, wherein the memory controller is configured to simultaneously apply a first access bias between the first selected column and the first selected row and to apply a second

access bias between the second selected column and the second selected row, wherein the memory controller is configured to:

prior to accessing the first memory cell, threshold the first memory cell by applying a first threshold bias between the first selected column and the first selected row, and

prior to accessing the second memory cell, threshold the second memory cell by applying a second threshold bias between the second selected column and the second selected row.

23. The memory device of Claim 22, wherein the memory controller is further configured to access in parallel the first and second memory cells comprising a chalcogenide material after the first and second memory cells are thresholded and while under a hold condition.

24. The memory device of Claim 22, wherein the memory controller is further configured to access in parallel the first and second memory cells comprising a chalcogenide material while the first and second memory cells are post-threshold recovery period.

25. The memory device of Claim 22, wherein the memory controller is further configured to inhibit a plurality of first inhibited memory cells by applying a first inhibit bias between the first selected column and a plurality of inhibited rows.

26. The memory device of Claim 25, wherein the memory controller is further configured to inhibit a plurality of second inhibited memory cells by applying a second inhibit bias between the first selected row and a plurality of inhibited columns.

27. The memory device of Claim 26, wherein the memory controller is further configured to apply a second inhibit bias different from the first inhibit bias.

28. The memory device of Claim 27, wherein the memory controller is further configured to inhibit a plurality of third inhibited memory cells by applying a third inhibit bias between the inhibited columns and the inhibited rows, wherein the third inhibit bias is different from the first inhibit bias and the second inhibit bias.

29. A method of simultaneously accessing a plurality of cells in an array of memory cells, comprising:

selecting a plurality of columns;

selecting a plurality of rows;

simultaneously applying respective access biases between each selected column and each selected row during a duration when a voltage of the memory cell is reduced to a threshold voltage to cause one of a write operation, an erase operation or a read operation to occur on each of the plurality of memory cells.

30. A method of simultaneously accessing a plurality of cells in an array of memory cells, comprising:

selecting a plurality of columns;

selecting a plurality of rows;

simultaneously applying respective access biases between each selected column and each selected row during a duration when a voltage of the memory cell is reduced to a threshold voltage, wherein simultaneously applying respective access biases comprises selecting each cell disposed between a unique selected column and a unique selected row, and wherein the unique selected column and row are not used to access other selected cells.

31. The method of Claim 30, further comprising:

sequentially thresholding each of the selected cells by applying respective threshold biases between selected columns and selected rows.

32. The method of Claim 31, wherein simultaneously accessing the cells comprises simultaneously accessing the selected cells while each of the selected cells are in a thresholded condition.

33. The method of Claim 32, wherein the each of the selected cells is in the thresholded condition following one of a recovery period after thresholding, a refreshing event, and a hold condition.

34. The method of Claim 31 wherein sequentially thresholding includes inhibiting a plurality of first inhibited memory cells by applying a first inhibit bias between a first selected column and a plurality of inhibited rows.

35. The method of Claim 34, wherein sequentially thresholding further includes inhibiting a plurality of second inhibited memory cells by applying a second inhibit bias between the first selected row and a plurality of inhibited columns.

36. The method of Claim 35, wherein the second inhibit bias is different from the first inhibit bias.

37. The method of Claim 36, wherein sequentially thresholding further includes inhibiting a plurality of third inhibited memory cells by applying a third inhibit bias between the inhibited columns and the inhibited rows, wherein the third inhibit bias is different from the first inhibit bias and the second inhibit bias.