

METHOD AND APPARATUS FOR ERROR INJECTION TECHNIQUES

ABSTRACT

A process and implementing computer system in which a power-on self-test (POST) routine initially clears (203) a mask register (111) which is effective to mask or block data from being written to addresses in a synchronous DRAM or SDRAM (107). After disabling interrupts and caches, the tested SDRAM memory (107) is cleared to all "0"s. Sequential data byte lanes are tested by writing bits in a predetermined pattern to inject errors at predetermined bytes in SDRAM, setting selected mask register bits and then writing all "0"s to the predetermined addresses. The tested memory locations are read and compared with the predetermined pattern for errors. Detected errors are noted by recordation and the memory locations are cleared as the method recycles until all of the data byte lanes have been tested and the results recorded.

Figure 1