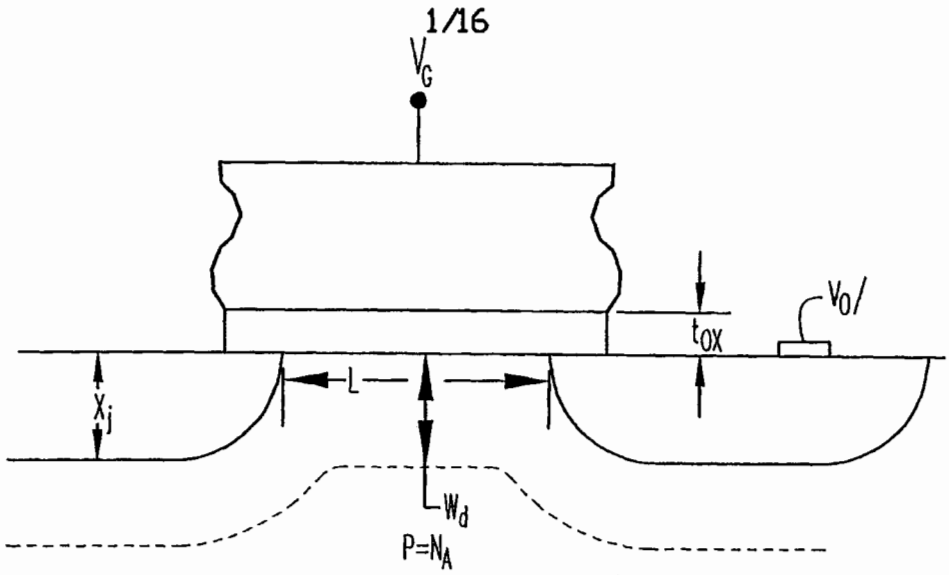


$V_G \longrightarrow V_G/k$ $\quad V_O \longrightarrow V_O/k$

$t_{ox} \longrightarrow t_{ox}/k$

$L \longrightarrow L/k$

$X_j \longrightarrow X_j/k$ JUNCTION DEPTH DECREASED

$W_d \longrightarrow W_d/k$

$N_A \longrightarrow k\ N_A$ SUBSTRATE DOPING INCREASED

Fig. 1

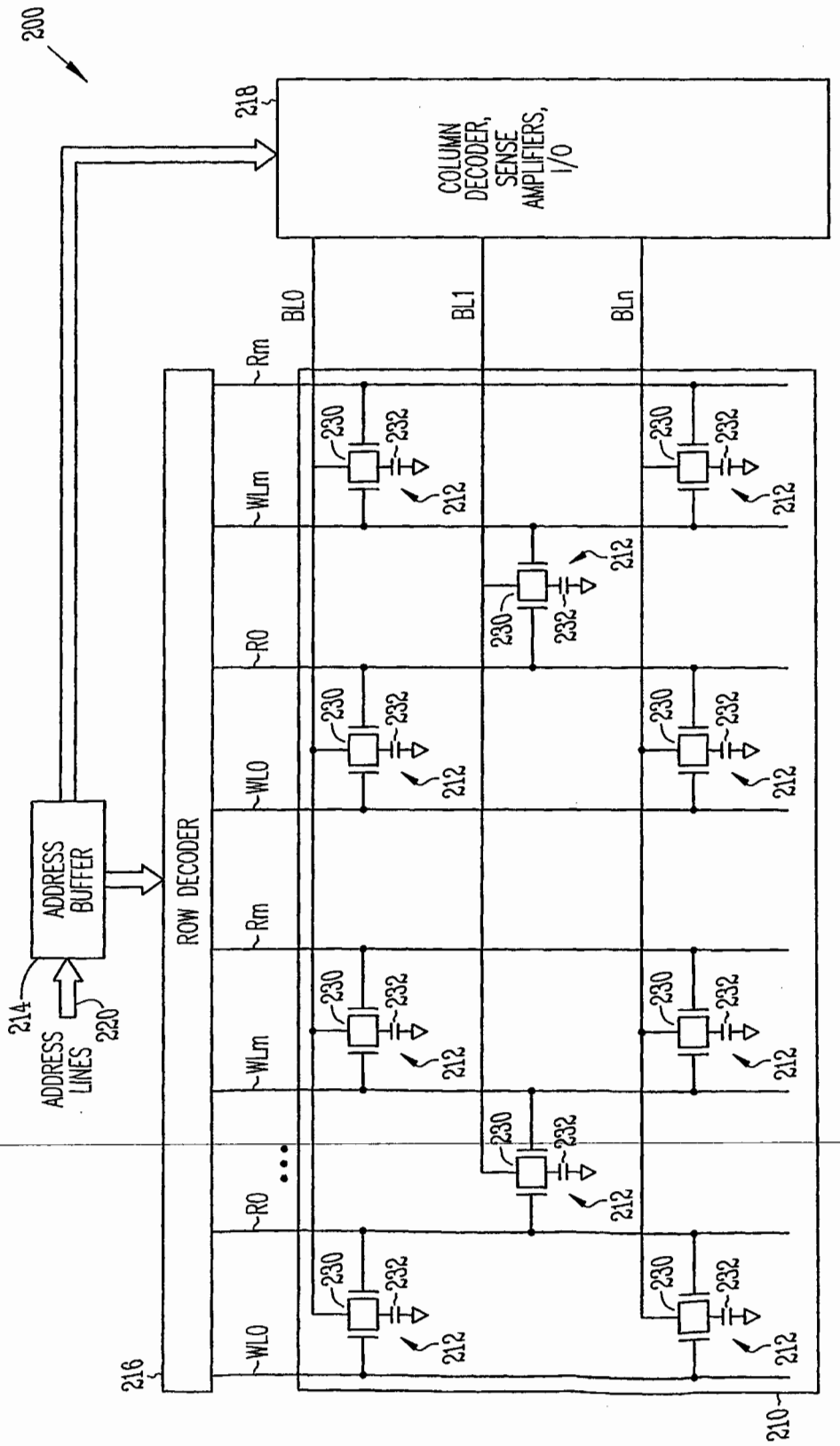

200
218
COLUMN DECODER, SENSE AMPLIFIERS, I/O
BL0
BL1
BLn
Rm
WLm
R0
WL0
ROW DECODER
ADDRESS BUFFER
214
ADDRESS LINES
220
216
210
230
232
212

Fig. 2A

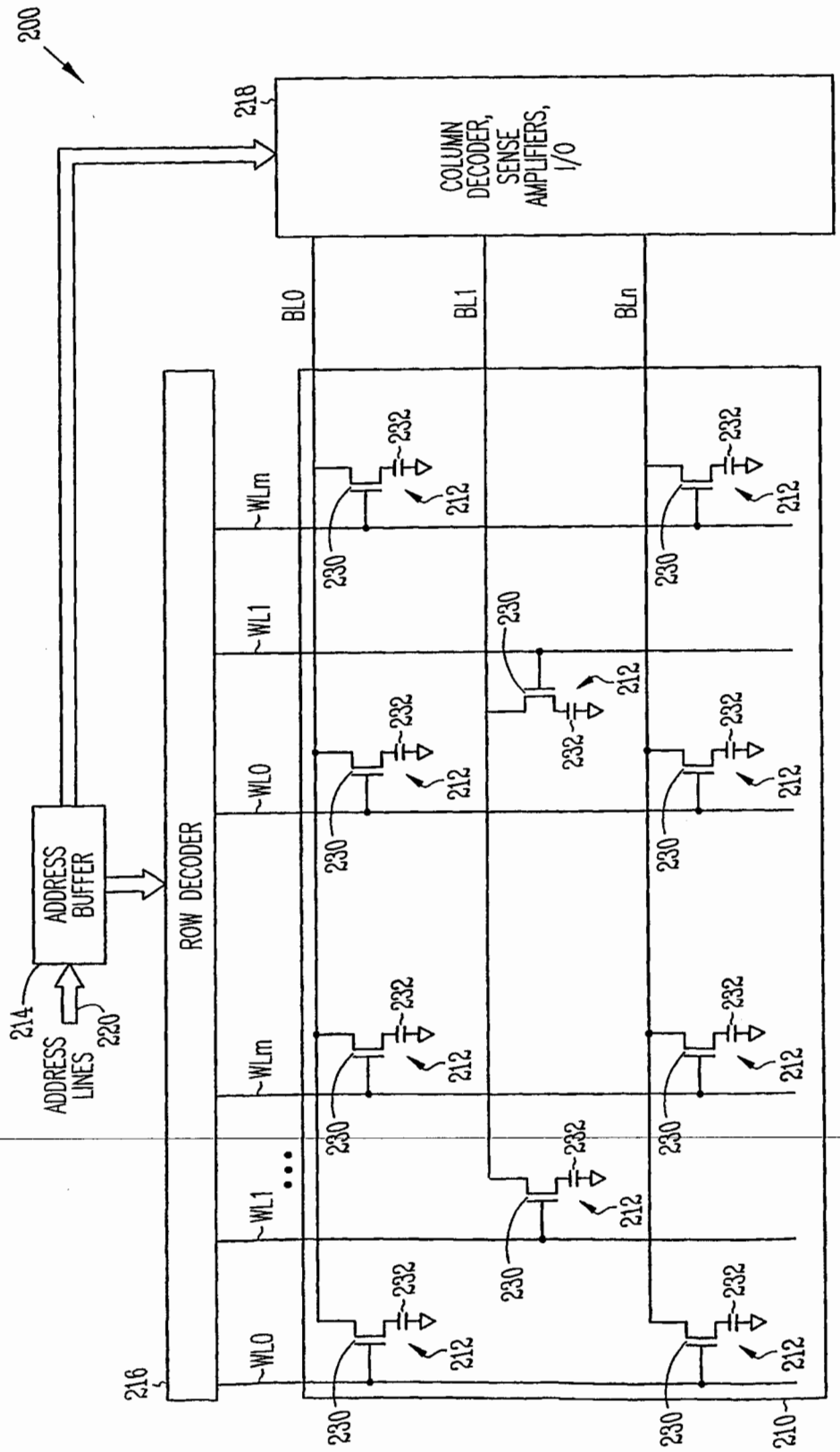

200
218
COLUMN DECODER, SENSE AMPLIFIERS, I/O
BL0
BL1
BLn
ROW DECODER
ADDRESS BUFFER
ADDRESS LINES
214
220
216
WLm
WL1
WL0
230
232
212
210

Fig.2B

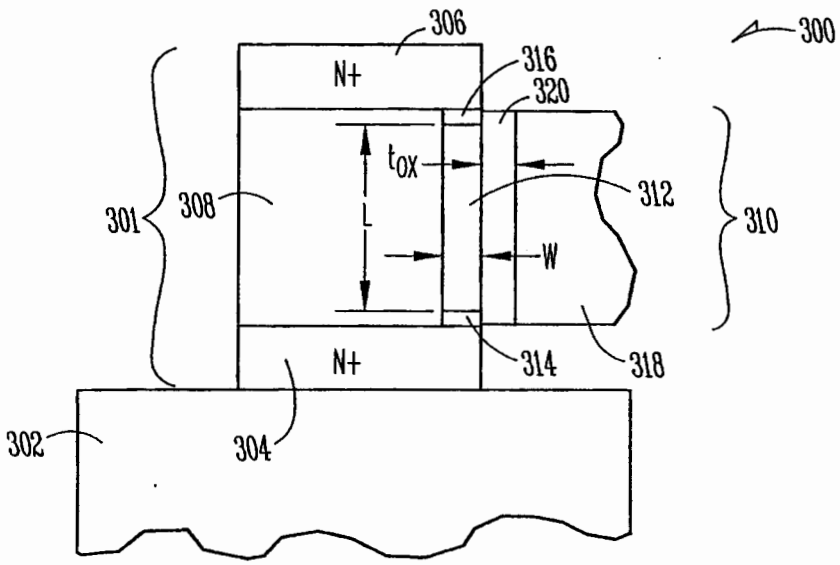


Fig. 3

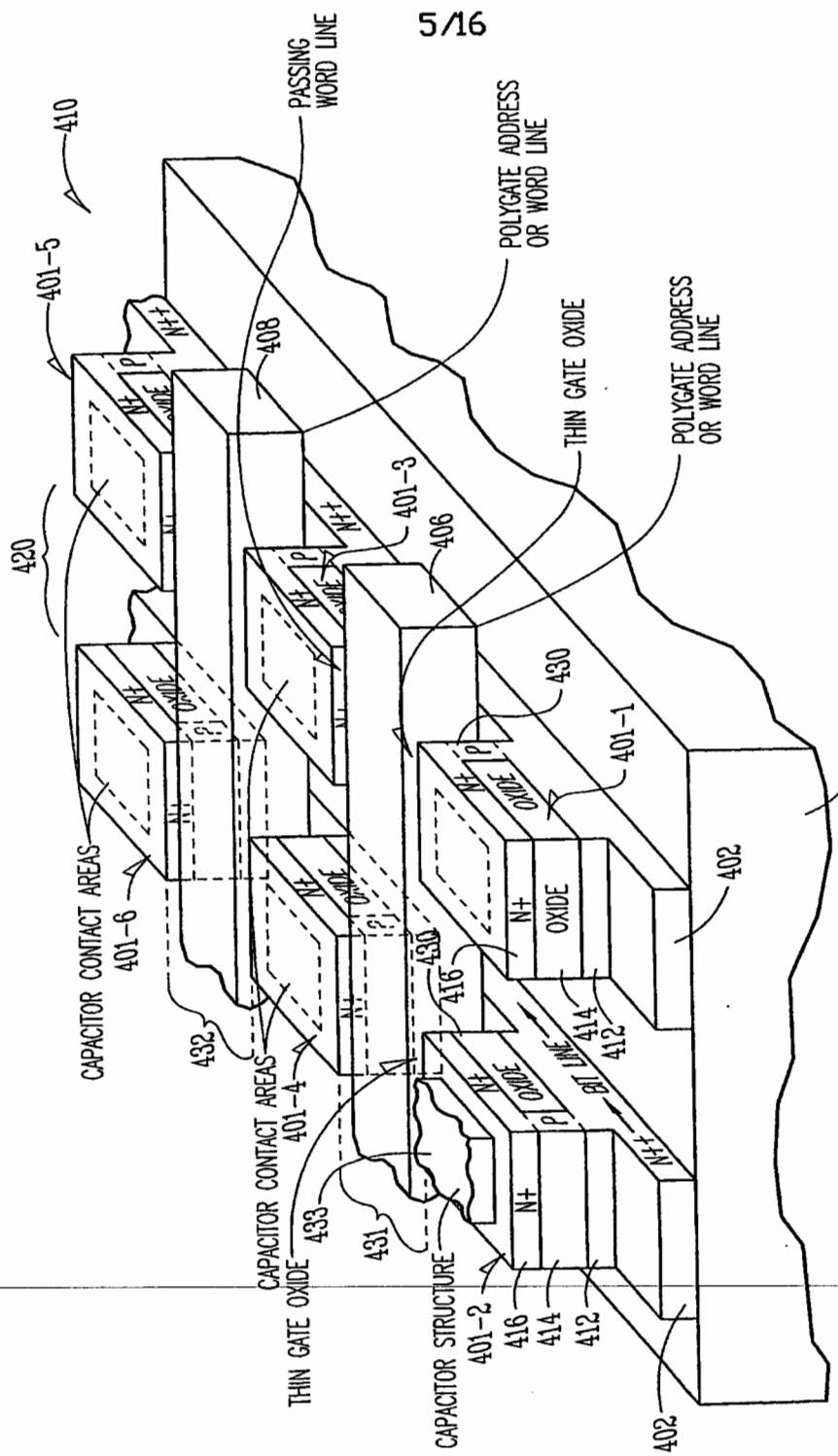

PASSING WORD LINE
POLYGATE ADDRESS OR WORD LINE
THIN GATE OXIDE
POLYGATE ADDRESS OR WORD LINE
410
401-5
408
420
401-3
406
430
401-1
400
402
CAPACITOR CONTACT AREAS
401-6
432
CAPACITOR CONTACT AREAS
401-4
433
THIN GATE OXIDE
431
CAPACITOR STRUCTURE
401-2
416
414
412
N+
OXIDE
P
BIT LINE

Fig. 4A

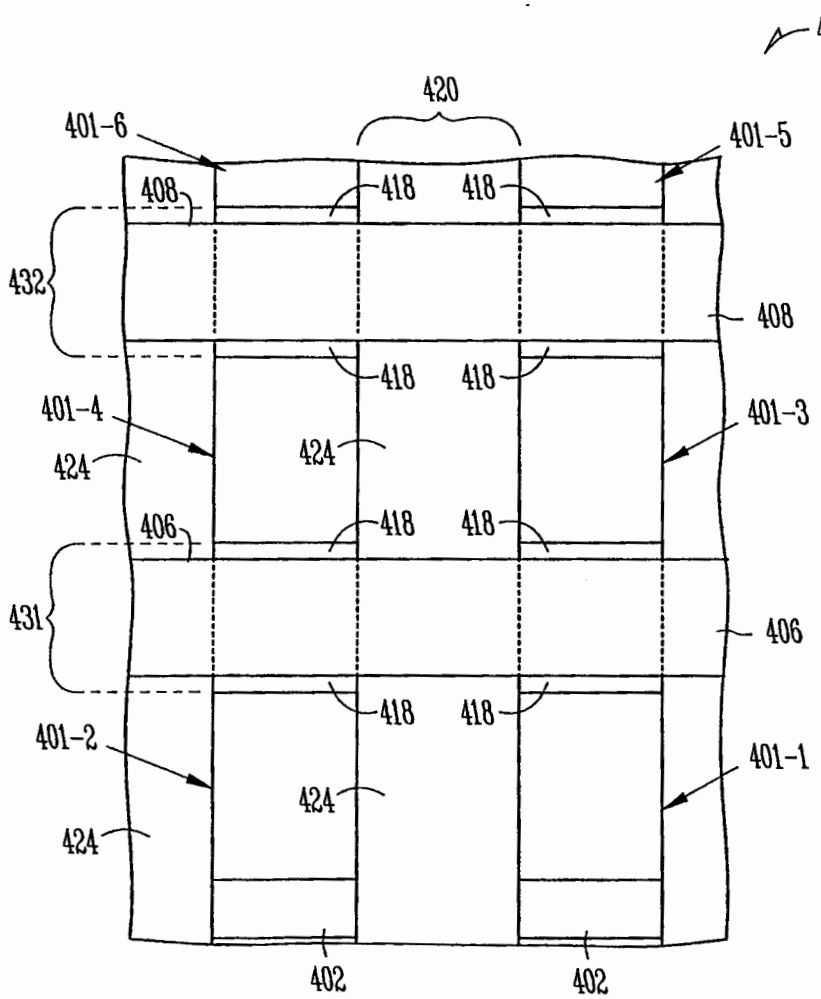

410
420
401-6
401-5
408
418
418
432
408
418
418
401-4
401-3
424
424
406
418
418
431
406
418
418
401-2
401-1
424
424
402
402

Fig. 4B

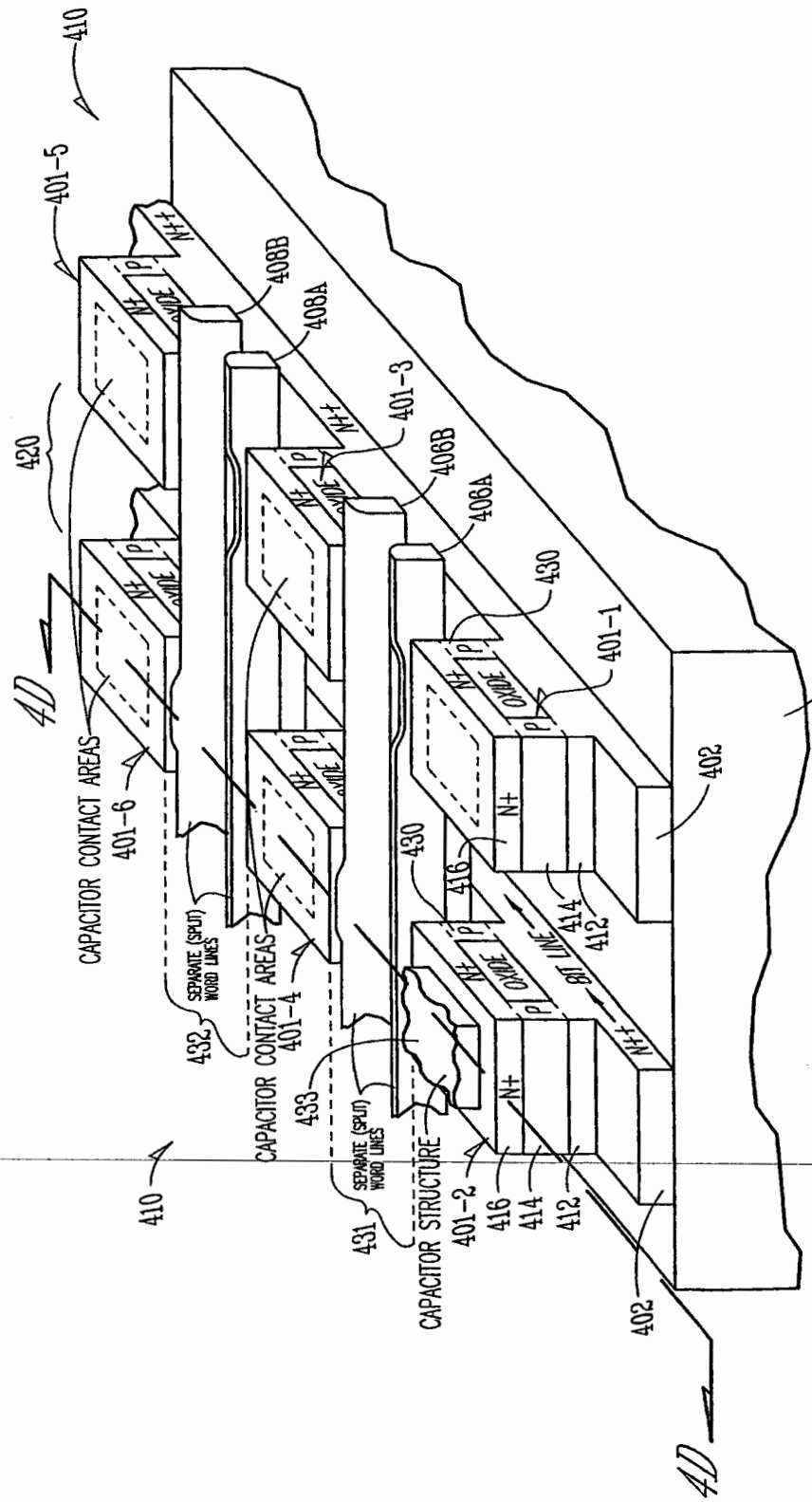

410
401-5
N+
P
OXIDE
408B
408A
401-3
420
406B
406A
430
401-1
400
4D
CAPACITOR CONTACT AREAS
401-6
402
N+
416
414
412
BIT LINE
SEPARATE (SPUT) WORD LINES
432
CAPACITOR CONTACT AREAS
401-4
433
431
CAPACITOR STRUCTURE
401-2

Fig. 4C

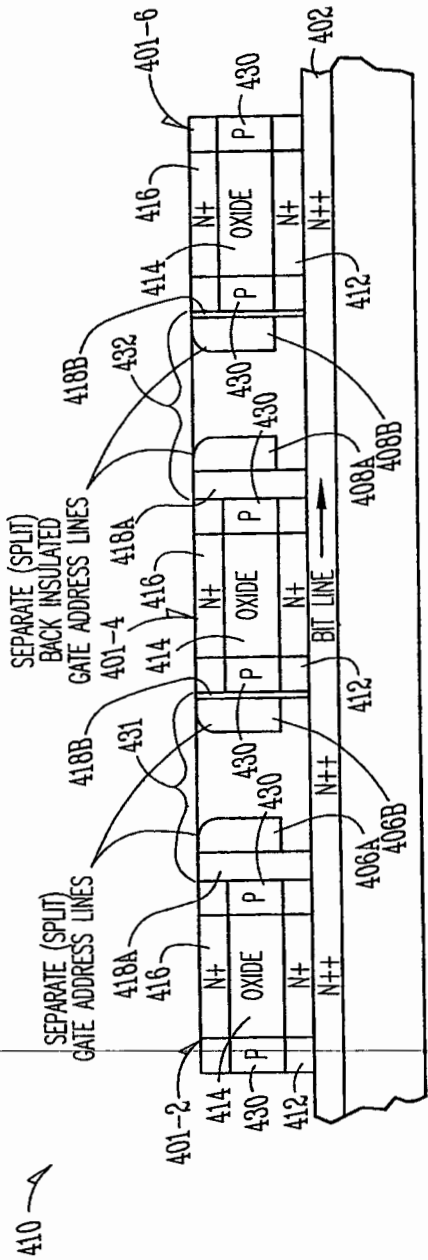

410
401-2
401-4
401-6
SEPARATE (SPLIT) GATE ADDRESS LINES
SEPARATE (SPLIT) BACK INSULATED GATE ADDRESS LINES
BIT LINE
N+
OXIDE
P
N++
402
412
414
416
418A
418B
430
431
432
406A
406B
408A
408B

Fig. 4D

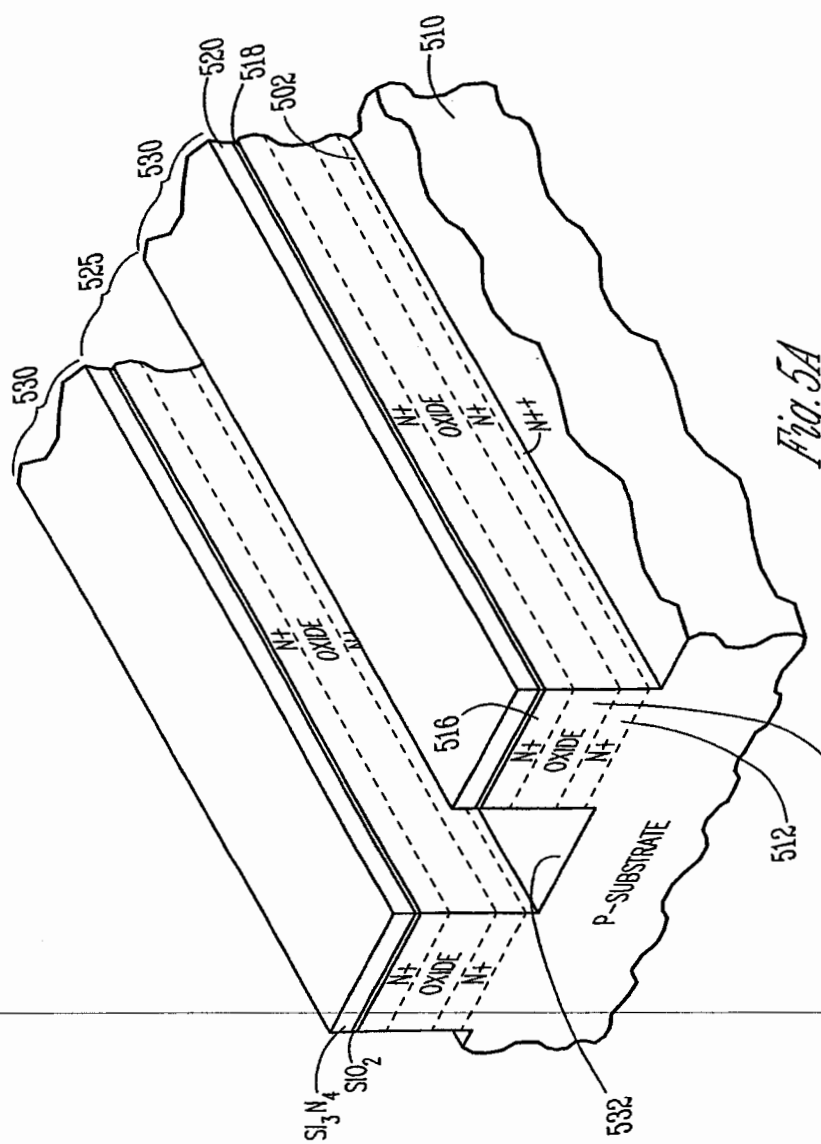

510
520
518
502
530
525
530
N+
OXIDE
N+
N++
516
512
514
P-SUBSTRATE
532
Si_3N_4
SiO_2

Fig. 5A

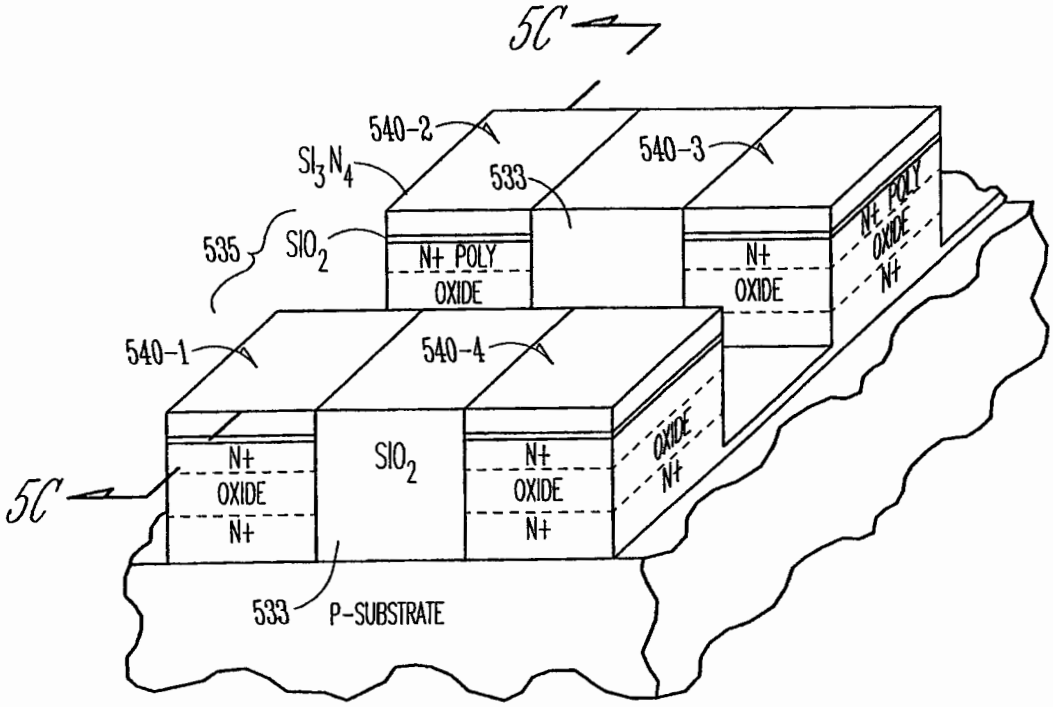

5C
540-2
Si_3N_4
533
540-3
535
SiO_2
N+ POLY
OXIDE
N+
OXIDE
N+ POLY
OXIDE
N+
540-1
540-4
5C
N+
OXIDE
N+
SiO_2
N+
OXIDE
N+
OXIDE
N+
533
P-SUBSTRATE

Fig. 5B

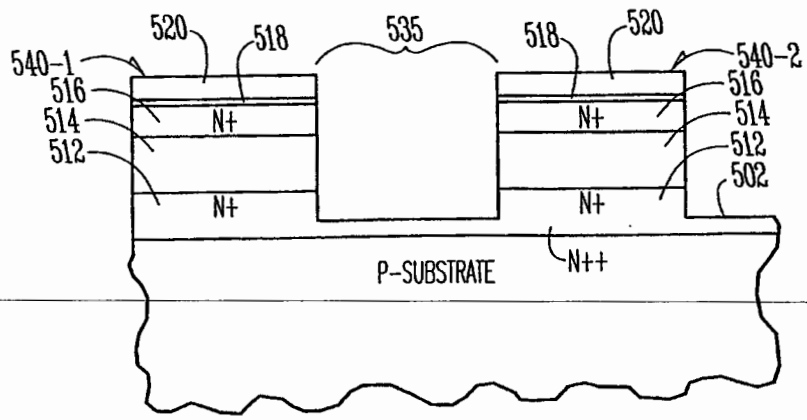

520
518
535
518
520
540-1
540-2
516
516
514
514
512
512
N+
N+
N+
N+
502
P-SUBSTRATE
N++

Fig. 5C

WO 03/083947 PCT/US02/03231

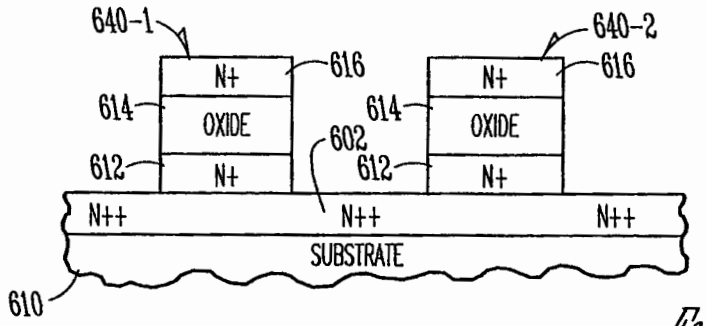


Fig. 6A

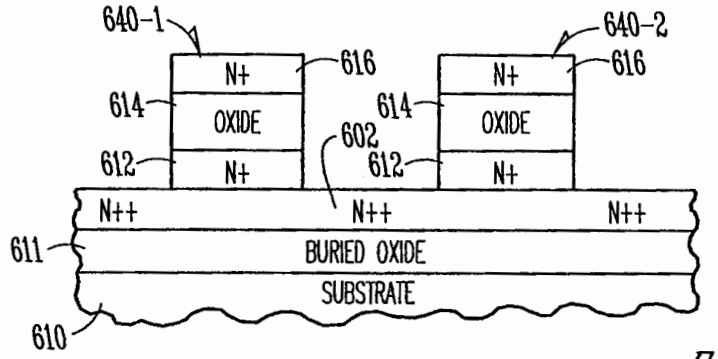


Fig. 6B

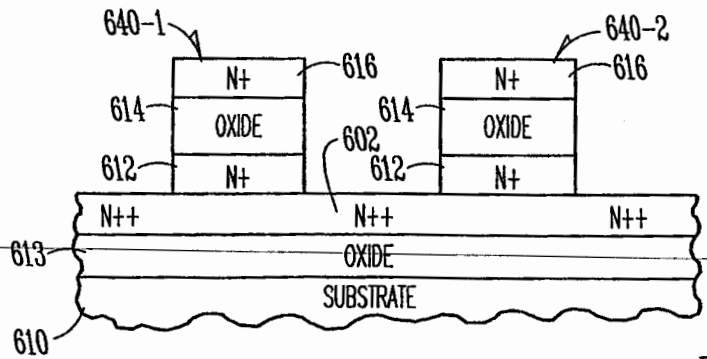


Fig. 6C

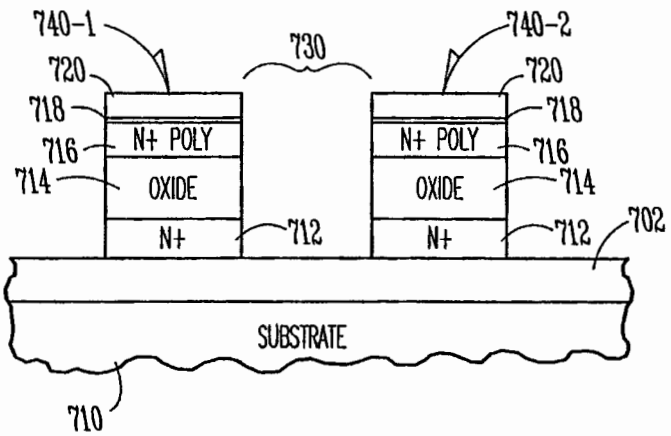


Fig. 7A

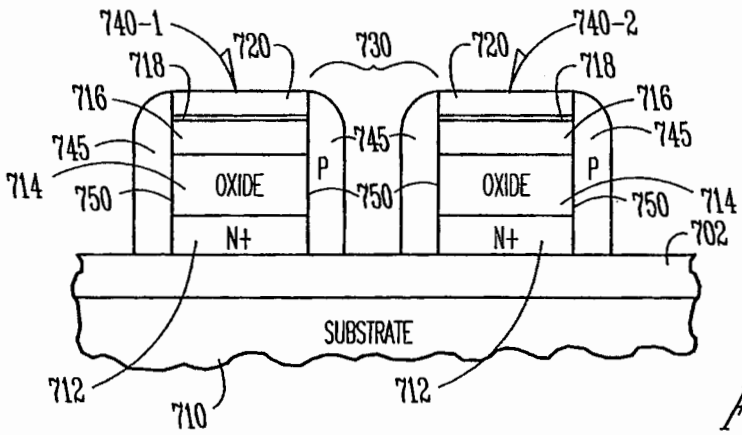


Fig. 7B

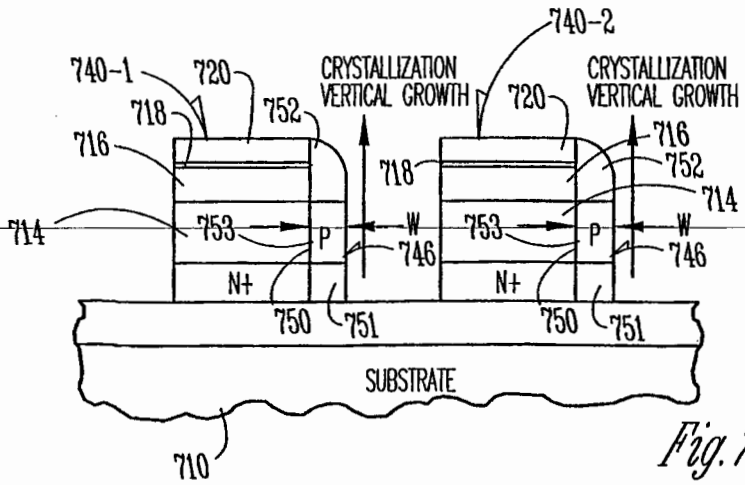


Fig. 7C

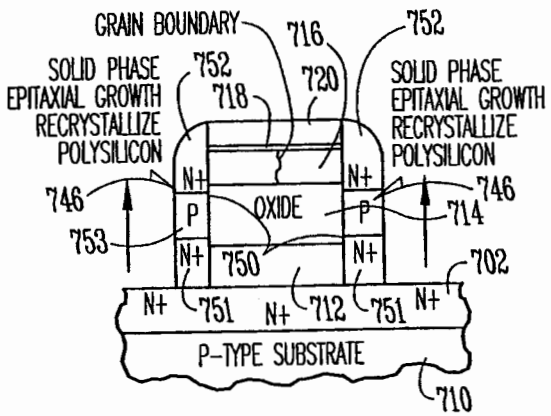

GRAIN BOUNDARY
716
752
SOLID PHASE EPITAXIAL GROWTH RECRYSTALLIZE POLYSILICON
752
718
720
SOLID PHASE EPITAXIAL GROWTH RECRYSTALLIZE POLYSILICON
746
N+
N+
746
P
OXIDE
P
714
753
N+
750
N+
702
N+
751
N+
712
751
N+
P-TYPE SUBSTRATE
710

Fig. 7D

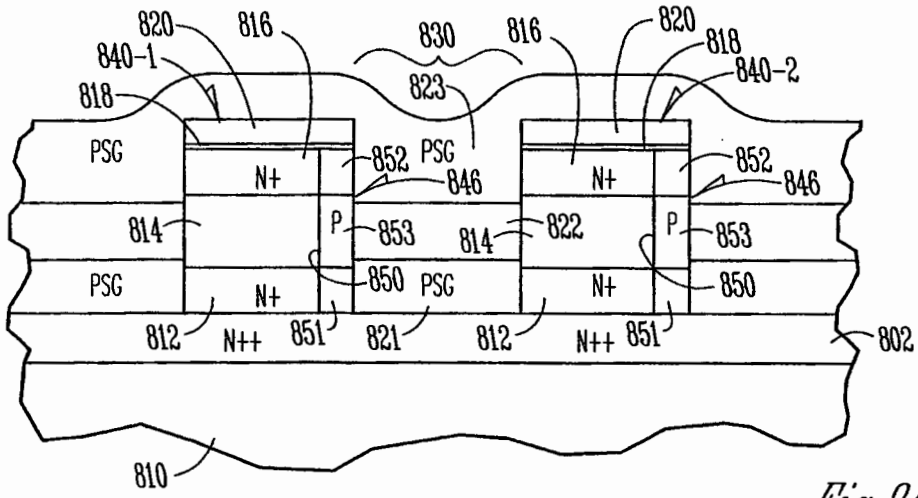


Fig. 8A

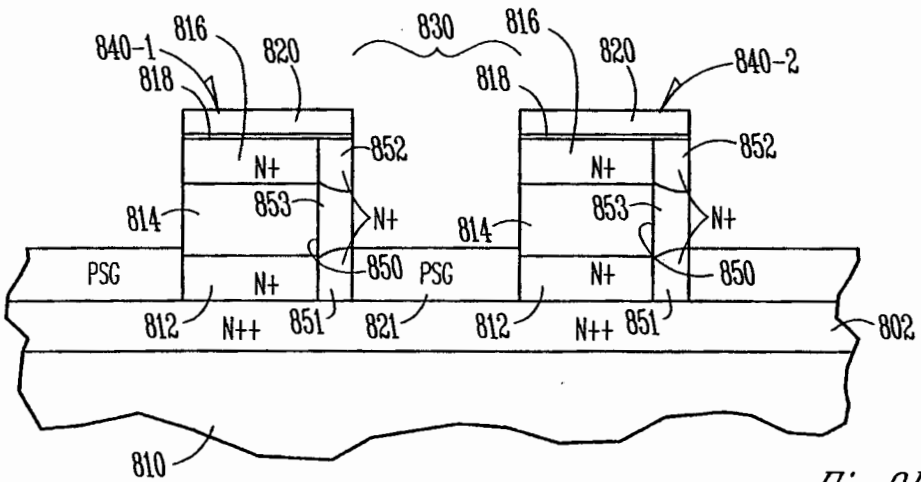


Fig. 8B

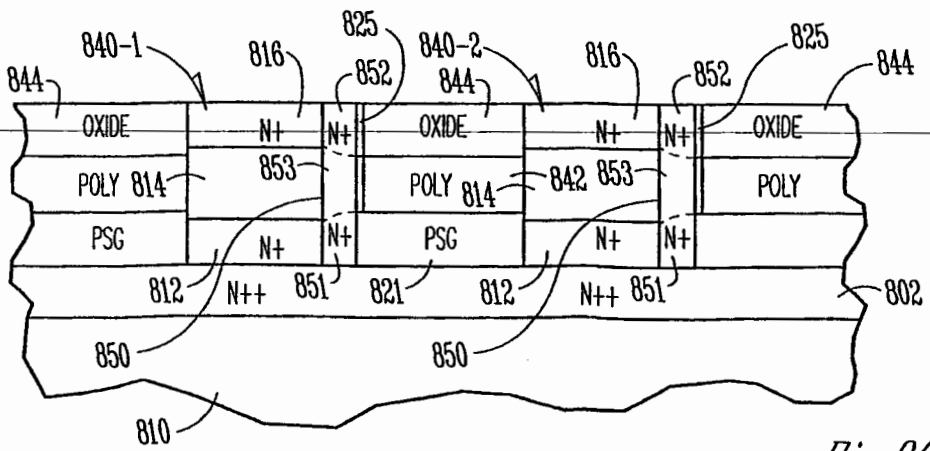


Fig. 8C

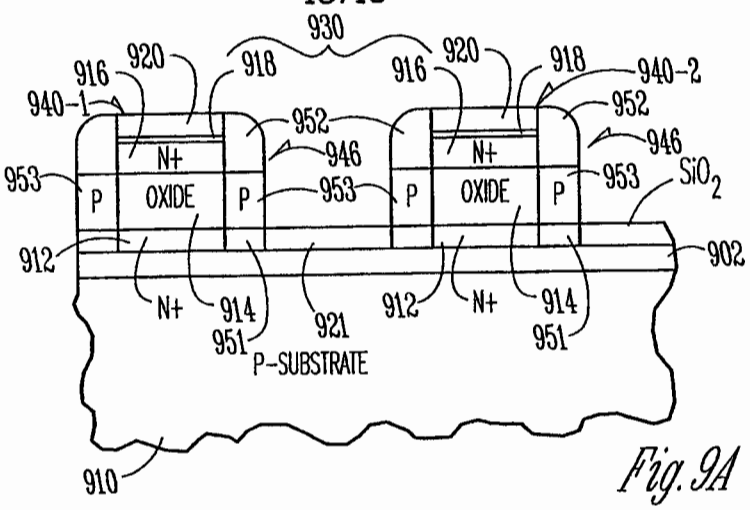


Fig. 9A

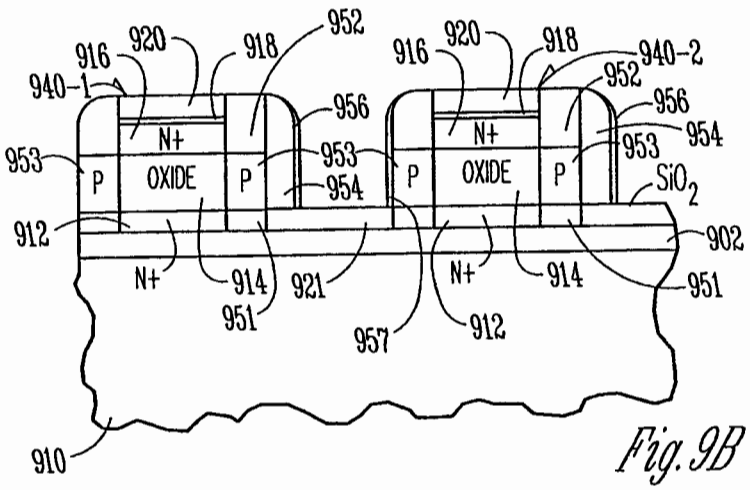


Fig. 9B

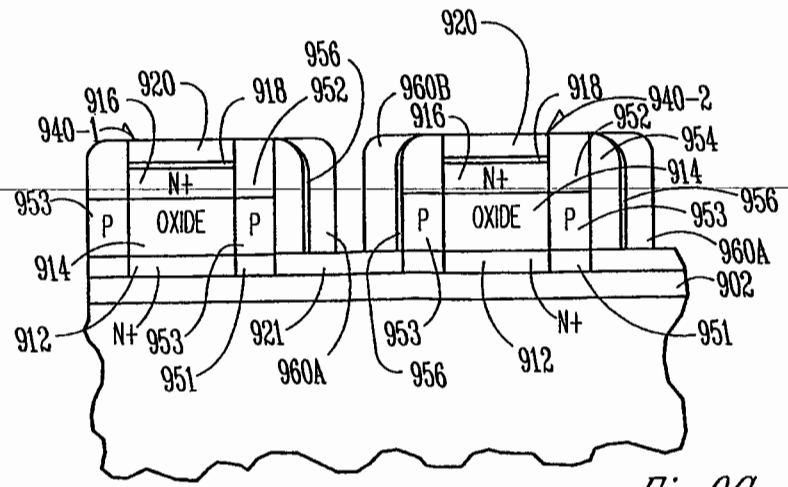


Fig. 9C

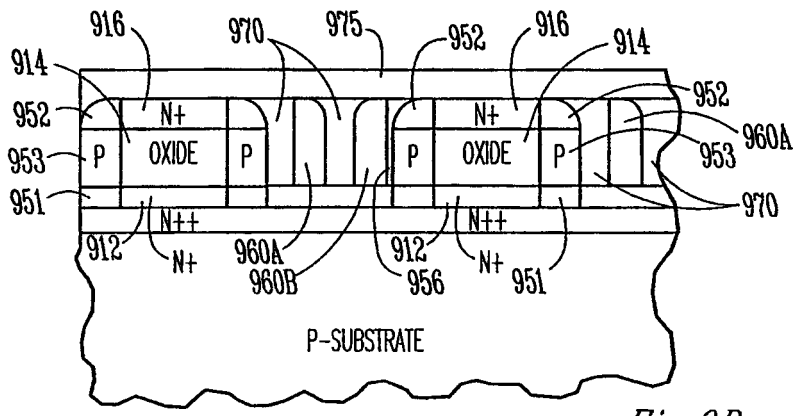

916
970
975
952
916
914
914
952
952
N+
N+
960A
953
P
OXIDE
P
P
OXIDE
P
953
951
970
N++
N++
912
N+
960A
960B
912
956
N+
951
P-SUBSTRATE

Fig. 9D