

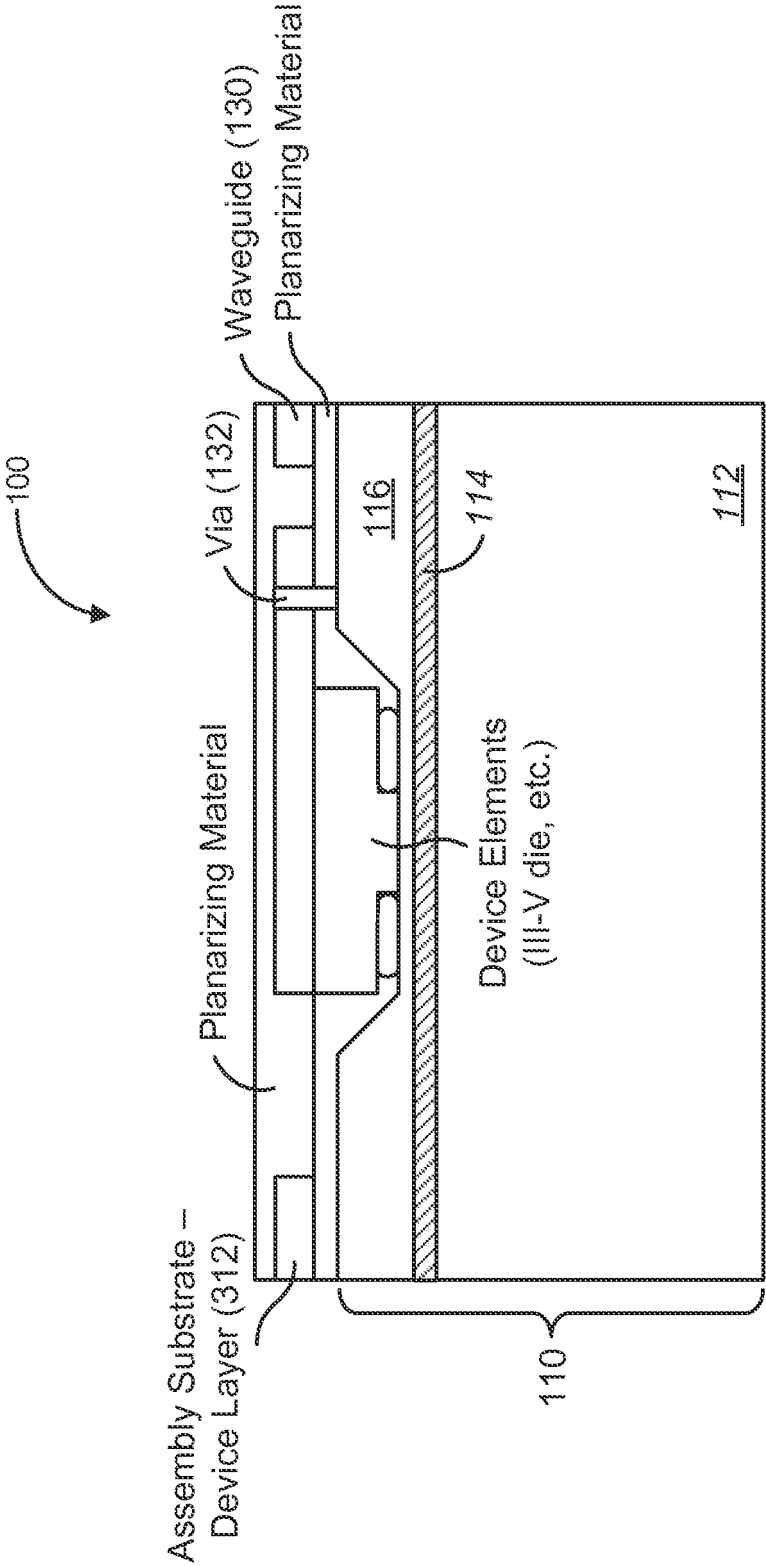


FIG. 1

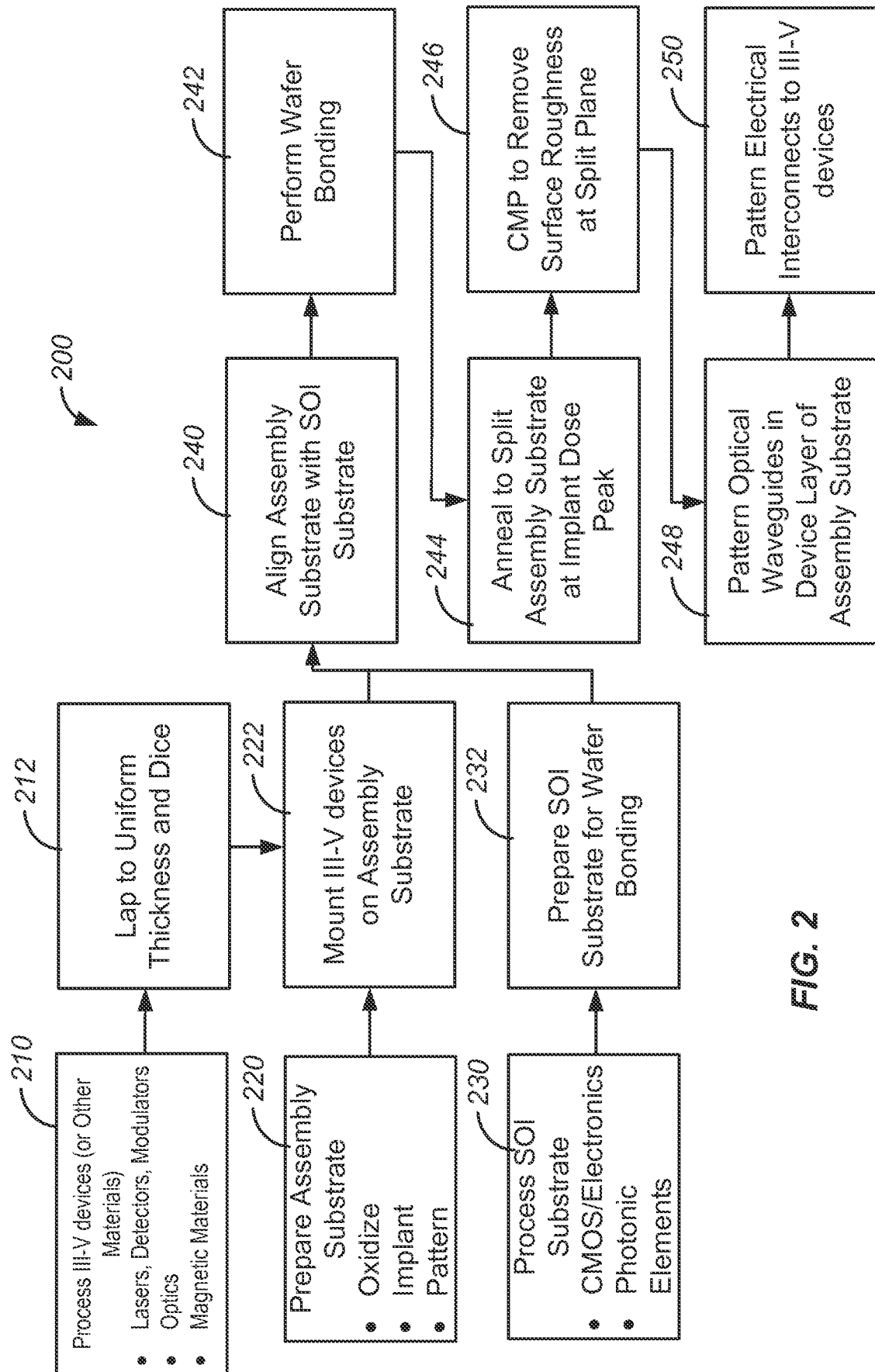


FIG. 2

Processed SOI Substrate

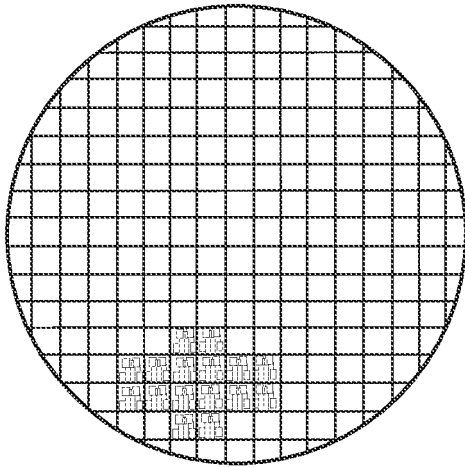


FIG. 3A

Processed and Diced III-V Substrate

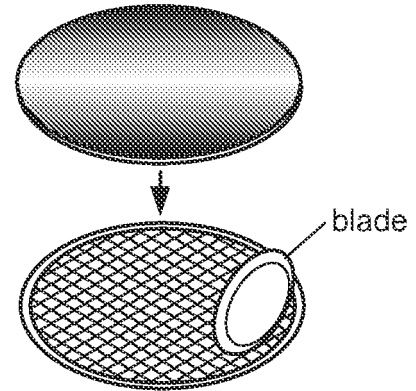


FIG. 3B

Assembly Substrate with III-V Die

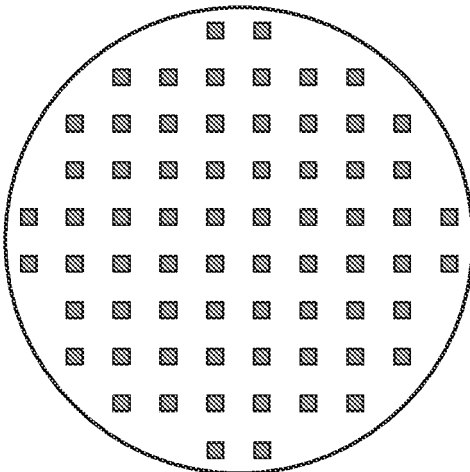


FIG. 3C

FIG. 3D

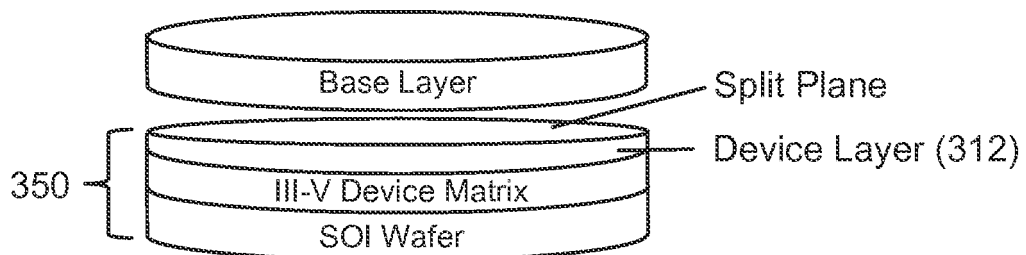
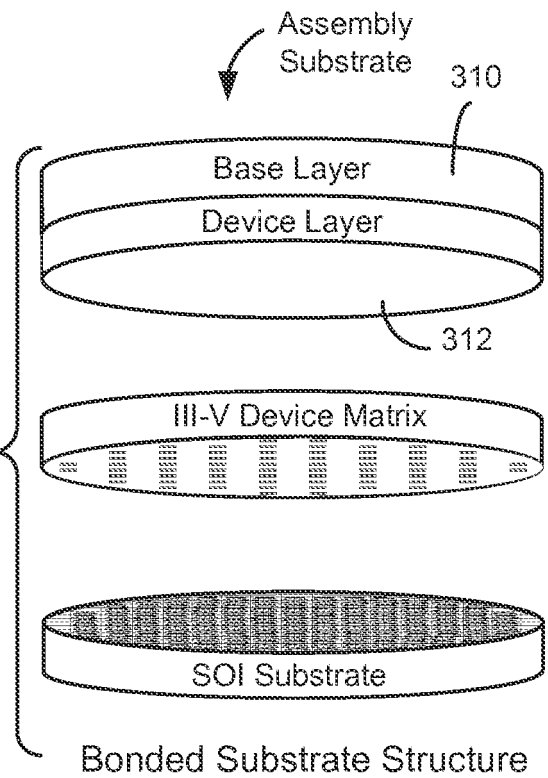


FIG. 3E

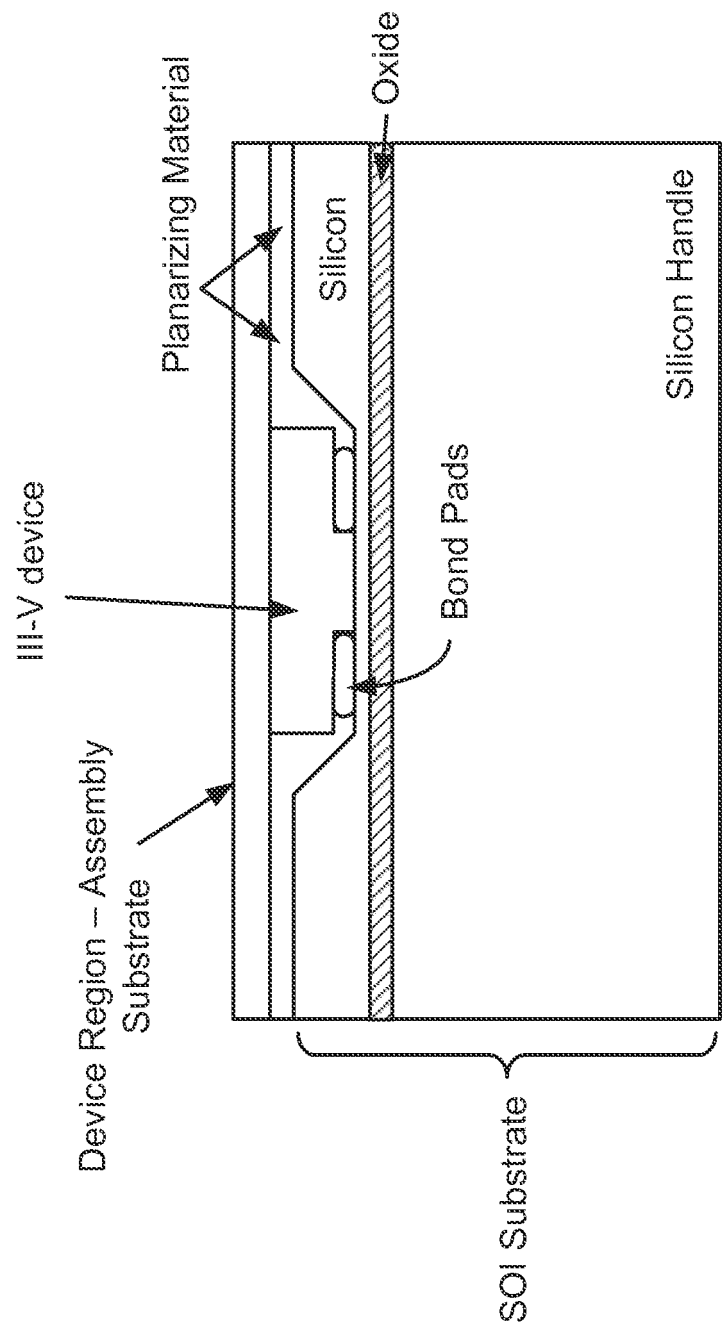


FIG. 4

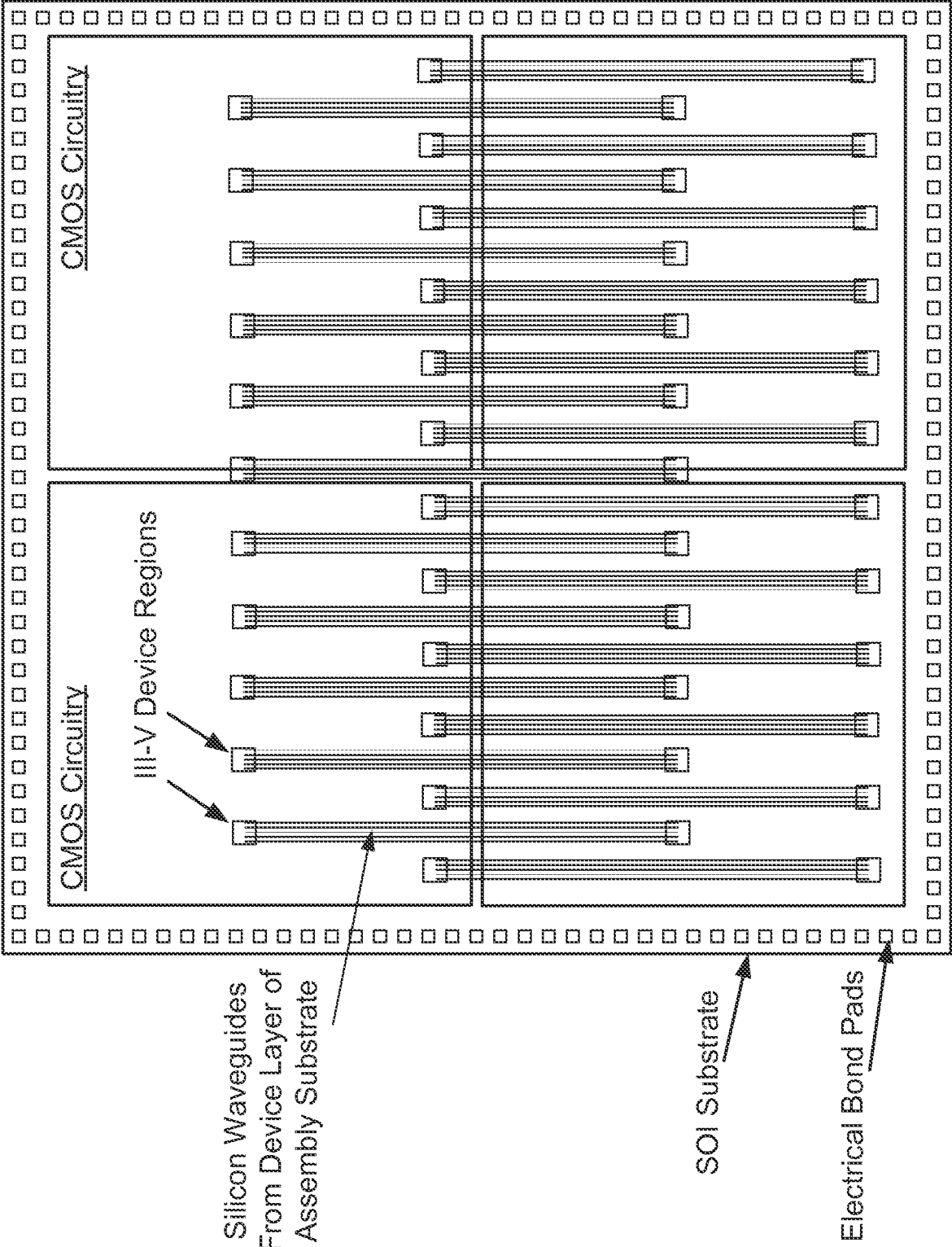
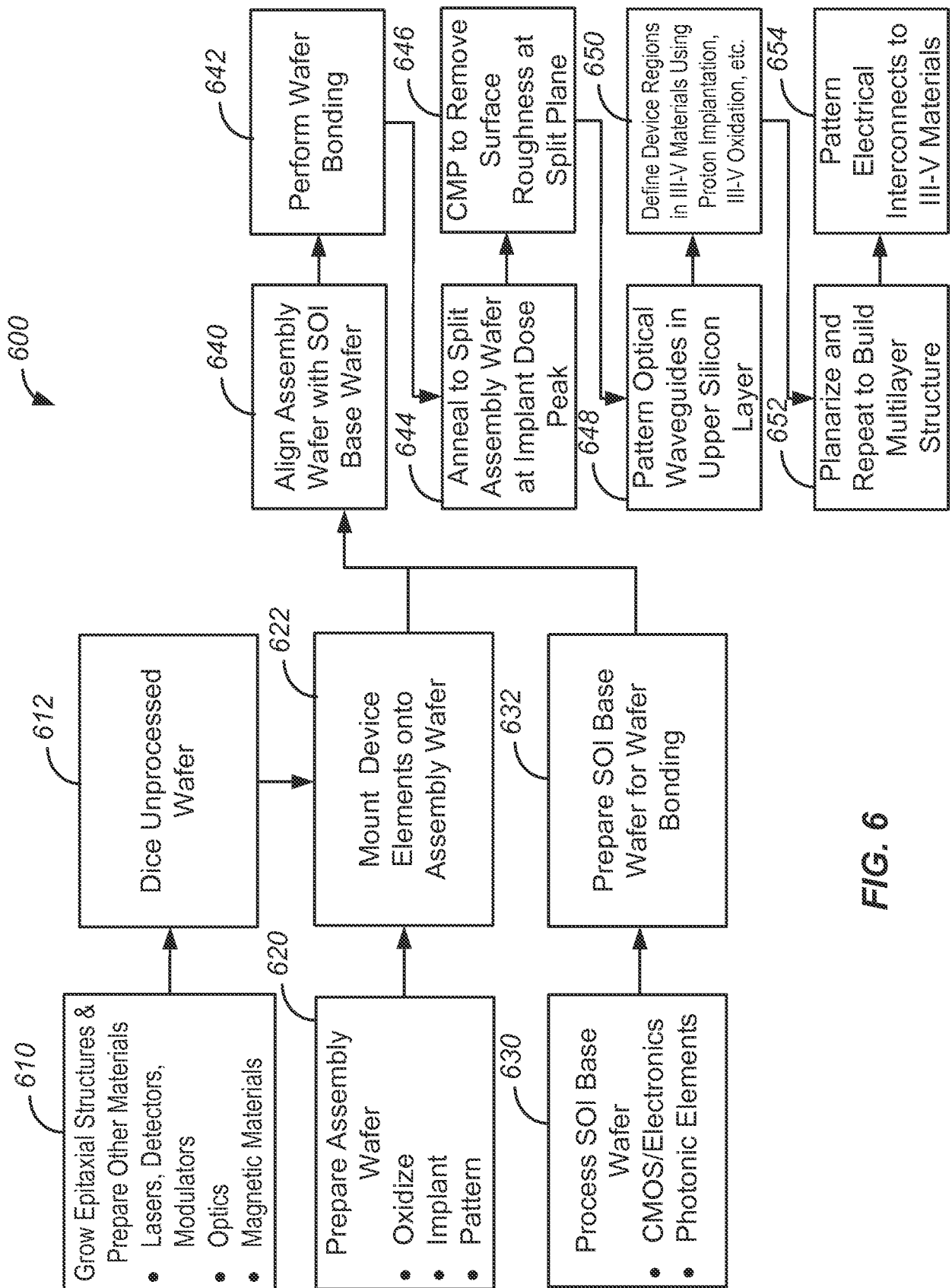
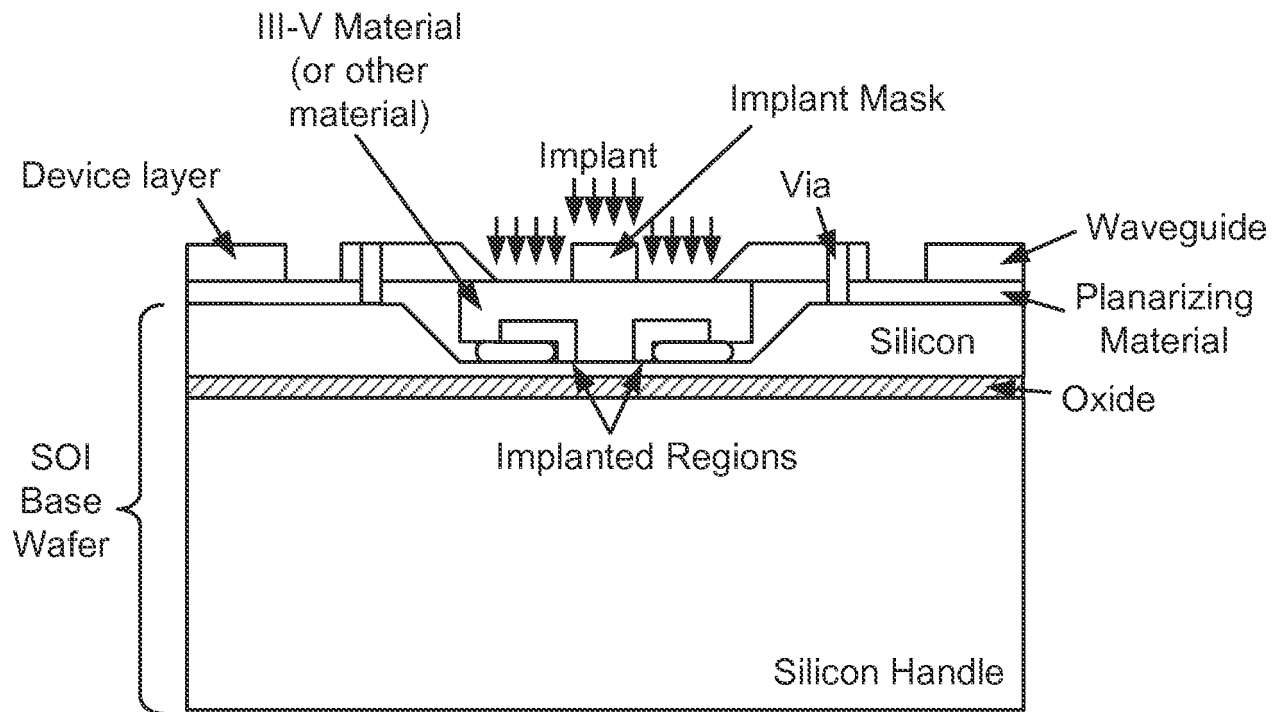
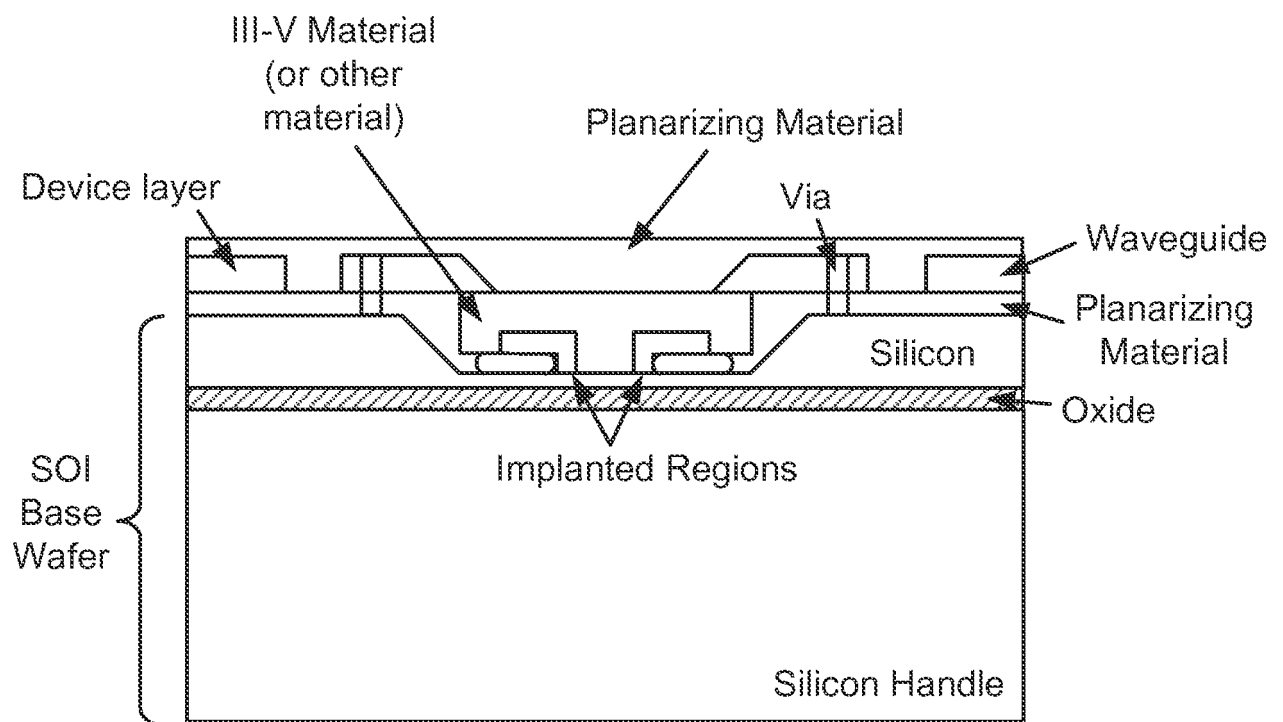


FIG. 5



**FIG. 7A****FIG. 7B**

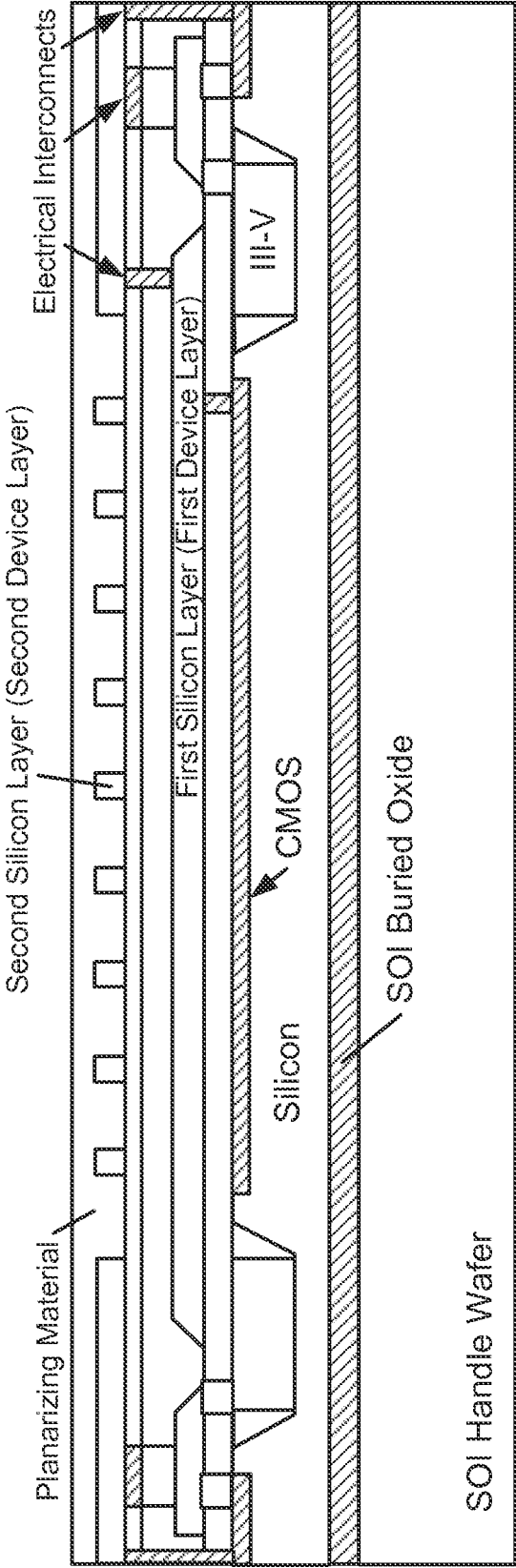


FIG. 7C

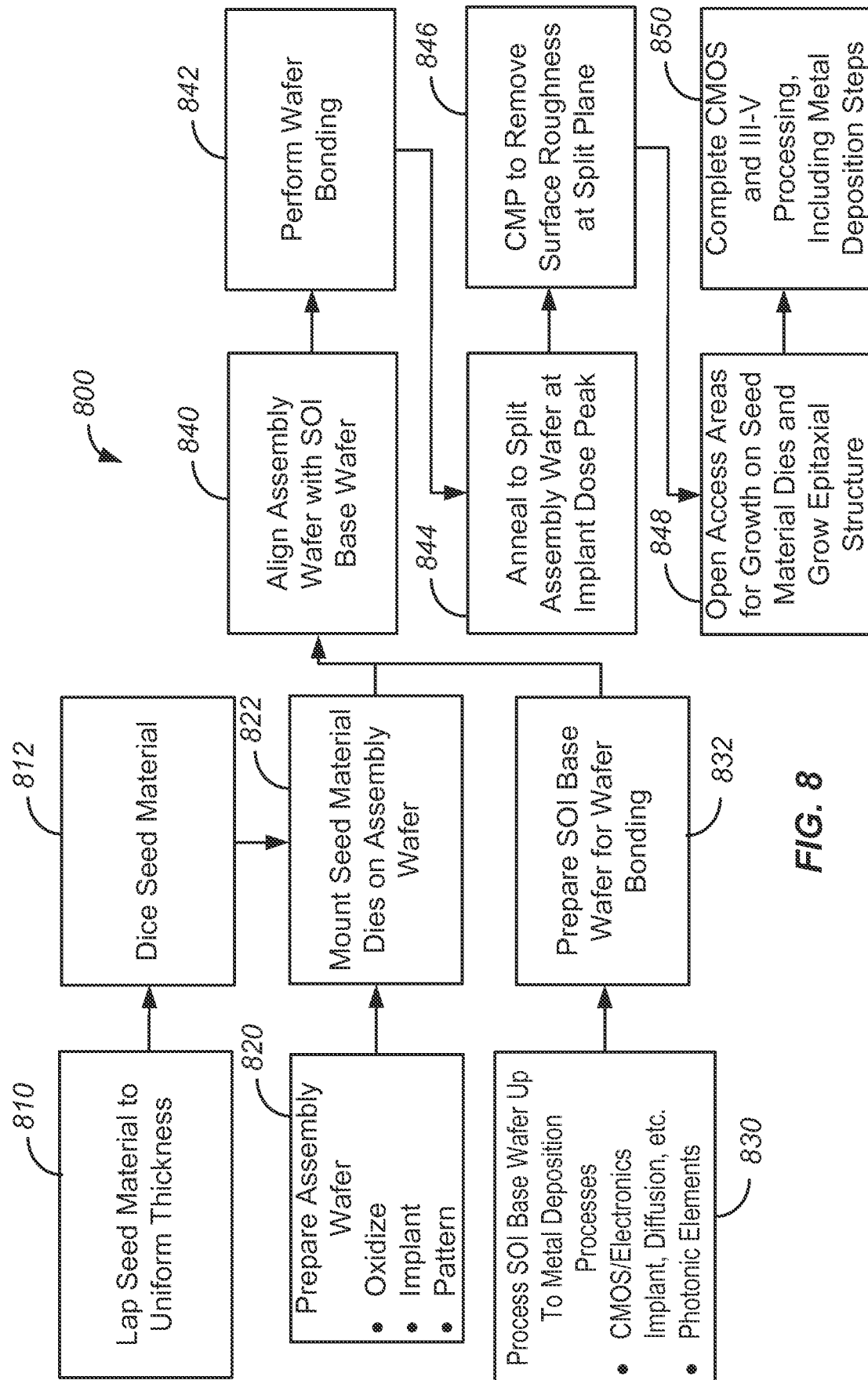


FIG. 9A

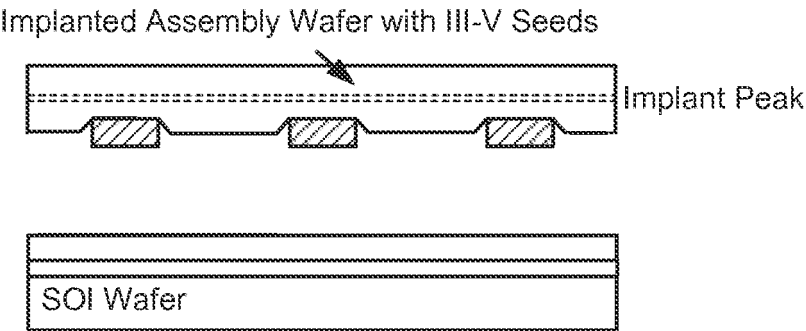


FIG. 9B

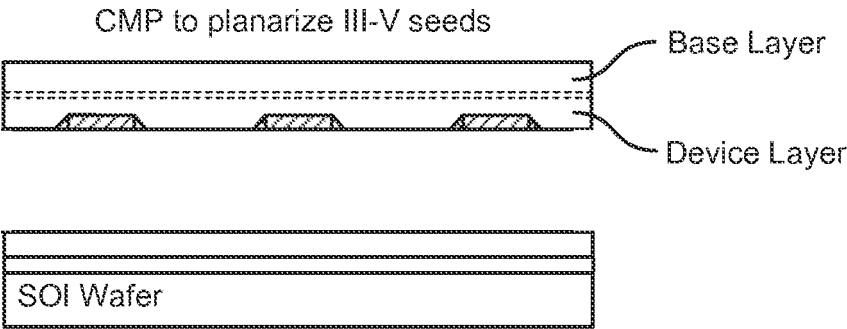


FIG. 9C

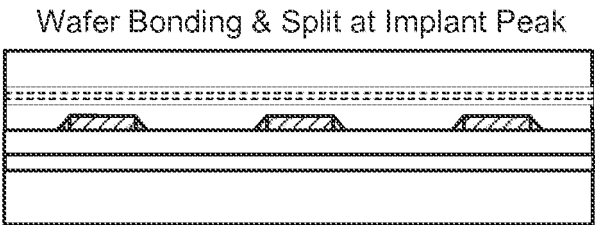


FIG. 9D

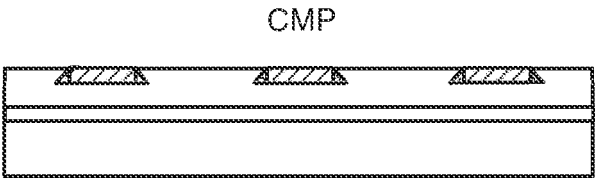
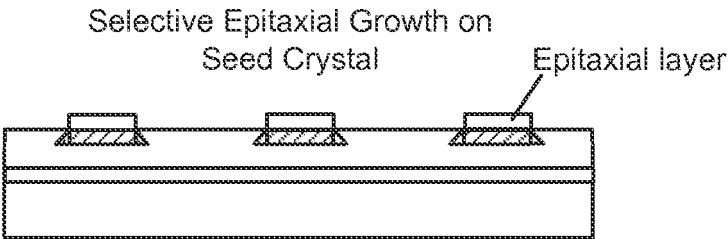


FIG. 9E



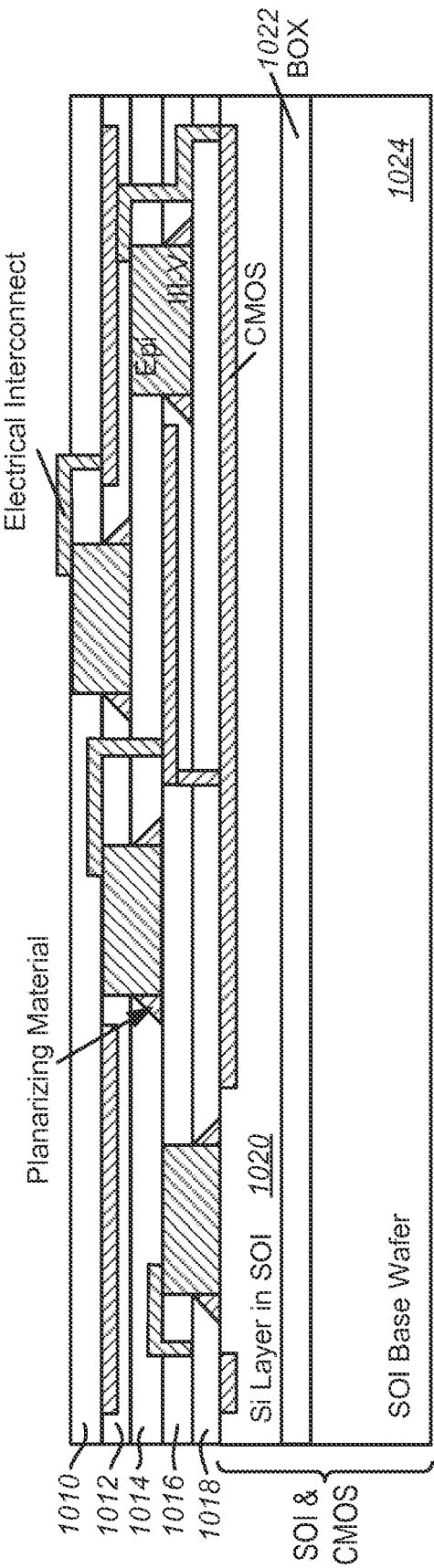
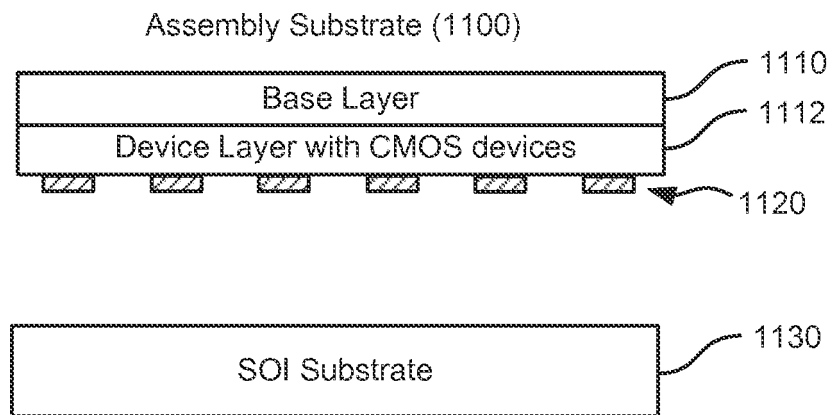
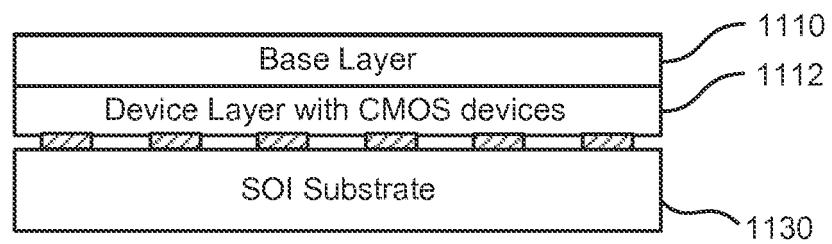
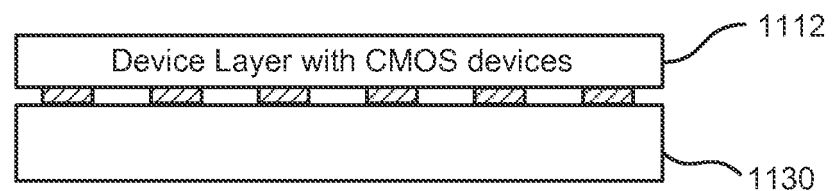


FIG. 10

**FIG. 11A****FIG. 11B****FIG. 11C**

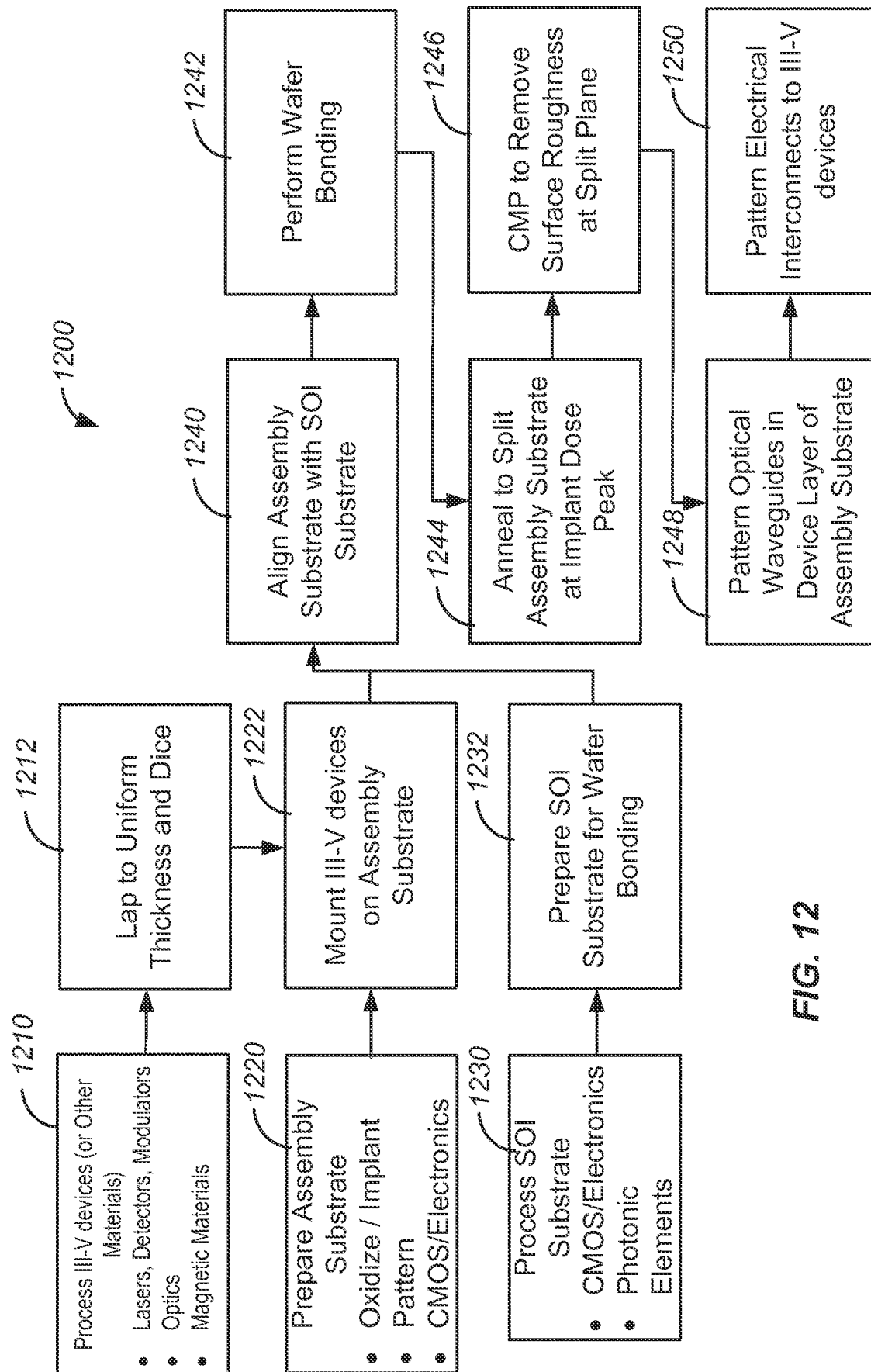
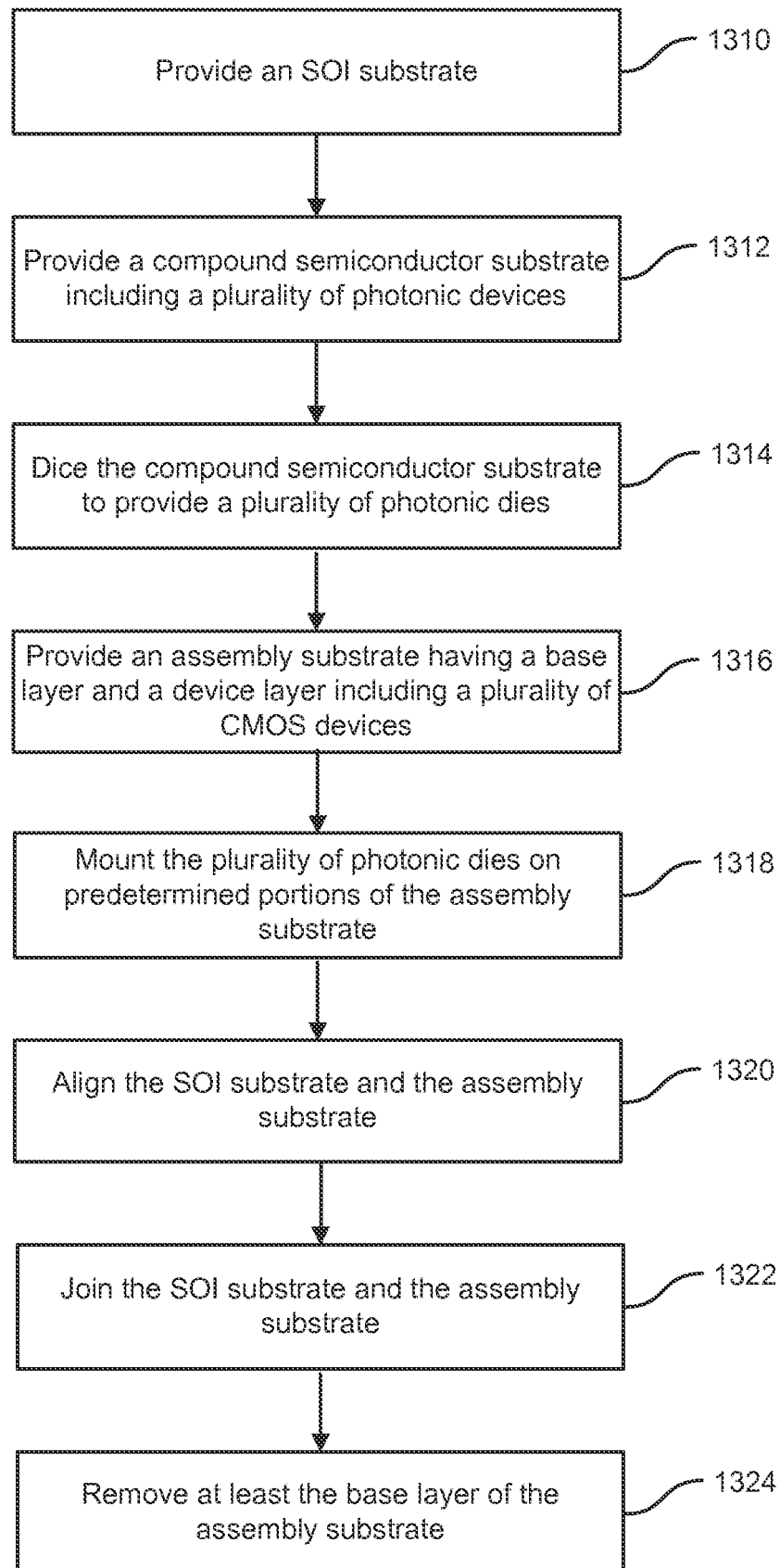
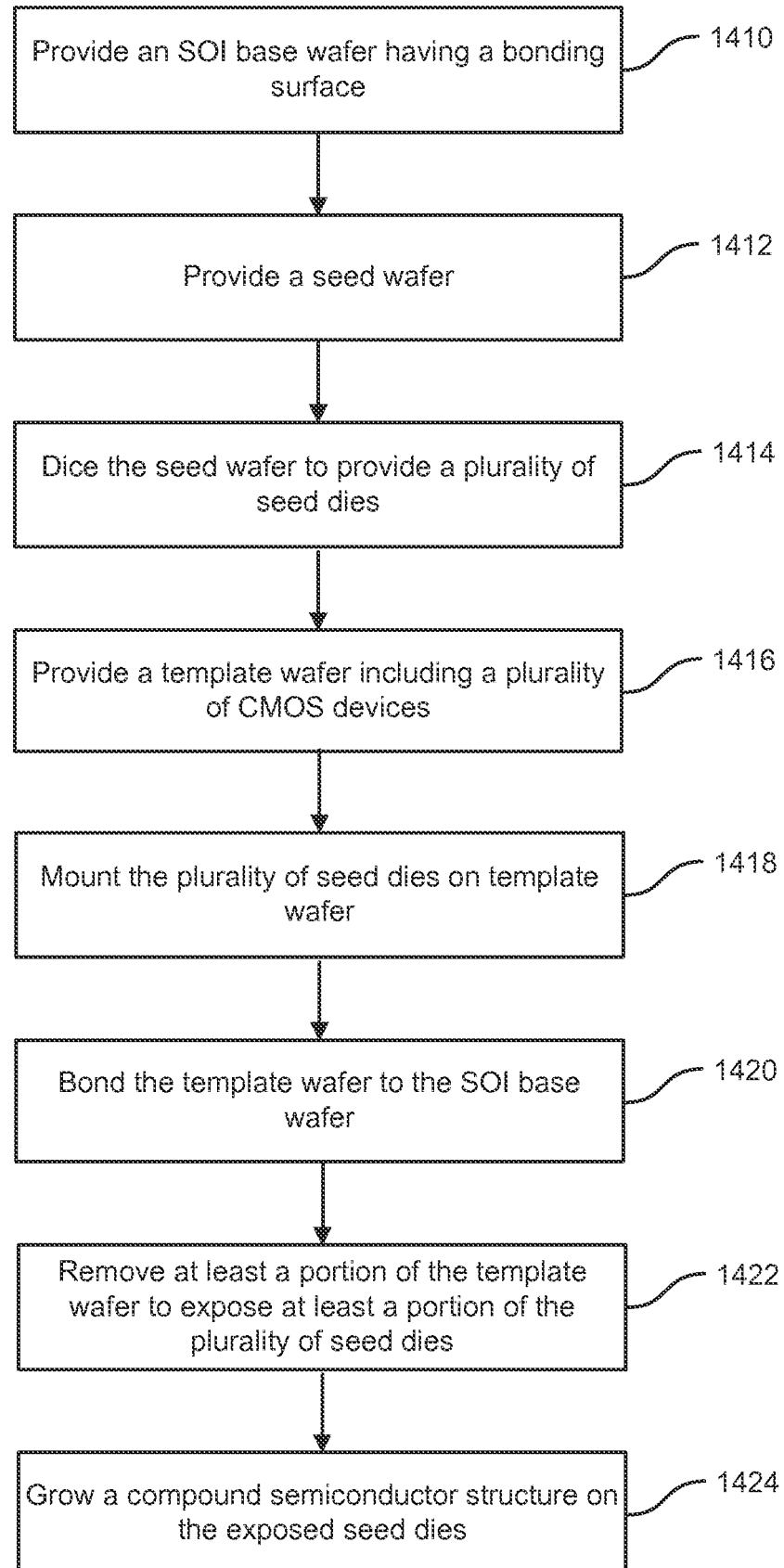


FIG. 12

**FIG. 13**

**FIG. 14**