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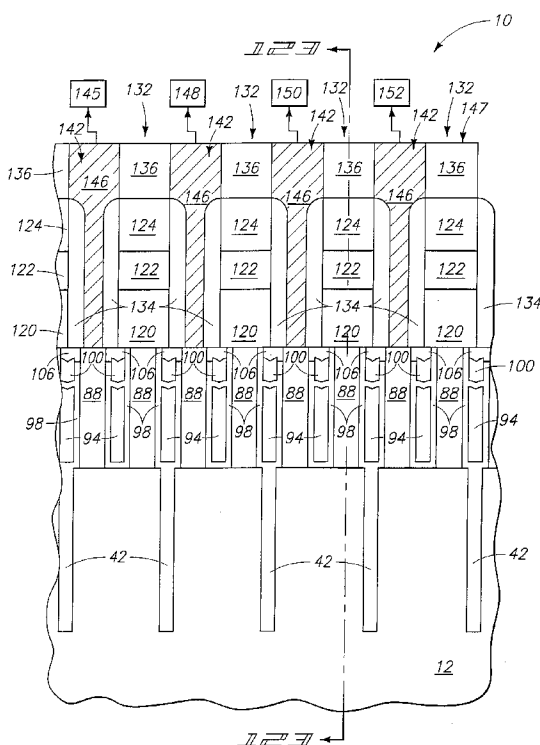
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(54) Title: DRAM STRUCTURES WITH SOURCE/DRAIN PEDESTALS AND MANUFACTURING METHOD THEREOF



(57) Abstract: The invention includes a semiconductor structure (10) having a gate line lattice (94) surrounding vertical source/drain regions (88). In some aspects, the source/drain regions can be provided in pairs, with one of the source/drain regions of each pair extending to a digit line (120, 122) and the other extending to a memory storage device (145), such as a capacitor thereby forming a DRAM. The source/drain regions extending to the digit line can have the same composition as the source/drain regions extending to the memory storage devices, or can have different compositions from the source/drain regions extending to the memory storage devices. The invention also includes methods of forming semiconductor structures. In exemplary methods, a lattice comprising a first material is provided to surround repeating regions of a second material. At least some of the first material is then replaced with a gate line structure, and at least some of the invention includes a semiconductor structure having a gate line lattice surrounding vertical source/drain regions. In some aspects, the source/drain regions can be provided in pairs, with one of the source/drain regions of each pair extending to a digit line and the other extending to a memory storage device, such as a capacitor. The source/drain regions extending to the digit line can have the same composition as the source/drain regions extending to the memory storage devices, or can have different compositions from the source/drain regions extending to the memory storage devices. The invention also includes methods, a lattice comprising a first material is provided to surround repeating regions of a second material. At least some of the first material is then replaced with a gate line structure, and at least some of the second material is replaced with vertical source/drain regions.