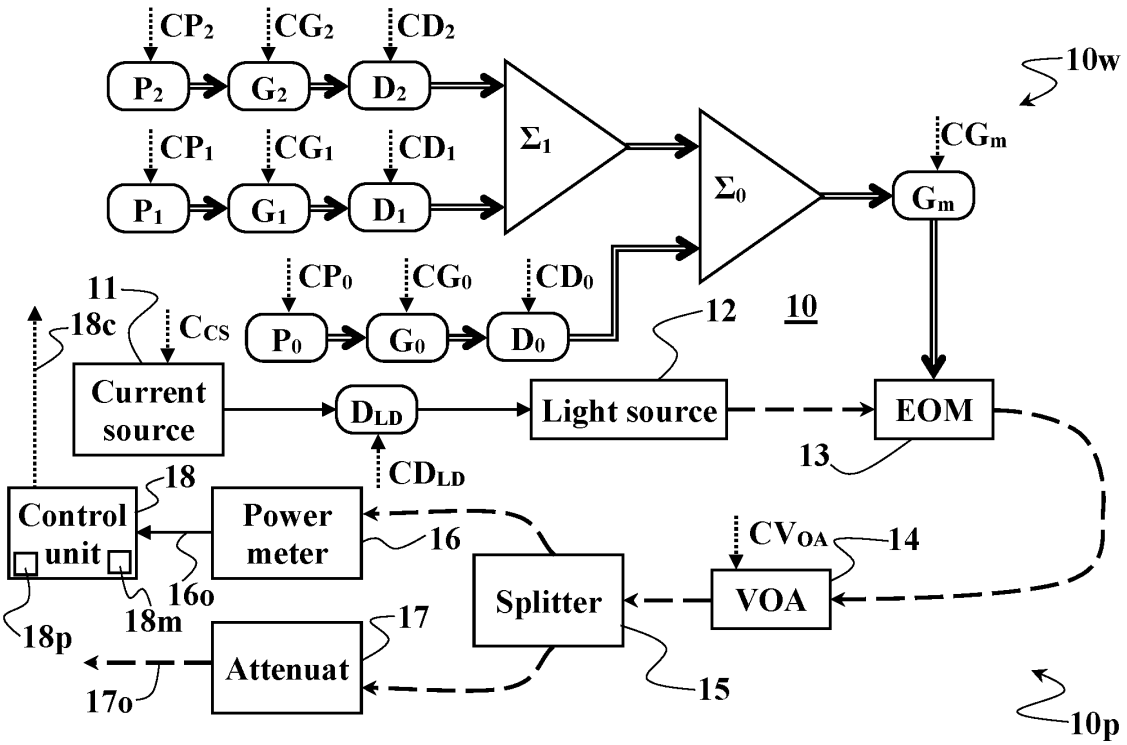

CP2
CG2
CD2
P2
G2
D2
CP1
CG1
CD1
P1
G1
D1
Σ1
Σ0
CGm
Gm
10w
CP0
CG0
CD0
P0
G0
D0
11
18c
CCS
12
10
Current source
DLD
Light source
EOM
13
CDLD
18
Control unit
Power meter
16
CVOA
14
16o
18m
18p
Splitter
VOA
17
Attenuat
17o
15
10p

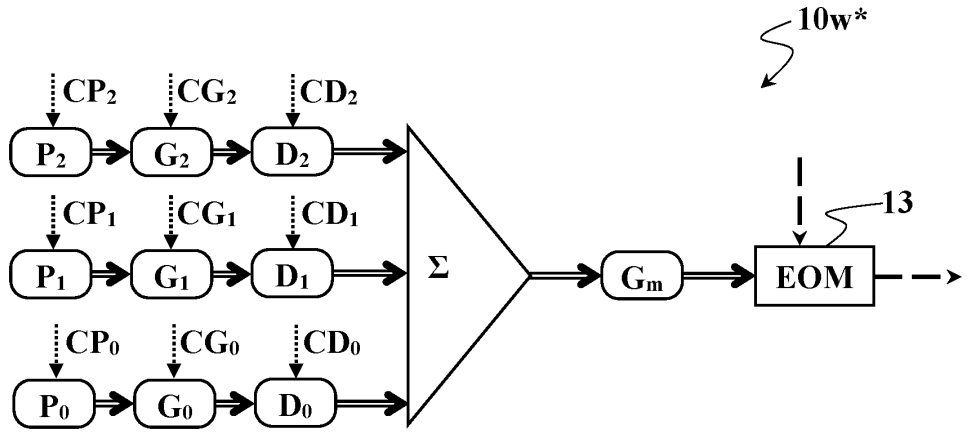
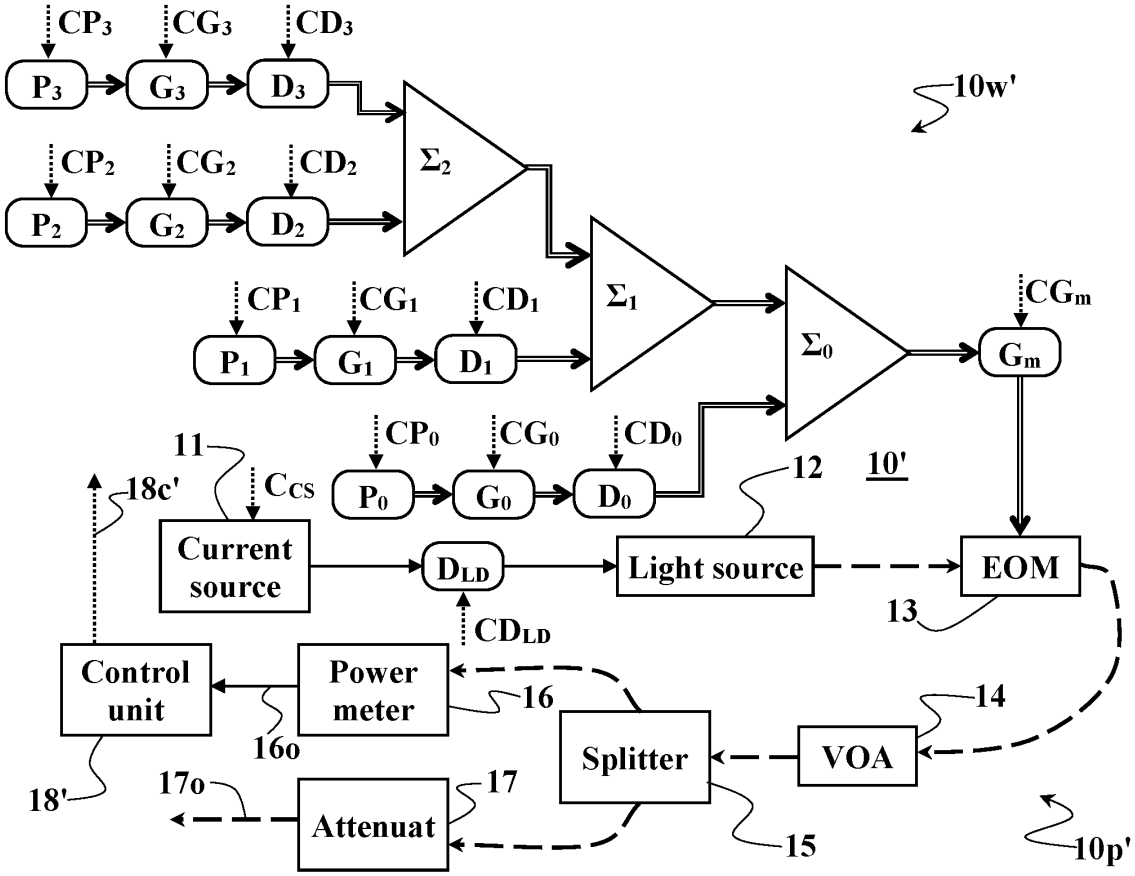

10w*
CP2
CG2
CD2
P2
G2
D2
CP1
CG1
CD1
P1
G1
D1
CP0
CG0
CD0
P0
G0
D0
Σ
Gm
13
EOM

Fig. 1A


CP3
CG3
CD3
P3
G3
D3
10w'
CP2
CG2
CD2
Σ2
P2
G2
D2
CP1
CG1
CD1
Σ1
CGm
P1
G1
D1
Σ0
Gm
CP0
CG0
CD0
11
12
10'
18c'
CCS
P0
G0
D0
Current source
DLD
Light source
EOM
13
CDLD
Control unit
Power meter
16
14
16o
Splitter
VOA
18'
17o
17
Attenuat
15
10p'

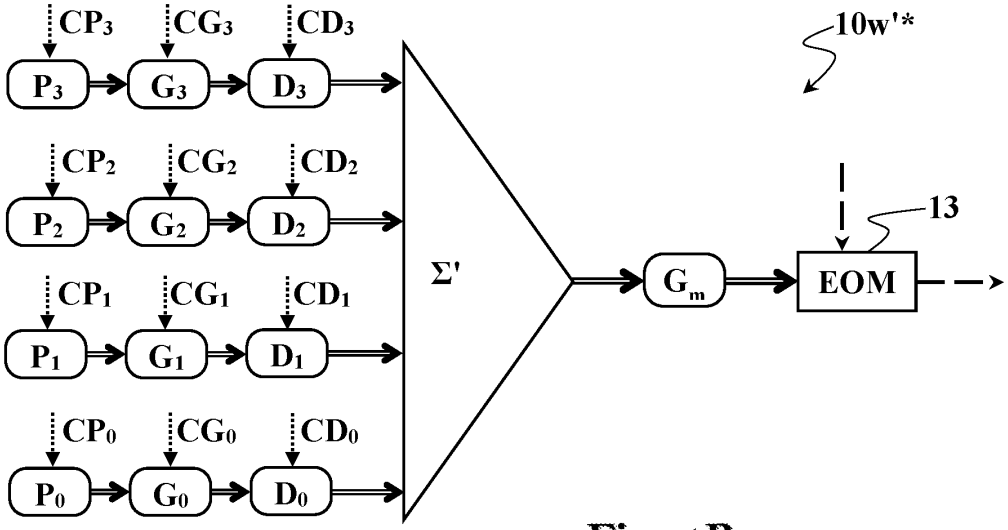

CP3
CG3
CD3
10w'*
P3
G3
D3
CP2
CG2
CD2
13
Σ'
P2
G2
D2
Gm
EOM
CP1
CG1
CD1
P1
G1
D1
CP0
CG0
CD0
P0
G0
D0

Fig. 1B

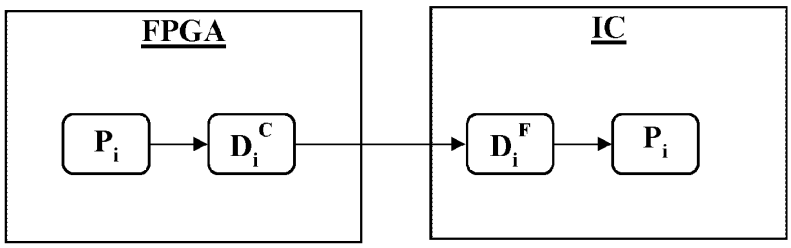

FPGA
IC
P_i
D_i^C
D_i^F
P_i

Fig. 1C

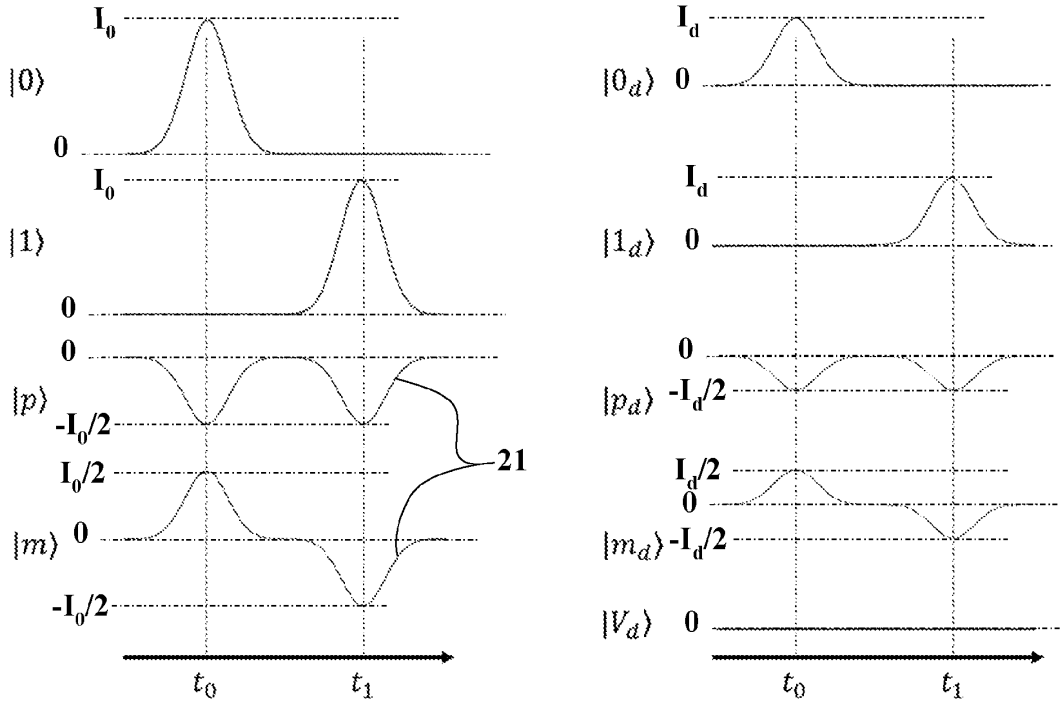

I_0
|0⟩
0
I_0
|1⟩
0
0
|p⟩
-I_0/2
I_0/2
|m⟩
0
-I_0/2
21
t_0
t_1
I_d
|0_d⟩
0
I_d
|1_d⟩
0
0
|p_d⟩
-I_d/2
I_d/2
0
|m_d⟩
-I_d/2
|V_d⟩
0
t_0
t_1

Fig. 2

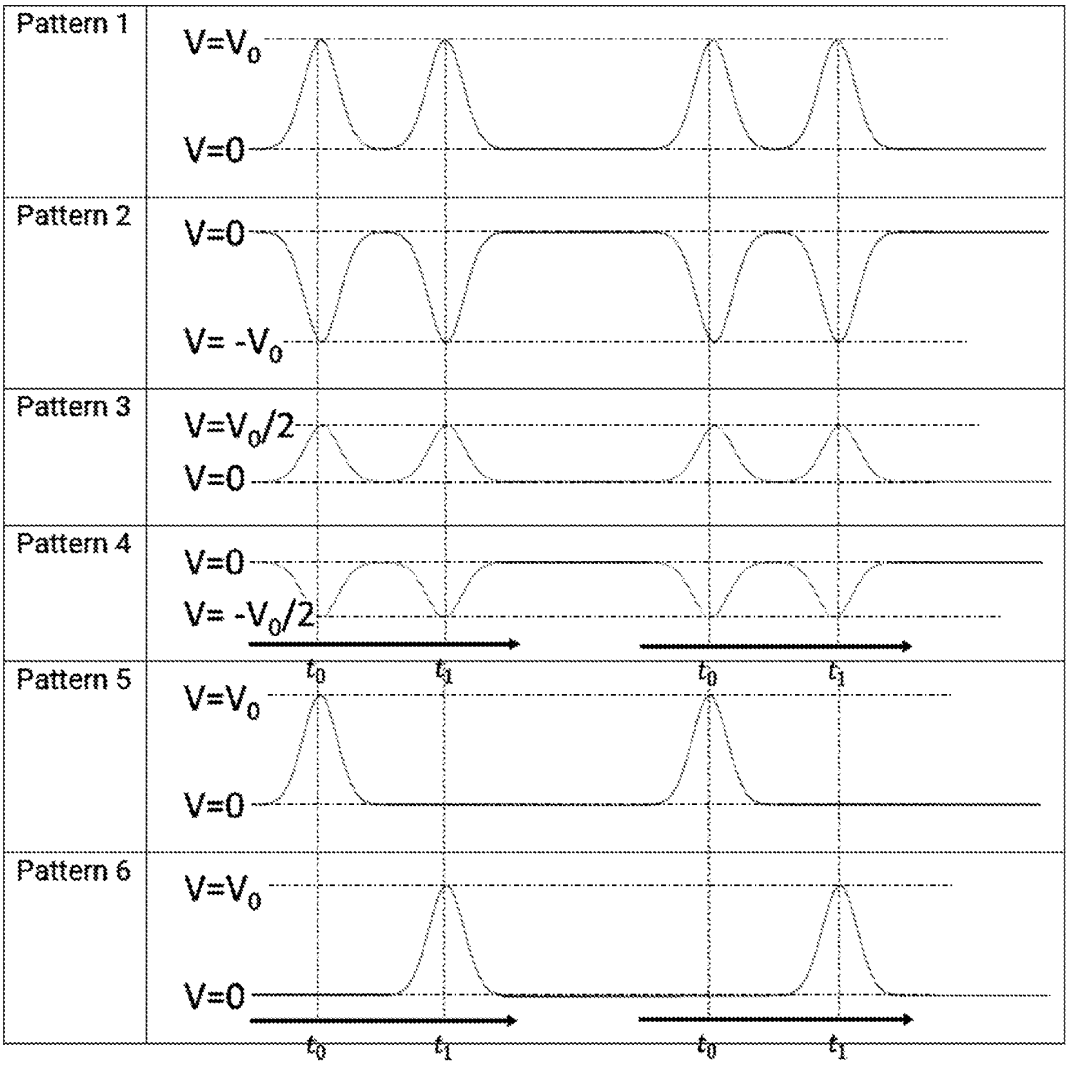

Pattern 1
V=V0
V=0
Pattern 2
V=0
V= -V0
Pattern 3
V=V0/2
V=0
Pattern 4
V=0
V= -V0/2
Pattern 5
V=V0
V=0
Pattern 6
V=V0
V=0
t0
t1
t0
t1
t0
t1
t0
t1

Fig. 3

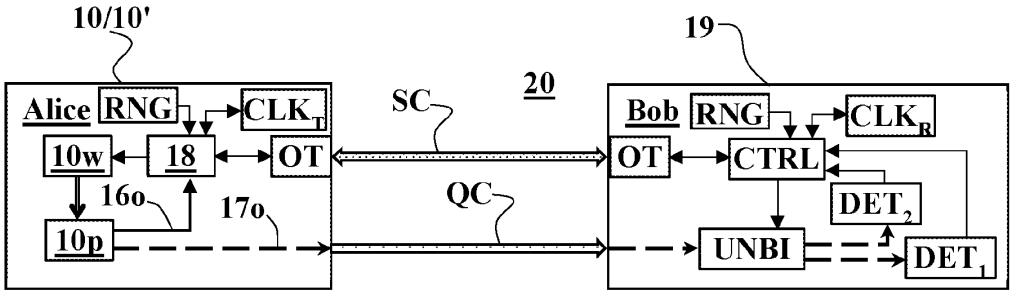

10/10'
19
Alice
RNG
CLK_T
SC
20
Bob
RNG
CLK_R
10w
18
OT
OT
CTRL
16o
17o
QC
DET_2
10p
UNBI
DET_1

Fig. 4

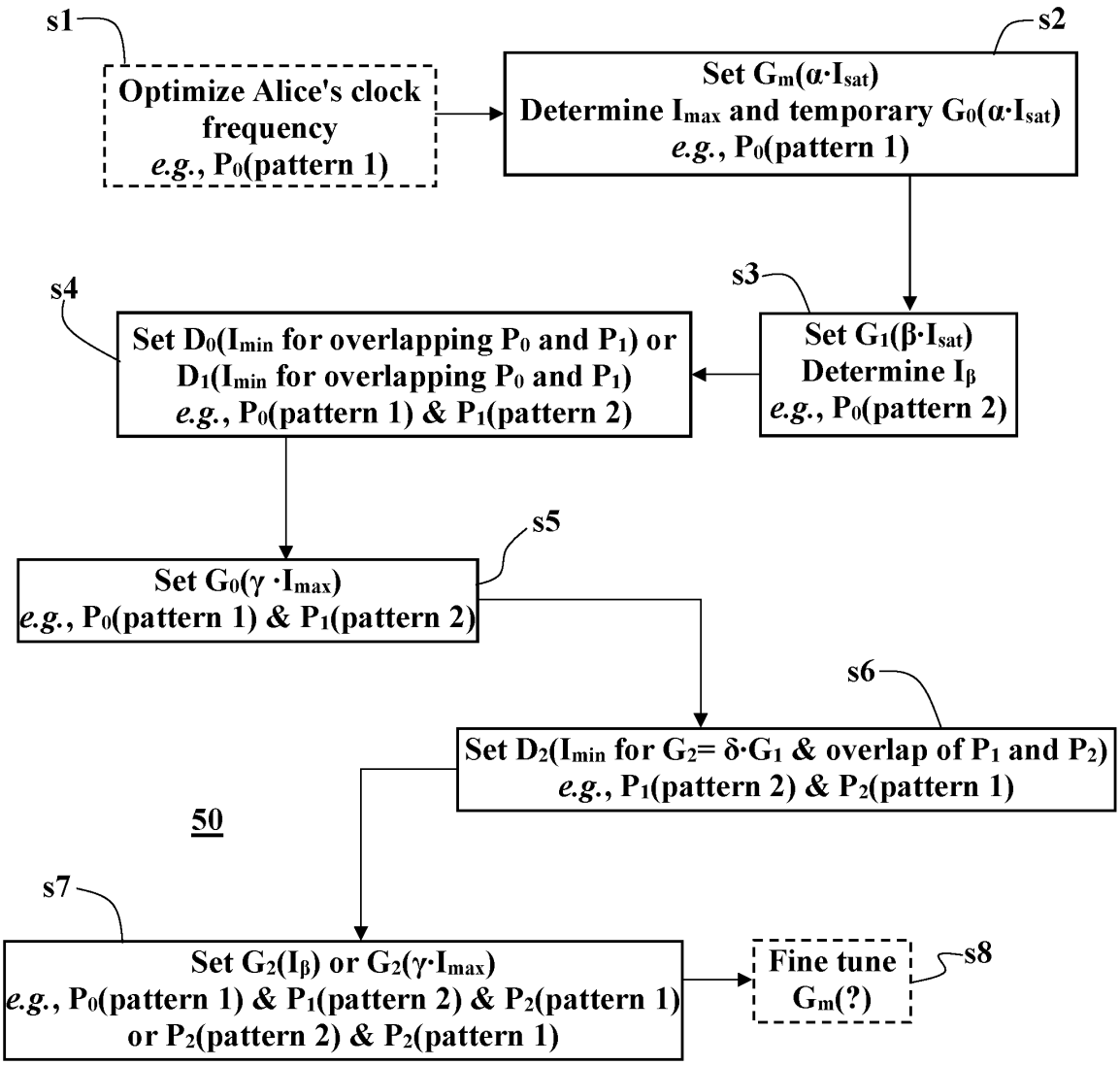

s1
Optimize Alice's clock frequency
e.g., P0(pattern 1)
s2
Set Gm(α·Isat)
Determine Imax and temporary G0(α·Isat)
e.g., P0(pattern 1)
s3
Set G1(β·Isat)
Determine Iβ
e.g., P0(pattern 2)
s4
Set D0(Imin for overlapping P0 and P1) or
D1(Imin for overlapping P0 and P1)
e.g., P0(pattern 1) & P1(pattern 2)
s5
Set G0(γ ·Imax)
e.g., P0(pattern 1) & P1(pattern 2)
s6
Set D2(Imin for G2= δ·G1 & overlap of P1 and P2)
e.g., P1(pattern 2) & P2(pattern 1)
50
s7
Set G2(Iβ) or G2(γ·Imax)
e.g., P0(pattern 1) & P1(pattern 2) & P2(pattern 1)
or P2(pattern 2) & P2(pattern 1)
Fine tune
Gm(?)
s8

Fig. 5A

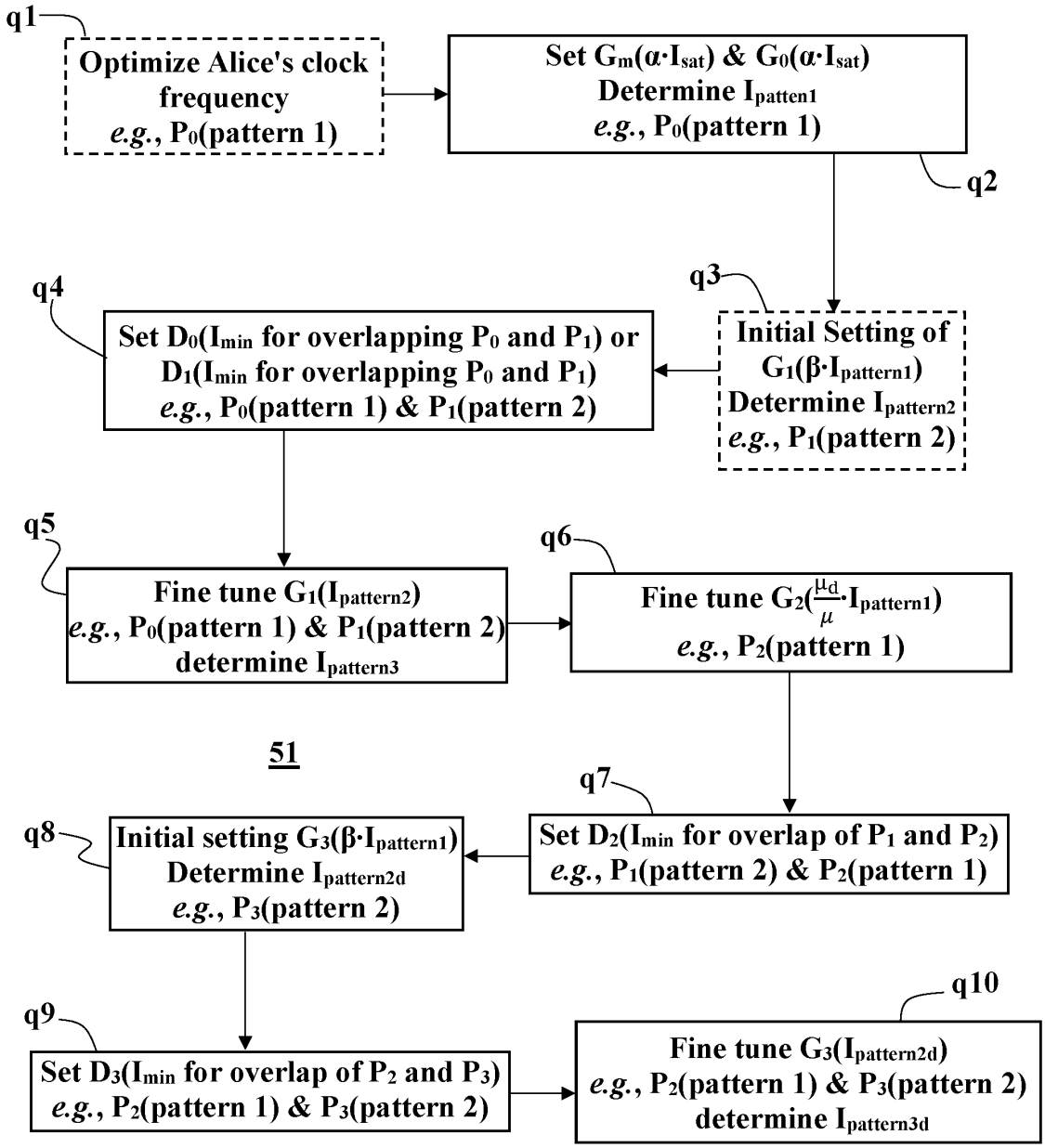

q1
Optimize Alice's clock frequency
e.g., P0(pattern 1)
Set Gm(α·Isat) & G0(α·Isat)
Determine Ipatten1
e.g., P0(pattern 1)
q2
q3
Initial Setting of G1(β·Ipattern1)
Determine Ipattern2
e.g., P1(pattern 2)
q4
Set D0(Imin for overlapping P0 and P1) or D1(Imin for overlapping P0 and P1)
e.g., P0(pattern 1) & P1(pattern 2)
q5
Fine tune G1(Ipattern2)
e.g., P0(pattern 1) & P1(pattern 2)
determine Ipattern3
q6
Fine tune G2(μd/μ·Ipattern1)
e.g., P2(pattern 1)
51
q7
Set D2(Imin for overlap of P1 and P2)
e.g., P1(pattern 2) & P2(pattern 1)
q8
Initial setting G3(β·Ipattern1)
Determine Ipattern2d
e.g., P3(pattern 2)
q9
Set D3(Imin for overlap of P2 and P3)
e.g., P2(pattern 1) & P3(pattern 2)
q10
Fine tune G3(Ipattern2d)
e.g., P2(pattern 1) & P3(pattern 2)
determine Ipattern3d

Fig. 5B