METHODS FOR DEPOSITION OF SEMICONDUCTOR MATERIAL

TECHNICAL FIELD

[0001] The invention pertains to methods for deposition of semiconductor material.

BACKGROUND OF THE INVENTION

[0002] There are numerous applications in which it is desired to selectively deposit semiconductor material onto a semiconductor surface relative to other surfaces. For instance, it can be desired to epitaxially form one or both of silicon and germanium on a semiconductor surface. A prior art method of epitaxially forming semiconductor material over a semiconductor surface is described with reference to Figs. 1-3.

[0003] Fig. 1 shows a semiconductor wafer fragment 10 at a preliminary processing stage. Fragment 10 comprises a semiconductor substrate 12. Substrate 12 can comprise, consist essentially of, or consist of monocrystalline silicon. The silicon can be appropriately doped with one or more conductivity-enhancing dopants. For instance, the silicon can be lightly background doped with p-type dopant, and can comprise various conductively-doped diffusion regions (not shown) formed therein. To aid in interpretation of the claims that follow, the terms "semiconductive substrate" and "semiconductor substrate" are defined to mean any construction comprising semiconductive material, including, but not limited to, bulk semiconductive materials such as a semiconductive wafer (either alone or in assemblies comprising other materials thereon), and semiconductive material layers (either alone or in assemblies comprising other materials). The term "substrate" refers to any supporting structure, including, but not limited to, the semiconductive substrates described above. The term "semiconductor material" refers to a material comprising one or more of the semiconductive elements, such as, for example, a material comprising one or both of silicon and germanium.

[0004] An electrically insulative material 14 is formed over substrate 12. Material 14 can comprise, consist essentially of, or consist of silicon and one or both of oxygen and nitrogen. For instance, material 14 can comprise silicon dioxide, silicon nitride, and/or silicon oxynitride. In the illustrated example, substrate 12 has an upper surface 13, and material 14 is formed directly against (i.e., in physical contact with) the

upper surface 13. Material 14 is patterned to have a gap 16 extending therethrough to the upper surface 13 of substrate 12. Material 14 has exposed surfaces 15.

[0005] Referring to Fig. 2, a semiconductor material 18 is formed within gap 16 and also over the surfaces 15 of insulative material 14. Material 16 will typically comprise, consist essentially of, or consist of one or both of silicon and germanium. If material 16 comprises, consists essentially of, or consists of silicon, such material can be formed utilizing dichlorosilane, H_2 and HCl. The dichlorosilane provides a silicon source. The H_2 participates in the silicon deposition, and also can remove undesired oxides forming over the growing silicon. The HCl etches material 18 before the material can form a uniform layer over insulative material 14. Specifically, the material 18 nucleates over insulative material 14 to form small islands on surface 15, as shown. The HCl continuously etches material 18 from the small islands, and accordingly removes material 18 from the islands before the islands can merge to form a continuous layer. The HCl is also thought to remove material 18 which is growing over surface 13 (the shown material 18 within gap 16), but such removal is too slow to prevent the layer of material 18 from forming within gap 16. Accordingly, the HCl effectively creates a selective deposition of material 18 over the surface 13 of semiconductor material 12 relative to the surfaces 15 of insulative material 14. The HCl can be replaced with Cl_2 in some aspects of the prior art.

[0006] Fig. 3 shows construction 10 at the conclusion of the epitaxial growth, and shows that the semiconductor material 18 has been selectively formed over surface 13 of semiconductor substrate 12 relative to surfaces 15 of insulative material 14.

[0007] A problem with the processing of Figs. 1-3 is that the utilization of HCl significantly slows the rate of deposition of semiconductor material 18 relative to a rate which would occur in the absence of the HCl. Accordingly, it is desired to develop deposition processes which can selectively form a semiconductor material over an exposed semiconductor substrate surface relative to exposed surfaces of non-semiconductor materials, and which have a higher rate than the processing sequence of Figs. 1-3.

[0008] The processing sequence of Figs. 1-3 is an exemplary prior art process. Other processes have been developed which are modifications of the process described with reference to Figs. 1-3. For instance, in one modification a semiconductor precursor (such as, for example, dichlorosilane) is provided in combination with H_2 to form semiconductor material 18 over a surface of a semiconductor substrate and over

surfaces of insulative materials. After the growth of the semiconductor material, HCl is provided to selectively remove the semiconductor material from over the insulative materials surfaces while leaving a layer of the semiconductor material over the semiconductor substrate surface. In some aspects, the cycling of deposition of semiconductor material, etching of semiconductor material from over insulative material surfaces, deposition of the material, etching of the material, etc., is repeated multiple times to form a semiconductor material to a desired thickness over a semiconductor substrate surface. A particular prior art methodology flows disilane for about 10 seconds, then Cl_2 for about 10 seconds, then H_2 for about 10 seconds, and repeats the process multiple times to form a semiconductor layer to a desired thickness over a semiconductor substrate surface.

[0009] Figs. 4 and 5 illustrate another exemplary prior art application for selective formation of epitaxially-grown semiconductor material over a semiconductor substrate. Referring initially to Fig. 4, a wafer fragment 20 comprises a substrate 22. Substrate 22 can comprise the same construction as described previously relative to substrate 12 of Fig. 1, and accordingly can comprise monocrystalline silicon lightly-background doped with p-type dopant. Substrate 22 comprises an upper surface 23.

[0010] An isolation region 24 extends within substrate 22. Isolation region 24 can comprise, for example, a shallow trench isolation region, and accordingly can comprise silicon dioxide. Isolation region 24 comprises an upper surface 25.

[0011] A transistor gate 26 is formed over surface 23 of substrate 22. Transistor gate 26 comprises an insulative material 28, a conductive material 30, and an insulative cap 32. Insulative material 28 can comprise, for example, silicon dioxide, and can be referred to as pad oxide. Conductive material 30 can comprise, for example, one or more of metal, metal compounds and conductively-doped semiconductor material (such as, for example, conductively-doped silicon). Insulative cap 32 can comprise, consist essentially of, or consist of silicon together with one or both of oxygen and nitrogen. For instance, insulative cap 32 can comprise, consist essentially of, or consist of silicon dioxide, silicon nitride, or silicon oxynitride. Insulative cap 32 comprises an upper exposed surface 33.

[0012] An anisotropically-etched sidewall spacer 34 is along a sidewall of transistor gate 26. Spacer 34 can comprise, consist essentially of, or consist of silicon together with one or both of oxygen and nitrogen. Accordingly, spacer 34 can comprise,

or consist essentially of, or consist of one or more of silicon dioxide, silicon nitride and silicon oxynitride. Spacer 34 has an exposed surface 35.

[0013] A conductively-doped diffusion region 36 extends within substrate 22 beside transistor gate 26. The conductively-doped diffusion region 36 and transistor gate 26 can be together incorporated into a transistor device.

[0014] Referring to Fig. 5, a semiconductor material 38 is formed over surface 23 of semiconductor substrate 22 selectively relative to surfaces 25 and 33 of insulative materials 24 and 32, respectively. Semiconductor material 38 can comprise, consist essentially of, or consist of one or both of silicon and germanium, and can be formed utilizing processing analogous to that described previously with reference to Figs. 1-3. Accordingly, the semiconductor material can be formed by deposition from a semiconductor precursor in combination with an etch which removes the deposited material from over surfaces 25 and 33 while leaving the material over surface 23. An undesired consequence of the etch is that such rounds an outer corner of deposited material 38, as can be seen at a location 40 in the diagram of Fig. 5. The rounded outer corner can be referred to as a faceted corner, and can increase degradation of a transistor device component (with a common effect being p-channel degradation), and can also adversely affect an implant profile if a dopant is implanted either into or through semiconductor material 38. For instance, conductively-doped diffusion region 36 would sometimes be formed by an implant subsequent to formation of material 38 rather than being present prior to deposition of semiconductor material 38. The rounded faceted corner 40 could then adversely affect formation of the diffusion region 36.

[0015] The semiconductor material 38 of Fig. 5 can ultimately be conductively doped, and can be incorporated into, for example, an elevated source/drain region associated with a transistor device comprising gate 26.

[0016] Numerous problems are encountered during the processing described above with reference to Figs. 1-5. Such problems include the faceted corner 40 and slow growth rate discussed previously. Another problem is that the deposition rate and quality can be sensitive to the amount of etchant (such as, for example, HCl) utilized during the deposition/etch processing, which can make it problematic to control wafer throughput and quality in a fabrication process. For instance, it is sometimes found that increasing HCl flow by 10% will decrease the growth rate of a deposited semiconductor material by about 20%. It would be desirable to develop deposition methods which alleviate, and preferably eliminate, some or all of the above-discussed problems.

SUMMARY OF THE INVENTION

[0017] In one aspect, the invention encompasses a method for deposition of semiconductor material. A substrate is provided within a reaction chamber. The substrate includes a first material and a second material, with the second material having a different composition than the first material. The first and second materials are exposed to a semiconductor material precursor under conditions in which growth of semiconductor material from the precursor comprises a lag phase prior to a growth phase. The conditions are also such that it takes longer for the growth phase to initiate on the second material than on the first material. A concentration of the precursor is pulsed into the chamber. The duration of the pulse is long enough for the growth phase to substantially occur on the first material, but not long enough for the growth phase to substantially occur on the second material.

[0018] In one aspect, the invention encompasses a method for deposition of a semiconductor material comprising one or both of silicon and germanium. A substrate is provided within a reaction chamber. The substrate has a first surface consisting essentially of one or more semiconductor materials and a second surface consisting of one or more electrically insulative materials. The first and second surfaces are exposed to at least one precursor selected from the group consisting of silicon-containing precursors and germanium-containing precursors to deposit a substance comprising one or both of silicon and germanium over the substrate. The exposure is under conditions in which deposition of the substance over the first and second surfaces comprises nucleation phase/growth phase dynamics, and under which it takes longer for the growth phase to initiate over the second surface than over the first surface. The exposure is conducted for a time long enough to substantially initiate the growth phase over the first surface but not long enough to substantially initiate the growth phase over the second surface. Thus, the substance is selectively formed over the first surface relative to the second surface.

BRIEF DESCRIPTION OF THE DRAWINGS

[0019] Preferred embodiments of the invention are described below with reference to the following accompanying drawings.

[0020] Fig. 1 is a diagrammatic, cross-sectional view of a semiconductor wafer fragment shown at a preliminary stage of a prior art process.

[0021] Fig. 2 is a view of the Fig. 1 wafer fragment shown at a prior art processing stage subsequent to that of Fig. 1.

[0022] Fig. 3 is a view of the Fig. 1 wafer fragment shown at a prior art processing stage subsequent to that of Fig. 2.

[0023] Fig. 4 is a diagrammatic, cross-sectional view of a semiconductor wafer fragment shown at a preliminary processing stage of a second prior art process.

[0024] Fig. 5 is a view of the Fig. 4 wafer fragment shown at a prior art processing stage subsequent to that of Fig. 4.

[0025] Fig. 6 is a graphical illustration of time versus thickness illustrating the growth dynamics for semiconductor material over two different surfaces under particular conditions.

[0026] Fig. 7 is a graphical illustration of gas flow versus time illustrating an exemplary processing sequence of an aspect of the present invention.

[0027] Fig. 8 is a diagrammatic, cross-sectional view of a reaction chamber configured for utilization in an exemplary aspect of the present invention.

[0028] Fig. 9 is a diagrammatic, cross-sectional view of a wafer fragment at a preliminary processing stage of an exemplary aspect of the present invention.

[0029] Fig. 10 is a view of the Fig. 9 wafer fragment shown at a processing stage subsequent to that of Fig. 9.

[0030] Fig. 11 is a view of the Fig. 9 wafer fragment shown at a processing stage subsequent to that of Fig. 10.

[0031] Fig. 12 is a view of the Fig. 9 wafer fragment shown at a processing stage subsequent to that of Fig. 11.

[0032] Fig. 13 is a diagrammatic, cross-sectional view of a semiconductor wafer fragment at a preliminary processing stage of a second embodiment aspect of the present invention.

[0033] Fig. 14 is a view of the Fig. 13 wafer fragment shown at a processing stage subsequent to that of Fig. 13.

[0034] Fig. 15 is a view of the Fig. 13 wafer fragment shown at a processing stage subsequent to that of Fig. 14.

[0035] Fig. 16 is a view of the Fig. 13 wafer fragment shown at a processing stage subsequent to that of Fig. 15.

[0036] Fig. 17 is a view of the Fig. 13 wafer fragment shown at the processing stage of Fig. 16 in accordance with an exemplary aspect of the invention.

DETAILED DESCRIPTION OF THE PREFERRED EMBODIMENTS

[0037] One aspect of the invention is a recognition that the dynamics of growth of deposited semiconductor materials on different surfaces can differ, and that this can be taken advantage of for selective deposition on particular surfaces.

[0038] Fig. 6 is a graphical illustration of the dynamics of growth of a deposited semiconductor material on two different surfaces. One of the surfaces is a semiconductor material (the line labeled 50), and the other is an insulative material (the line labeled 60). The insulative material can consist of silicon together with one or both of oxygen and nitrogen (i.e., can consist of silicon dioxide, silicon nitride or silicon oxynitride).

[0039] The rate of growth of the deposited semiconductor material over the surfaces is illustrated in the Fig. 6 graph as a change in thickness of the deposited material over time. Notably, the growth dynamics on both the semiconductor surface (line 50) and the insulative material surface (line 60) are similar in that both have a delay phase (lag phase) prior to a growth phase. Specifically, the thickness of the deposited material does not increase from the zero timepoint, but rather begins to increase after a lag phase. The lag phase for growth on the semiconductor material corresponds to time T_1, and the lag phase for the growth on the insulative material corresponds to time T_2.

[0040] The lag phase for growth of the deposited material on the semiconductor material is significantly shorter than the lag phase for the growth on the insulative material. In exemplary applications, the lag phase T_1 may be about 2 seconds, while the lag phase T_2 may be about 10 seconds. The particular length of a lag phase can be impacted by the deposition conditions utilized. For instance, if the deposition conditions comprise a semiconductor precursor in the absence of an etchant material (such as HCl), the lag phases will be relatively short. In contrast, if an etchant is present the lag phases will be extended. Particular conditions may extend one of the lag phases T_1 or T_2 more than the other. Such can reduce the interval between T_1 and T_2 in some cases, and in other cases can increase the interval between T_1 and T_2.

[0041] The lag phases T_1 and T_2 are believed to result from nucleation phase/growth phase dynamics during deposition of semiconductor material. Specifically, there is initially a nucleation phase of the deposited semiconductor material during which there is substantially no increase in the thickness of the material over an underlying surface. The nucleation phase then progresses to a growth phase, with the

growth phase being defined as the phase in which there is a substantial increase in thickness of the deposited material. Accordingly, the lag phase times T_1 and T_2 correspond to the duration of the nucleation phases on the semiconductor surface and insulative material surface, respectively, and the lines 50 and 60 correspond to the growth phases on the semiconductor material surface and the insulative material surface, respectively. In some aspects, the growth phase can be considered a period of substantially linear increase in the thickness of a deposited material.

[0042] The increased lag phase over an insulative material surface relative to a semiconductor surface can be taken advantage of to selectively deposit a semiconductor material on the semiconductor surface relative to the insulative material surface. Specifically, an insulative material surface and a semiconductor material surface can both be exposed to a pulse of semiconductor precursor, but the pulse can be of a duration which exceeds the lag phase T_1 while being less than the lag phase T_2. Accordingly, there will be growth of semiconductor material on the semiconductor surface, but there will not be growth of semiconductor material on the insulative material surface.

[0043] An exemplary method is diagrammatically illustrated in Fig. 7. Specifically, Fig. 7 shows a graph of gas flow versus time for a pulse/purge sequence that can be utilized for growing semiconductor materials selectively over a semiconductor surface. Each pulse corresponds to flow of appropriate semiconductor material precursor within a reaction chamber to a sufficient concentration to grow semiconductor material over semiconductor surfaces and insulative material surfaces. The pulses are for a duration longer than the lag phase for growth on the semiconductor surface, but less than or equal to the lag phase for growth on the insulative material surface (i.e., of for a time longer than T_1 of Fig. 6, but no greater than the time T_2 of Fig. 6). After each pulse, the semiconductor material precursor is purged from within the reaction chamber.

[0044] In particular aspects, the semiconductor material which is deposited comprises, consists essentially of, or consists of one or both of silicon and germanium. In such aspects, the semiconductor material precursor utilized during the pulses can be selected from the group consisting of dichlorosilane, trichlorosilane, tetrachlorosilane, disilane, silane and germane.

[0045] The material utilized for the purge can comprise any suitable purge gas, and/or vacuum. If a purge gas is utilized, such can be inert relative to reaction with

exposed substrate surfaces in the reaction chamber, or in some aspects can be reactive with one or more exposed materials in the reaction chamber. In particular aspects, the purge will comprise flowing a gas through a reaction chamber, with such gas containing H_2. The gas can comprise a halogen-containing component in addition to the H_2, such as, for example, Cl_2, or a halogen acid, such as, for example, HCl. If HCl is utilized during the purge, such can be present in the reaction chamber to a concentration of less than 0.1 volume percent. The utilization of a halogen-containing material during the purge can be advantageous in that it can remove nucleated semiconductor materials from over insulative surfaces. However, it can slow down a deposition process by also removing deposited semiconductor material from over a semiconductor surface. Accordingly, the invention also encompasses aspects in which a purge gas does not include etchants. In some aspects, the purge gas utilizes H_2 without any halogen-containing components, and specifically, without any chlorine-containing components.

[0046] If halogen-containing material, or other etchant, is desired in the reaction chamber, such can be provided in the chamber during the pulsing of the semiconductor material into the reaction chamber alternatively to, or in addition to, providing the etchant during the purging. In exemplary aspects, HCl is present in the reaction chamber during the pulse of semiconductor material into the chamber, and is present to a concentration of less than 0.1 volume percent. The HCl can advantageously remove semiconductor material nucleating on insulative surfaces. A disadvantage of including etchants with deposition precursors is that the etchants can slow down a deposition process, and accordingly in some aspects it can be advantageous to not have etchants (such as, for example, Cl) present during the pulse of semiconductor material into a reaction chamber.

[0047] Fig. 8 illustrates an exemplary reaction apparatus 70 that can be utilized in particular aspects of the present invention. Apparatus 70 comprises a chamber 72. A substrate holder 74 is within the chamber, and is shown holding an exemplary substrate 76. Substrate 76 can correspond to, for example, a semiconductor wafer, such as, for example, a monocrystalline silicon wafer. An inlet 78 extends into the chamber, and is blocked by a valve 80. An outlet 82 also extends into the chamber, and is blocked by a valve 84.

[0048] In operation, materials are flowed into chamber 72 through inlet 78, and expelled from chamber 72 through outlet 82. The materials flowed into chamber 72 can be suitable reactants during a pulse of precursor into the chamber, and can be suitable

purge gases during a purge of materials from the chamber. Additionally, a vacuum (not shown) can be provided downstream of outlet 82 to assist in purging materials from within the chamber.

[0049] The apparatus 70 can be any suitable apparatus, including, for example, a chemical vapor deposition (CVD) apparatus, an atomic layer deposition (ALD) apparatus, a plasma-enhanced (PE) CVD or ALD apparatus, etc.

[0050] Figs. 9-12 illustrate an exemplary aspect of the invention. Fig. 9 shows a semiconductor wafer fragment 100 at a preliminary processing stage. Fragment 100 comprises a substrate 102 and an insulative material 104 over substrate 102. Substrate 102 can comprises identical materials to those discussed above for substrate 12 of Fig. 1. Accordingly, substrate 102 can comprise, consist essentially of, or consist of semiconductor materials, and in particular aspects will comprise, consist essentially of, or consist of one or both of silicon and germanium.

[0051] Substrate 102 comprises an upper surface 103. The portion of substrate 102 comprised by surface 103 can be monocrystalline or polycrystalline, and in particular aspects will comprise, consist essentially of, or consist of one or both of silicon and germanium in monocrystalline or polycrystalline form. The semiconductor material of surface 103 can be doped or undoped. Specifically, surface 103 can be comprised by a conductively-doped diffusion region (not shown) in particular aspects of the invention, or can be comprised by undoped semiconductor material in other aspects of the invention.

[0052] Insulative material 104 can comprise identical materials to those discussed above for material 14 of Fig. 1, and accordingly can comprise, consist essentially of, or consist of silicon in combination with one or both of nitrogen and oxygen.

[0053] Insulative material 104 comprises a surface 105. In particular aspects, surface 105 can comprise, consist essentially of, or consist of one or more of silicon dioxide, silicon nitride and silicon oxynitride. Materials 102 and 104 can be referred to as first and second materials, respectively, in the discussion that follows; and surfaces 103 and 105 can be referred to as first and second surfaces respectively.

[0054] In exemplary aspects of the invention, the wafer comprising fragment 100 is provided within a reaction chamber, such as, for example, the chamber above with reference to Fig. 8, and first and second surfaces 103 and 105 are exposed to at least one semiconductor material precursor. The surfaces are exposed to the precursor

under conditions in which growth of semiconductor material from the precursor over the first and second materials 102 and 104 will comprise a lag phase prior to a growth phase, and under which it takes longer for the growth phase to initiate on surface 105 of material 104 than on surface 103 of material 102. The precursor is injected within the chamber to a sufficient concentration for growth of semiconductor material from the precursor on both first surface 103 and second surface 105. However, the precursor concentration is maintained within the chamber for a duration only long enough for the growth phase to substantially occur on first surface 103, and not long enough for the growth phase to substantially occur on second surface 105. A growth phase is considered to have "substantially occurred" on a surface if a detectable layer of uniform thickness has formed on the surface, and not if nucleated islands are the only deposition on the surface. The duration that the precursor concentration is maintained in the chamber can be considered a pulse of the precursor within the chamber.

[0055] In some aspects, the deposition of semiconductor material on surfaces 103 and 105 can be considered to have a first activation time relative to surface 103, and a second activation time relative to surface 105. The term "activation time" refers to the time of the lag phase associated with growth of semiconductor material over the surfaces, and specifically is the time which elapses before the growth phase initiates. The activation time relative to surface 105 (the second activation time) is longer than the activation time relative to surface 103 (the first activation time). The semiconductor material precursor is pulsed into the chamber for a time longer than the first activation time and no greater than the second activation time. The pulse thus selectively deposits semiconductor material over the first surface 103 relative to the second surface 105.

[0056] The precursor utilized for deposition of semiconductor material over surface 103 can comprise at least one precursor selected from the group of silicon-containing precursors and germanium-containing precursors. Accordingly, the semiconductor material deposited over surface 103 can comprise, consist essentially of, or consist of one or both of silicon and germanium. If the semiconductor material comprises both silicon and germanium, it can be referred to as silicon/germanium. In particular aspects, the precursor can comprise one or more materials selected from the group consisting of dichlorosilane, trichlorosilane, tetrachlorosilane, disilane, silane and germane.

[0057] Fig. 10 shows fragment 100 after exposure of surfaces 103 and 105 to the semiconductor material precursor. A semiconductor material 110 is selectively

formed over surface 103 relative to surface 105. Semiconductor material 110 can comprise any suitable semiconductor material, and in particular aspects will comprise, consist essentially of, or consist of one or both of silicon and germanium.

[0058] The deposition of material 110 can be, in some aspects, considered a "blanket" deposition in that surfaces 103 and 105 are both exposed to precursor, even though the deposition is selective for the particular surface 103.

[0059] The formation of material 110 can be accomplished utilizing the various conditions discussed above with reference to Figs. 6 and 7. Accordingly, the formation of material 110 can be accomplished utilizing a semiconductor material precursor alone in the reaction chamber, or in combination with a halogen-containing material. Exemplary halogen-containing materials are halogen-containing acids (for example, HCl), and diatomic halogen molecules (for example, Cl_2). If HCl is present in the reaction chamber during deposition of semiconductor material 110, the HCl will preferably be present in the chamber to a concentration of less than or equal to about 0.1 volume percent (i.e., the HCl will be present to a concentration of from greater than 0 volume percent to less than or equal to about 0.1 volume percent).

[0060] In the shown aspect of the invention, material 110 is deposited to a thickness which is less than the initial thickness of material 104, and accordingly material 110 only partially fills a gap extending through material 104. Material 110 can be thick enough at the processing stage of Fig. 10 for particular applications. For other applications, it can be desired that a thicker amount of semiconductor material be provided. An exemplary thickness of material 110 is from about 10Å to about 5000Å.

[0061] Fig. 11 shows fragment 100 after another pulse of semiconductor material is utilized to selectively form a layer 112 of semiconductor material over the layer 110. The conditions utilized for forming layer 112 can be similar to, or identical to, the conditions utilized for forming semiconductor material 110. Specifically, it is noted that semiconductor material 110 comprises a surface 111 of semiconductor material. Accordingly, the conditions described above with reference to Figs. 6 and 7 can be utilized for selectively forming semiconductor material over surface 111 relative to the surface 105 of material 104.

[0062] Layers 110 and 112 can be considered to have been formed by the pulse/purge cycle of Fig. 7. Such pulse/purge cycle can be repeated multiple times to deposit a desired thickness of semiconductor material. Fig. 12 shows construction 100

after a layer 114 of semiconductor material is selectively formed over layer 112 relative to surface 105 of material 104.

[0063] Layers 110, 112 and 114 can comprise the same semiconductor material compositions as one another, or different compositions, and can be together considered to be a stack of semiconductor material layers. At least two of the layers will comprise different compositions relative to one another if different semiconductor material precursors, or semiconductor material precursor combinations, are utilized during formation of one of the layers than are utilized during formation of another of the layers. The layers 110, 112 and 114 can all be crystalline in particular aspects of the invention. Further, in some aspects of the invention layers 110, 112 and 114 can be epitaxially grown single crystal materials.

[0064] Figs. 13-17 illustrate another aspect of the invention. Fig. 13 shows a semiconductor wafer fragment 200 comprising a substrate 202, an isolation region 204 extending into the substrate, and a transistor gate 206 over the substrate. Substrate 202, isolation region 204 and transistor gate 206 can comprise the same compositions as discussed above with reference to Fig. 4 for substrate 22, isolation region 24 and transistor gate 26, respectively. Accordingly, substrate 202 can comprise, consist essentially of, or consist of monocrystalline semiconductor material, such as, for example, monocrystalline silicon; isolation region 204 can comprise, consist essentially of, or consist of silicon dioxide; and transistor gate 206 can comprise layers 208, 210 and 212 having identical compositions to layers 28, 30 and 32 described previously.

[0065] An anisotropically etched sidewall spacer 214 is adjacent a sidewall of transistor gate 206, and can comprise an identical composition as discussed above for spacer 34 of Fig. 4.

[0066] A conductively-doped diffusion region 216 extends within substrate 202 proximate gate 206, and can comprise an identical composition as the diffusion region 36 discussed above with reference to Fig. 4.

[0067] In an exemplary aspect, substrate 202 comprises an upper surface 203 consisting essentially of, or consisting of semiconductor material; isolation region 204 comprises an upper surface 205 consisting essentially of or consisting of, for example, silicon dioxide; layer 212 comprises an upper surface 213 consisting essentially of, or consisting of, for example, silicon nitride, silicon dioxide and/or silicon oxynitride; and sidewall spacer 214 comprises a surface 215 consisting essentially of, or consisting of, for example, silicon nitride, silicon dioxide, and/or silicon oxynitride.

[0068] Construction 200 can be exposed to the conditions discussed above with reference to Figs. 6 and 7 to selectively grow semiconductive material over surface 203 relative to surfaces 205, 213 and 215. Fig. 14 shows construction 200 after growth of semiconductor material 220 selectively over surface 203.

[0069] An upper surface of semiconductor material 220 can be utilized as a substrate in subsequent processing to form another semiconductor material 222 over material 220 as shown in Fig. 15. Additionally, an upper surface of semiconductor material 222 can be utilized as a substrate for selectively forming another semiconductor material 224 as shown in Fig. 16. The layers 220, 222 and 224 can all be crystalline in particular aspects of the invention, and in some aspects can be epitaxially grown single crystal materials.

[0070] The structure 200 of Fig. 16 advantageously has a substantially square outer corner 230 at the region where the problematic rounded corner 40 occurred in the prior art structure of Fig. 5. Accordingly, the problems discussed above relative to Fig. 5 can be alleviated, and in particular aspects even entirely overcome, utilizing the processing of the present invention.

[0071] The structure of Fig. 16 shows semiconductor materials 220, 222 and 224 as separate distinct layers from one another. As discussed previously, the invention includes processing in which the multiple layers formed through sequential pulse/purge cycles of the type described with reference to Fig. 7 have different compositions relative to one another, and such would form a structure of the type formed in Fig. 16. However, as was also discussed above, the invention encompasses processes in which the multiple pulse/purge cycles of the type described with reference to Fig. 7 form layers having the same composition as one another. In such aspect, the layers 220, 222 and 224 of Fig. 16 would not be distinguishable from one another in the structure of Fig. 16. Fig. 17 shows construction 200 at the processing stage of Fig. 16 in an aspect in which layers 220, 222 and 224 of Fig. 16 have the same composition as one another and merge to form a single semiconductor material 240. Fig. 17 also illustrates another exemplary advantageous aspect of the present invention in which there has been lateral overgrowth of semiconductor material 240 over isolation region 204. Such lateral overgrowth can help to reduce p-channel degradation relative to transistor devices lacking the overgrowth.

[0072] The invention described herein can provide numerous advantages relative to prior art processes. For instance, the invention can reduce the faceting

described with reference to Fig. 5; can increase lateral overgrowth of a semiconductor material as described above with reference to Fig. 17; can reduce processing time due to removal of etchant, or decreasing of etchant concentration relative to prior art processes; can increase the robustness of processes by removing the etchant that prior art processing was undesirably sensitive to; and can increase selectivity for semiconductor formation over semiconductor surfaces relative to other surfaces by substantially avoiding, and in some cases entirely avoiding, detectable growth of semiconductor materials on undesired surfaces, such as, for example, surfaces comprising silicon nitride, silicon dioxide, and/or silicon oxynitride.

CLAIMS

The invention claimed is:

1. A method for deposition of semiconductor material, comprising:

providing a substrate, the substrate comprising a first material and a second material;

exposing the first and second materials to at least one semiconductor material precursor under conditions in which growth of semiconductor material from the at least one precursor over the first and second materials comprises a lag phase period prior to a growth phase, and under which it takes longer for the growth phase to initiate on the second material than on the first material; and

the exposing being conducted for long enough for the growth phase to occur on the first material, but not for long enough for the growth phase to substantially occur on the second material.

2. The method of claim 1 wherein the growth phase of the semiconductor material on the first material forms a layer of the semiconductor material having a thickness of from about 10Å to about 5000Å.

3. The method of claim 2 wherein the semiconductor material is a single crystal material epitaxially grown over the first material.

4. The method of claim 1 wherein the exposing is conducted in a reaction chamber and comprises a pulse of the at least one precursor into the chamber followed by a purge to remove the at least one precursor substantially entirely from within the chamber.

5. The method of claim 4 wherein the purge utilizes one or more of H_2, Cl_2 and HCl.

6. The method of claim 5 wherein the purge utilizes H_2 without a chlorine-containing component.

7. The method of claim 4 wherein a sequence comprising two or more of the pulses is utilized to form a thickness of semiconductor material.

8. The method of claim 7 wherein the same semiconductor precursor is flowed into the chamber during each of the two or more pulses.

9. The method of claim 7 wherein a different semiconductor precursor is flowed into the chamber during one of the two or more pulses relative to another of the two or more pulses.

10. The method of claim 1 further comprising flowing an etchant into the reaction chamber during at least some of the exposing, and wherein the etchant is suitable for etching some of the semiconductor material.

11. The method of claim 1 wherein no etchant suitable for etching the semiconductor material is within the reaction chamber during the exposing.

12. The method of claim 1 further comprising flowing a halogen-containing material into the reaction chamber during at least some of the exposing.

13. The method of claim 12 wherein the halogen of the halogen-containing material is Cl.

14. The method of claim 12 wherein the halogen-containing material is HCl and is present in the reaction chamber to a concentration of less than or equal to about 0.1 volume percent.

15. The method of claim 1 wherein the semiconductor material consists essentially of one or both of silicon and germanium.

16. The method of claim 1 wherein the semiconductor material consists essentially of silicon.

17. The method of claim 1 wherein the semiconductor material consists essentially of germanium.

18. The method of claim 1 wherein the semiconductor material consists of one or both of silicon and germanium.

19. The method of claim 1 wherein the semiconductor material consists of silicon.

20. The method of claim 1 wherein the semiconductor material consists of germanium.

21. The method of claim 1 wherein the first material comprises a semiconductor material and wherein the second material comprises an electrically insulative material.

22. The method of claim 21 wherein the first material is monocrystalline or polycrystalline.

23. The method of claim 21 wherein the first material consists essentially of doped or undoped silicon.

24. The method of claim 23 wherein the second material consists essentially of silicon and one or both of oxygen and nitrogen.

25. The method of claim 21 wherein the first material consists of doped or undoped silicon.

26. The method of claim 25 wherein the second material consists of silicon and one or both of oxygen and nitrogen.

27. The method of claim 21 wherein the first material consists essentially of doped or undoped germanium.

28. The method of claim 27 wherein the second material consists essentially of silicon and one or both of oxygen and nitrogen.

29. The method of claim 21 wherein the first material consists of doped or undoped germanium.

30. The method of claim 29 wherein the second material consists of silicon and one or both of oxygen and nitrogen.

31. The method of claim 21 wherein the first material consists essentially of doped or undoped silicon/germanium.

32. The method of claim 31 wherein the second material consists essentially of silicon and one or both of oxygen and nitrogen.

33. The method of claim 21 wherein the first material consists of doped or undoped silicon/germanium.

34. The method of claim 33 wherein the second material consists of silicon and one or both of oxygen and nitrogen.

35. A method for deposition of semiconductor material, comprising:

providing a substrate within a reaction chamber, the substrate including a first material with a first surface and including a second material with a second surface;

providing a semiconductor material precursor having a first activation time associated therewith for forming semiconductor material over the first surface and a second activation time associated therewith for forming semiconductor material over the second surface, the second activation time being longer than the first activation time; and

providing a pulse of the semiconductor material precursor within the chamber, the pulse being maintained in the chamber for a time longer than the first activation time and no greater than the second activation time to selectively form semiconductor material from the semiconductor material precursor over the first surface relative to the second surface.

36. The method of claim 35 wherein the semiconductor material formed from the precursor deposits over the first surface as a crystalline layer.

37. The method of claim 35 wherein the pulse is followed with a purge utilizing one or more of H_2, Cl_2 and HCl to remove the semiconductor material precursor substantially entirely from within the chamber.

38. The method of claim 36 wherein the purge utilizes H_2 without a chlorine-containing component.

39. The method of claim 35 wherein two or more of the pulses are sequentially utilized to form a stack of semiconductor material.

40. The method of claim 39 wherein the same semiconductor precursor is flowed into the chamber during each of the two or more pulses.

41. The method of claim 39 wherein a different semiconductor precursor is flowed into the chamber during one of the two or more pulses relative to another of the two or more pulses.

42. The method of claim 35 further comprising flowing a halogen acid into the chamber during at least some of the time of the pulse of the semiconductor material precursor.

43. The method of claim 42 wherein the halogen acid is HCl.

44. The method of claim 42 wherein the halogen acid is HCl and is present in the reaction chamber to a concentration of less than or equal to about 0.1 volume percent.

45. The method of claim 35 wherein substantially no halogen acid is present within the chamber during the time of the pulse of the semiconductor material precursor.

46. The method of claim 35 wherein the semiconductor material precursor is selected from the group consisting of dichlorosilane, trichlorosilane, tetrachlorosilane, disilane, silane and germane.

47. The method of claim 35 wherein the semiconductor material of the semiconductor material precursor is silicon.

48. The method of claim 35 wherein the semiconductor material of the semiconductor material precursor is germanium.

49. The method of claim 35 wherein the first surface consists essentially of doped or undoped silicon.

50. The method of claim 49 wherein the second surface consists essentially of silicon and one or both of oxygen and nitrogen.

51. The method of claim 35 wherein the first material consists of doped or undoped silicon.

52. The method of claim 51 wherein the second material consists of silicon and one or both of oxygen and nitrogen.

53. The method of claim 35 wherein the first material consists essentially of doped or undoped germanium.

54. The method of claim 53 wherein the second material consists essentially of silicon and one or both of oxygen and nitrogen.

55. The method of claim 35 wherein the first material consists of doped or undoped germanium.

56. The method of claim 55 wherein the second material consists of silicon and one or both of oxygen and nitrogen.

57. The method of claim 35 wherein the first material consists essentially of doped or undoped silicon/germanium.

58. The method of claim 57 wherein the second material consists essentially of silicon and one or both of oxygen and nitrogen.

59. The method of claim 35 wherein the first material consists of doped or undoped silicon/germanium.

60. The method of claim 59 wherein the second material consists of silicon and one or both of oxygen and nitrogen.

61. A method for deposition of semiconductor material, comprising:

providing a substrate within a reaction chamber, the substrate having a first surface consisting essentially of one or more semiconductor materials, the substrate having a second surface consisting of one or more electrically insulative materials;

providing a pulse of at least one precursor selected from the group of silicon-containing precursors and germanium-containing precursors within the reaction chamber and utilizing the at least one precursor for depositing a substance comprising one or both of silicon and germanium over the substrate;

the depositing of the substance over the substrate occurring under conditions in which depositing of the substance over the first and second surfaces comprises nucleation phase/growth phase dynamics, and under which it takes longer for the growth phase to initiate over the second surface than over the first surface; and

the pulse having a sufficient duration to substantially initiate the growth phase over the first surface but not being of sufficient duration to substantially initiate the growth phase over the second surface.

62. The method of claim 61 wherein:

the pulse is a first pulse of the at least one precursor and forms a layer of the deposited substance;

the first pulse is followed with a purge to remove the at least one precursor substantially entirely from within the chamber; and

the purge is followed with a second pulse of the at least one precursor into the chamber; the second pulse being for a sufficient duration to substantially initiate the growth phase over the layer of the deposited substance but not of sufficient duration to substantially initiate the growth phase over the second surface.

63. The method of claim 62 wherein the purge utilizes at least one halogen-containing component.

64. The method of claim 62 wherein the purge utilizes no halogen-containing component.

65. The method of claim 62 wherein the purge utilizes H_2 and one or both of Cl_2 and HCl.

66. The method of claim 61 further comprising flowing a halogen-containing material into the chamber during at least some of the time of the pulse of the at least one precursor.

67. The method of claim 61 further comprising flowing a halogen acid into the chamber during at least some of the time of the pulse of the at least one precursor.

68. The method of claim 67 wherein the halogen acid is HCl.

69. The method of claim 67 wherein the halogen acid is HCl and is present in the reaction chamber to a concentration of less than or equal to about 0.1 volume percent.

70. The method of claim 61 wherein substantially no halogen acid is present within the chamber during the time of the pulse of the at least one precursor.

71. The method of claim 61 wherein the at least one precursor is selected from the group consisting of dichlorosilane, trichlorosilane, tetrachlorosilane, disilane, silane, germane and mixtures thereof.

72. The method of claim 61 wherein the first surface is polycrystalline.

73. The method of claim 61 wherein the first surface is monocrystalline.

74. The method of claim 61 wherein the first surface consists essentially of one or both of germanium and silicon.

75. The method of claim 61 wherein the first surface consists of one or both of germanium and silicon.

76. The method of claim 61 wherein the second surface consists essentially of silicon and one or both of oxygen and nitrogen.

77. The method of claim 61 wherein the second surface consists of silicon and one or both of oxygen and nitrogen.