CLAIMS

1. An integrated circuit comprising:

a first network interface processor for communicating with a first network;

a second network interface processor for communicating with a second network, wherein the second network interface processor is a separate processor from the first network interface processor;

a first unidirectional interconnect connecting the first and second network interface processors;

wherein the first unidirectional interconnect is configured to allow data transfer from the first network interface processor to the second network interface processor via the first unidirectional interconnect and to prevent data transfer from the second network interface processor to the first network interface processor via the first unidirectional interconnect,

wherein the first network interface processor is configured to transmit data to the second network interface processor via the first unidirectional interconnect; and

the second network interface processor is configured to receive data from the first network interface processor via the first unidirectional interconnect; and

a second unidirectional interconnect connecting the first and second network interface processors;

wherein the second unidirectional interconnect is configured to allow data transfer from the second network interface processor to the first network interface processor via the second unidirectional interconnect and to prevent data transfer from the first network interface processor to the second network interface processor via the second unidirectional interconnect,

wherein the second network interface processor is configured to transmit data to the first network interface processor via the second unidirectional interconnect;

the first network interface processor is configured to receive data from the second network interface processor via the second unidirectional interconnect; and

wherein the integrated circuit is configured to only permit transmission of data of a predetermined size via the second unidirectional interconnect.

2. The integrated circuit of claim 1, wherein the first unidirectional interconnect comprises a first data diode configured to allow data transfer from the first network interface processor to the second network interface processor via the first unidirectional interconnect and to prevent data transfer from the second network interface processor to the first

network interface processor via the first unidirectional interconnect, optionally, wherein the data diode is an optical data diode.

3. The integrated circuit of claim 1 or claim 2, wherein the first unidirectional interconnect further comprises a first switch configured to disable the first unidirectional interconnect such that no data transfer between the first network interface processor and the second network interface processor via the first unidirectional interconnect is possible when the first switch is open.

4. The integrated circuit of claim 3, further comprising a secure area configured to control operation of the first switch.

5. The integrated circuit of claim 4, wherein the secure area comprises a hardware root of trust configured to control operation of the first switch.

6. The integrated circuit of any preceding claim, wherein the integrated circuit is configured to generate authentication data for data received at the first network interface processor from the first network.

7. The integrated circuit of claim 1, wherein the second unidirectional interconnect comprises a second data diode configured to allow data transfer from the second network interface processor to the first network interface processor via the second unidirectional interconnect and to prevent data transfer from the first network interface processor to the second network interface processor via the second unidirectional interconnect, optionally, wherein the data diode is an optical data diode.

8. The integrated circuit of claim 1 or claim 7, wherein the second unidirectional interconnect further comprises a second switch configured to disable the second unidirectional interconnect such that no data transfer between the first network interface processor and the second network interface processor via the second unidirectional interconnect is possible when the second switch is open.

9. The integrated circuit of claim 8, when dependent upon claim 4 or claim 5, wherein the secure area is configured to control operation of the second switch.

10. The integrated circuit of any of claims 1 to 9, when dependent upon claim 4 or claim 5, wherein the integrated circuit is configured to authenticate data received at the second network interface processor from the second network by verifying authentication data associated with the received data.

11. The integrated circuit of claim 10, wherein the received data is decrypted by the second network using a key issued by the secure area.

12. The integrated circuit of any preceding claim, wherein the secure area has a specific non-reversible memory configuration so that depending on its non-reversible configuration, the secure area forces the switch or switches to a permanent and non-reversible lock of the respective direction.