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SEMICONDUCTOR DEVICE AND FABRICATION PROCESS THEREOF

The present invention relates to a semiconductor device and to a process for fabricating such a semiconductor device.

In a semiconductor device in which MIS field-effect transistors (MISFETS) are used as circuit components, it has been proposed to connect directly a polysilicon gate and a source or drain region doped with an impurity, in each of or between the MISFETS. In the construction shown in Fig. 1 of the accompanying drawings, for example, a polysilicon gate 2 of an n-channel MOSFET Q_1 formed over a semiconductor substrate 1 is in direct contact with a portion of a source or drain region 3 of an n-channel MOSFET Q_2. In order to effect this direct contact, a contact hole 5 is formed in part of an insulating film 4 over, for example, the source region of MOSFET Q_2, and the source region 3 is doped with an n-type impurity to a high concentration through this hole to form an n^+-type contact region 6, to which the gate 2 of the other n-channel MOSFET Q_1 is in direct contact.

Since the contact region 6 is formed by diffusion, its depth X_j is liable to be greater than that of the source region 3. As a result, a leak X_1 is likely to occur between the n-type MOSFET Q_1 and

the contact region 6 which are arranged so that a field oxide film 7 is inserted between them, and a leak X_2 is likely to occur because of e.g. a drop in V_{th}, between the contact region 6 and a drain region 9. It is considered that those leaks are the cause of deterioration of the characteristics of these transistors.

It is thought that in order to prevent these leaks, both the space a between the contact region 6 and a channel portion 8 and the width b of the field-insulating film 7 should be increased. To provide mask margins during the formation of the contact region 6, moreover, it is necessary to make the dimensions a and b larger. These restrictions on the dimensions a and b impede the "scale-down", i.e. the miniaturisation, of the elements, raising the problem that a high degree of integration is difficult to achieve.

The present invention seeks to provide a device in which the contact region between e.g. a polysilicon gate and a source or drain of a field effect transistor does not suffer the defects of the prior art contacts.

To achieve this, a first aspect of the invention provides a semiconductor device comprising:

a) a semiconductor substrate having a first impurity doped region which is a source or drain region of a MISFET in a surface region thereof;

b) a polysilicon layer, which is a gate electrode of the or another MISFET, over the semiconductor substrate; and

c) a metal silicide layer extending from the first impurity doped region to the polysilicon layer directly to connect electrically the first impurity doped region and the polysilicon layer, the metal silicide layer extending onto the surface of the polysilicon layer furthest from the substrate.

Such an arrangement may have the further advantage that the reliability of the contacts is improved.

The metal silicide layer contacts components of the device, which components may be part of the same semiconductor element, or may be two different elements. One may be a first impurity region in a semiconductor substrate (forming e.g. a source or drain region) with the other a polysilicon layer (forming e.g. a gate).

According to a second aspect of the invention there is provided a process of fabricating a semiconductor device, comprising the steps of:

a) forming at least one MISFET of the semiconductor device, the at least one MISFET including an impurity doped region as a source or drain region in a surface region of a semiconductor substrate and a polysilicon layer as a gate electrode extending over the semiconductor substrate;

b) forming a metal layer, of a metal which forms a silicide, continuously extending from the polysilicon layer to the impurity doped region; and

c) selectively turning the metal layer into the silicide thereof to form a metal silicide layer over the

polysilicon layer and the impurity doped region.

By forming a metal film, turning it into its silicide and then removing residual metal, after the removal of the side walls of the polysilicon, moreover, the polysilicon and the impurity-doped region may be connected by the metal silicide.

Embodiments of the invention will now be described in detail, by way of example, with reference to the accompanying drawings, in which:

Figure 1 is a section through the construction of a connection which has been proposed prior to the

present invention and has already been described;

Figure 2 is a section through a device being a first embodiment of the present invention;

Figure 3 is a top plan view of the embodiment of Figure 2;

Figure 4 is a circuit diagram of the embodiment of Figure 2;

Figures 5(A) to 5(F) are sectional views illustrating the steps in the fabrication process of the first embodiment;

Figure 6 is a section through a device being a second embodiment of the present invention;

Figure 7 is a top plan view of the second embodiment of Figure 6; and

Figures 8(A) to (D) are sections illustrating steps in the fabrication process of the second embodiment.

Figures 2 to 4 show one embodiment of a semiconductor device of the present invention. As shown in Figures 2 and 3, n-channel MOSFETS Q_A and Q_B are arranged at right angles to each other on the main surface of a p-type semiconductor substrate 11, for example, and are isolated by a field insulating film 12. MOSFET Q_A has a polysilicon gate 14 formed on a gate-insulating film 13, and source and drain

regions 15 which are doped with an n-type impurity. The other MOSFET, Q_B, similarly has a polysilicon gate 16 and source-drain regions 17. One end portion 14a of the polysilicon gate 14 of MOSFET Q_A may extend over one of the source-drain regions 17 of MOSFET Q_B, and is connected to that source or drain region 17. More specifically, an end

portion of the polysilicon gate 14 is arranged over the source or drain region 17. One portion of a side wall 21, of silicon oxide, on the side of the polysilicon gate has been removed by, e.g., a process to form an opening 18 to the source or drain region 17 of MOSFET Q_B. The electrical connection between the source or drain region 17 and the polysilicon gate 14 is effected by metal silicide layers 19 and 20 which are formed so as to extend from the surface of the source or drain region 17 over the upper and side surfaces of the polysilicon gate 14. Side walls 21 and 22 made of silicon oxide (SiO_2) are formed over the side surfaces of the polysilicon gates 14 and 16, except for the contact. The device of this construction is formed into a circuit such as that shown in Figure 4. A metal silicide layer 23 connected to an element outside the figure is formed on the upper face of the polysilicon gate 16.

The process of fabricating the device of this construction will now be described with reference to Figures 5(A) to (F).

First of all, the field-insulating film 12 and the gate-insulating film 13 (200 Å) made of silicon oxide are formed on the main surface of the p-type semiconductor substrate 11, e.g., of silicon as shown in Figure 5(A), and the polysilicon gates 14 and 16 are formed thereon by the deposition and patterning (or etching) of polysilicon. The n-type impurity ions are then implanted by

a self-alignment method into the main surface of the semiconductor substrate 11, to form the source and drain regions 15 and 17. This forms the two MOSFETs Q_A and Q_B.

Next, as shown in Figure 5(B), silicon oxide films 21A and 22A (200 Å) are formed over the upper and side surfaces of the polysilicon gates 14 and 16 by thermal oxidation of silicon. The, after an SiO_2 film (4000 – 5000 Å) has been formed over the whole surface by a CVD method, as shown in Figure 5(C), it is removed by reactive ion etching (RIE), or a similar method, from the upper surfaces of the polysilicon gates 14 and 16 and from the source and drain regions. During this time, the silicon oxide film is not removed from the sides of the polysilicon gates 14 and 16, to form the side walls 21 and 22. With regard to formation of the side walls, note Tsang, et al., "Fabrication of High-Performance LDDFET's With Oxide Sidewall-Spacer Technology", in IEEE Transactions on Electron Devices, Vol. ED-29, No. 4 (April 1982), pages 590-6, the contents of which is incorporated herein by reference. As shown in Figure 5(D), parts of the side walls 21 and 22 are also subjected to selective wet etching to etch away the side walls where wiring will be required using a resist film as a mask. In this embodiment, the part thus removed is a portion of the side wall 21 of the polysilicon gate 14 of MOSFET Q_A. The side wall

21 of the polysilicon gate 14 is etched to form the connection opening 18 for the silicon gate 14 and the source or drain region 17. While the opening 18 is being formed, the portion of the side wall 21 of the polysilicon gate 14 which faces the opening 18 is etched away.

In addition, as shown in Figure 5(E), a metal such as molybdenum (Mo) or the like is deposited (by sputtering) over the whole surface to form a metal layer 24 (500 Å), which is then subjected to a heat treatment (in N_2 gas). As a result, as shown in Figure 5(F), metal silicide layers 23, 19, 20 and 25 (about 1000—2000 Å) are formed over the portion at which the metal layer 24 and the silicon are in contact, i.e., the upper surface of the polysilicon gate 16, partially over the upper and side surfaces of the polysilicon gate 14, and over the source and drain regions 17, respectively. The metal silicide layer 20 formed over the side surfaces of the polysilicon gate 14, in particular, connect the polysilicon gate 14 and the source or drain region 17 directly. The gate-insulating film 13 is interposed between the polysilicon gate 14 and the source or drain region 17, but the metal silicide layers formed over these two parts are brought into connection with each other by a bridge action in which they protrude to provide a connection. Thus, the metal silicide can be formed in self-alignment with the side wall 21 and the field oxide 12; note Figure 3.

The metal layers are then etched so that the metal layer 24 which was not turned into the silicide is etched off to leave the metal silicide layers 23, 19, 20 and 25 alone, completing the construction shown in Figure 2. During this time, a mask can be used, formed over the bridge portion, to block the etching of the metal over that portion, so that such portion, if needed for the connection at the bridge portion, may be retained between the polysilicon gate 14 and the source or drain region 17.

According to the semiconductor device with the construction described above, the metal silicide wiring step can be utilized unchanged to realize a direct contact between the polysilicon gate 14 and the source or drain region 17 by the metal silicide. Because of the connection by the metal silicide layers 19 and 20, moreover, the connection resistance is low and the reliability is high.

The contact region is made redundant, and can be eliminated, to eliminate the danger of deterioration of the characteristics due to leaks between the MOSFETs and the channel portions. As a result, as shown in Figure 2, the dimension $\underbrace{a_1}_{(0.3\mu m)}$ between the opening 18 and the gate 16 and the dimension $\underbrace{b_1}_{(1\mu m)}$ of the field insulating film 12 can both be reduced, to effect a high degree of integration of the elements.

Figures 6 and 7 show another embodiment of the present invention, in which a polysilicon gate 34 of one MOSFET Q_C is connected directly to one of source-drain regions 35, i.e., a source region 35a in the present embodiment, by a metal silicide layer 36.

As shown in Figure 8(A), more specifically, the polysilicon gate 34 is formed on a p-type semiconductor substrate 31 over a gate-insulating film 33, and is then doped with an n-type impurity to form the source-drain regions 35. As shown in Figure 8(B), after a SiO_2 film is formed by the CVD method, a silicon oxide film (side walls 37 at both sides) 37A is then formed on both the side surfaces and the upper surface of the polysilicon gate 34.

One side wall 37 of the polysilicon gate 34 is etched away through an opening, as shown in Figure 8(C). As further shown in Figure 8(C), the silicon oxide film on the upper surface of the polysilicon gate 34 and on the side wall 37 etched away has also been removed, e.g., by RIE. In addition, as shown in Figure 8(D), a metal layer 39 is formed over the whole surface and is turned into its silicide, e.g., by heat treatment to form the metal silicide layer 36 extending over the source region 35a to one side surface and the upper surface of the polysilicon gate 34.

The metal layer is etched away to leave the metal silicide layer 36, and form the semiconductor

construction shown in Figures 6 and 7.

Since the contact region can be omitted in the present embodiment as well, characteristic deterioration can be prevented to increase the reliability, and facilitate the fabrication.

Since the contact region can be omitted to remove the danger of deterioration of characteristics due to leaks, moreover, no masking margin need be considered when determining the dimensions of the metal silicide layer 36 of Figure 7, so that the dimensions can be reduced to enable miniaturization of the elements.

As can be appreciated from the foregoing, the following beneficial and advantageous results are obtained through use of the present invention:

(1) After the side walls of the polysilicon gates are removed, the metal silicide is formed over the polysilicon gate and the source or drain region to provide connection therebetween. As a result, the contact region, which is necessary in the prior art, can be omitted to remove the deterioration of characteristics due to leaks, so that a highly reliable connection structure can be obtained.

(2) Because the contact region is not necessary, leaks between the MOSFETs and the channel portions do not occur, so that the dimensions of the opening over the source or drain region and of the field-insulating film can be reduced, enabling the miniaturization of the

elements to provide a high degree of integration.

(3) Since the metal silicide steps of the prior art, other than the step of etching away the side walls of the polysilicon gate, can be used almost unchanged, the process can be simplified to facilitate fabrication.

(4) Since there is no necessity for a contact region, the source and drain regions can be made shallower to suit them for "scale-down".

Although the invention has been described above in connection with embodiments thereof, it should not be limited to these embodiments. For example, the metal of the metal silicide need not be limited to Mo alone; platinum (Pt), tungsten (W), titanium (Ti) or tantalum (Ta) can be used therefor. Moreover, the silicide pattern may be changed as required, in accordance with the circuit. The present invention also has application in applying lightly doped Drain/Source Field Effect Transistor (LDDFET) structure to switching MOSFETs of memory cells of a DRAM or a SRAM.

While various embodiments in accordance with the present invention have been described, it is understood that the invention is not limited to those embodiments, but is susceptible of numerous changes and modifications as known to those skilled in the art.

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CLAIMS:

1. A semiconductor device comprising:

a) a semiconductor substrate having a first impurity doped region which is a source or drain region of a MISFET in a surface region thereof;

b) a polysilicon layer, which is a gate electrode of the or another MISFET, over the semiconductor substrate; and

c) a metal silicide layer extending from the first impurity doped region to the polysilicon layer directly to connect electrically the first impurity doped region and the polysilicon layer, the metal silicide layer extending onto the surface of the polysilicon layer furthest from the substrate.

2. A semiconductor device according to claim 1, wherein the polysilicon layer and the first impurity doped region overlap and are separated from each other by an insulating layer on the semiconductor substrate.

3. A semiconductor device according to claim 1 or claim 2, further comprising:

d) a field oxide film on the semiconductor substrate;

e) a thin insulator film on the semiconductor substrate; and

f) a side wall of insulator material at the sides of the polysilicon layer except for portions of the sides in contact with the metal silicide layer;

wherein the polysilicon layer is on said thin insulator film and the field oxide film; wherein said first

impurity doped region is in self-alignment with the polysilicon layer and the field oxide film; and wherein the metal silicide layer is in self-alignment with the field oxide film and the side wall.

4. A semiconductor device according to any one of claims 1 to 3 wherein the first impurity doped region is a source or drain region of a first field effect transistor and the polysilicon layer is a gate electrode of a second field effect transistor.

5. A semiconductor device according to claim 4, wherein the first and second MOSFETs are substantially at right angles to each other.

6. A semiconductor device substantially as herein described with reference to and as illustrated in Figs. 2 to 5 or Figs. 6 to 8 of the accompanying drawings.

7. A process of fabricating a semiconductor device, comprising the steps of:

a) forming at least one MISFET of the semiconductor device, the at least one MISFET including an impurity doped region as a source or drain region in a surface region of a semiconductor substrate and a polysilicon layer as a gate electrode extending over the semiconductor substrate;

b) forming a metal layer, of a metal which forms a silicide, continuously extending from the polysilicon layer to the impurity doped region; and

c) selectively turning the metal layer into the silicide thereof to form a metal silicide layer over the

polysilicon layer and the impurity doped region.

8. A process according to claim 7, wherein, after step c), portions of the metal layer not turned into the silicide are removed by etching.

9. A process according to claim 7 or claim 8, wherein the polysilicon layer has insulating side walls at the sides thereof, and wherein, prior to forming the metal layer, portions of the insulating side walls closest to the impurity doped region are removed, whereby the metal layer is formed directly contacting the sides of the polysilicon layer.

10. A process according to any one of claims 7 to 9, wherein there are at least one plurality of elements, with one of the elements including the impurity doped region and another of the elements including the polysilicon layer.

11. A process according to any one of claims 7 to 9, wherein there is a single element including both the impurity doped region and the polysilicon layer.

12. A process of fabricating a semiconductor device substantially as any one herein described with reference to Figs. 2 to 8 of the accompanying drawings.