CLAIMS

1. An integrated circuit (IC) structure, comprising:

a non-planar fin having a source and a drain, wherein the fin comprises silicon;

a transistor gate on the non-planar fin between the source and the drain, wherein the transistor gate comprises:

a gate trench formed between transistor gate sidewalls;

a gate dielectric on the fin, wherein the gate dielectric is formed from hafnium silicon oxide;

a non-planar NMOS gate electrode disposed in the gate trench formed between the transistor gate sidewalls, wherein the transistor gate sidewalls are on opposing sides of the non-planar NMOS gate electrode, wherein the non-planar NMOS gate electrode comprises:

a NMOS work-function material conformally deposited within the gate trench and comprises a composition including aluminum, titanium, and carbon;

a titanium-containing gate fill barrier conformally deposited adjacent to the NMOS work-function material; and

a tungsten-containing gate fill material being disposed adjacent to the titanium-containing gate fill barrier,

a capping structure being disposed in a recess between the transistor gate sidewalls and over a recessed non-planar NMOS gate electrode, wherein a portion of the non-planar NMOS gate electrode is removed to form the recess and the recessed non-planar NMOS gate electrode, wherein the capping structure comprises silicon nitride;

a dielectric layer adjacent to the transistor gate sidewalls,; and

a contact opening formed through the dielectric layer to expose one of the source and the drain and the contact opening is configured to be deposited with a conductive material.

2. The integrated circuit (IC) structure of claim 1, wherein the composition of the NMOS work-function material comprises between about 20 to 40% by weight aluminum, between about 30 to 50% by weight titanium, and between about 10 to 30% by weight carbon.

3. The integrated circuit (IC) structure of claim 1, wherein the composition of the NMOS work-function material comprises about 33% by weight aluminum, about 43% by weight titanium, and about 24% by weight carbon.

4. The integrated circuit (IC) of claim 1, wherein the dielectric layer is made of a dielectric material different from the pair of gate spacers and the capping structure.

5. The integrated circuit (IC) of any one of the preceding claims, wherein a PMOS work function material is being deposited, within the gate trench, after the gate dielectric and before the NMOS work function material.

6. A method of fabricating an integrated circuit (IC) structure, comprising:

forming a non-planar fin, wherein the fin comprises silicon;

forming a sacrificial transistor gate on the fin;

depositing a sidewall dielectric material layer over the sacrificial transistor gate and the fin;

forming transistor gate sidewalls from a portion of the sidewall dielectric material layer, wherein the transistor gate sidewalls are on opposing sides of the sacrificial non-planar transistor gate;

forming a source in the fin on one side of the sacrificial transistor gate;

forming a drain in the fin on an opposing side of the sacrificial transistor gate;

removing the sacrificial transistor gate to form a gate trench between the transistor gate sidewalls, wherein a portion of the non planar fin is exposed;

forming a transistor gate in the gate trench, comprising:

forming a gate dielectric on the fin, wherein the gate dielectric is formed from hafnium silicon oxide;

forming a non-planar NMOS gate electrode on the gate dielectric, wherein forming the NMOS gate electrode comprises:

conformally depositing a NMOS work-function material within the gate trench, and comprises a composition including aluminum, titanium, and carbon;

conformally depositing a titanium-containing gate fill barrier adjacent to the NMOS work function material; and

depositing a tungsten-containing gate fill material adjacent to the titanium-containing gate fill barrier;

removing a portion of the non-planar NMOS gate electrode to form a recess between the transistor gate sidewalls;

forming a capping structure within the recess and over the recessed non-planar NMOS gate electrode, wherein the capping structure comprises silicon nitride;

forming a dielectric layer adjacent to the sidewalls,;

forming a contact opening through the dielectric layer to expose one of the source and the drain; and

depositing the contact opening with a conductive material.

7. The method of claim 6, wherein the composition of the NMOS work-function material comprises between about 20 to 40% by weight aluminum, between about 30 to 50% by weight titanium, and between about 10 to 30% by weight carbon.

8. The method of claim 6, wherein the composition of the NMOS work-function material comprises about 33% by weight aluminum, about 43% by weight titanium, and about 24% by weight carbon.

9. The method of claim 6, wherein the dielectric layer is made of a dielectric material different from the transistor gate sidewalls and the capping structure.

10. The method of claim 6, further including: conformally depositing a PMOS work-function material adjacent to the transistor gate side walls; and removing a portion of the PMOS work-function material within areas for fabrication of the non-planar NMOS gate electrode prior to depositing the NMOS work-function material.

11. The method of claim 10, wherein conformally depositing the PMOS work-function material comprises conformally depositing a titanium nitride PMOS work-function material.