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COMPLETE SPECIFICATION

DRAWINGS ATTACHED

Semiconductor Devices and Circuits

We, RADIO CORPORATION OF AMERICA, a Corporation organized under the laws of the State of Delaware, United States of America, of 30, Rockefeller Plaza, City and State of New York, United States of America, do hereby declare the invention, for which we pray that a patent may be granted to us, and the method by which it is to be performed, to be particularly described in and by the following statement:—

This invention relates in general to semiconductor devices and to signal translating circuits employing same.

According to the present invention, there is provided a semiconductor device with a substrate of semiconductive material having a first conductivity, said substrate having two major surfaces, spaced drain and source regions arranged on one of said major surfaces of said substrate defining the ends of a conductive channel in said one major surface, said drain and source regions and said channel being of different resistivity from and/or of opposite conductivity type to said substrate, said drain and source regions effectively forming respective rectifying junctions with said substrate, a gate region being formed of insulating material and extending over at least a portion of said channel in said major surface of said substrate, electrodes respectively arranged on said source, drain and gate regions and adapted to have current flowing in said channel when a difference of potential is applied between said source and drain electrodes with no charge being present from said gate electrode or gate region, and electrical connecting means arranged on said other major surface of said substrate.

The present invention also provides a sig-

nal translating circuit including the aforementioned semiconductor device and including means connecting said gate, source and drain electrodes as a signal translating circuit, and means for applying a potential to said substrate to control the efficiency of translation of said circuit.

Referring to the accompanying drawings: FIGURE 1 is a diagrammatic view of a field effect transistor embodying the invention;

FIGURE 2 is a cross section view taken along line 2-2 of FIGURE 1;

FIGURE 3 is a symbolic representation of an insulated gate field effect transistor;

FIGURE 4 is a graph showing a family of drain current versus drain voltage curves, for various values of gate-to-source voltages for the transistor of FIGURE 1;

FIGURE 5 is a schematic circuit diagram of an amplifier circuit embodying the invention;

FIGURE 6 is a schematic circuit diagram of a tuned high frequency amplifier embodying a feature of the invention;

FIGURE 7 is a schematic circuit diagram of a high frequency amplifier circuit utilizing two field effect transistors connected in parallel having a transconductive versus gate voltage, composite characteristic with remote cut-off;

FIGURE 8 is a schematic circuit diagram partly in block form of a portion of a signal receiver including a gain controlled r.f. amplifier circuit;

FIGURE 9 is a schematic circuit diagram of the r.f. amplifier stage of a signal receiver, similar to the r.f. amplifier stage shown in FIGURE 8, illustrating another embodiment of a feature of the invention;

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FIGURE 10 is a schematic circuit diagram of another high frequency amplifier circuit embodying a feature of the invention; and

FIGURE 11 is a graph showing the transconductance vs. gate voltage characteristic of a single field effect transistor and the composite characteristic of a pair of field effect transistors having different gate bias voltages.

Referring now to the drawings and particularly to FIGURE 1, a field effect transistor 10 which may be used with circuits embodying the invention includes a body 12 of semiconductor material. The body 12 may be either a single crystal or polycrystalline and may be made from any material of the semiconductor art. For example, the body 12 may be nearly intrinsic silicon, such as for example lightly doped P-type silicon of 100 ohm-cm. material.

In the manufacture of a device shown in FIGURE 1, heavily doped silicon dioxide is deposited over the surface of the silicon body 12. The silicon dioxide is doped with N-type impurities. By means of a photo-resist and acid etching, or other suitable technique, the silicon dioxide is removed where the gate electrode is to be formed, and around the outer edges of the silicon wafer as viewed in FIGURE 1. The deposited silicon dioxide is allowed to remain over those areas where the source-drain regions are to be formed.

The body 12 is then heated in a suitable atmosphere such as in water vapor so that exposed silicon areas are oxidized to form grown silicon dioxide layers indicated by the lightly stippled areas of FIGURE 1. During the heating process, impurities from the deposited silicon dioxide layer diffuse into silicon body 12 to form the source and drain regions. FIGURE 2 shows the source-drain regions labelled *S* and *D* respectively.

By means of another photo-resist and acid etching or like step the deposited silicon dioxide over part of the source-drain diffused regions is removed. Electrodes are formed for the source, drain and gate regions by evaporation of a conductive material by means of an evaporation mask. The conductive material evaporated may be chromium and gold in the order named, for example used, but other suitable metals may be used.

The finished wafer is shown in FIGURE 1, in which the stippled area between the outside boundary and the first dark zone 14 is grown silicon dioxide. The white area 16 is the metal source electrode. Dark zones 14 and 18 are deposited silicon dioxide zones overlying the diffused source region and the dark zone 20 in deposited silicon dioxide zone overlying the diffused drain region. White areas 22 and 24 are the metallic gate and drain electrodes respectively. The stippled zone 28 is a layer of grown silicon di-

oxide on a portion of which the gate electrode 22 is placed and which insulates the gate electrode 22 from the substrate silicon body 12 and from the source and drain electrodes as shown in FIGURE 2.

As can best be seen in FIGURE 2 the silicon wafer is mounted on a conductive base or header 26. The layer of grown silicon dioxide 28 on which the gate electrode 22 is mounted, overlies an inversion layer 75 or conducting channel *C* connecting the source and drain regions. The gate electrode 22 is arranged closer to the source region *S* so that the distance between the source region *S* and the gate electrode 22 is smaller than the distance between the gate electrode 22 and the drain region *D*. If desired, the gate electrode may overlap the deposited silicon dioxide layer 18. The advantages obtained by the configuration shown in FIGURES 1 and 2 will be pointed out subsequently in conjunction with the description of FIGURES 5 and 6.

FIGURE 3 is a symbolic representation of the insulated gate field effect transistor previously described in FIGURES 1 and 2. There is shown the gate electrode *G*, the drain electrode *D*, the source electrode *S*, and the substrate of semiconductor material *Si*. The gate electrode is closer to the source electrode *S* than to the drain electrode *D* as described with reference to FIGURES 1 and 2. It should be noted that electrodes *D* and *S* operate as the drain and the source electrodes as a function of the polarity of the bias potential applied therebetween, i.e. the electrode to which a positive bias potential is applied (relatively to the bias potential applied to the other electrode) operates as the drain electrode.

The drain and source electrodes are connected to each other by the conductive channel *C*. The electrons flow from source to drain in this thin channel region close to the surface. The conductive channel *C* is shown in FIGURE 2 in dotted lines.

FIGURE 4 is a family of curves 30-39 illustrating the drain current versus drain voltage characteristic of the transistor of FIGURE 1 for different values of gate-to-source voltage. A feature of an insulated-gate field effect transistor is that the zero bias characteristic can be at any of the curves 30-39. In FIGURE 4 the curve 37 corresponds to the zero bias gate-to-source voltage. Curves 38 and 39 represent positive gate voltages relative to the source and the curves 30-36 represent negative gate voltages relative to the source.

The location of the zero bias curve can be selected during the manufacture of this transistor, i.e. by controlling the time and/or temperature of the step of the process when the silicon dioxide layer 28 shown in FIGURES 1 and 2 is grown.

Reference is now made to FIGURE 5 which is a schematic diagram of a signal translating circuit in the form of an amplifier circuit employing an insulated gate field effect transistor 40 similar to the one described in FIGURES 1, 2 and 3. The transistor 40 has a source electrode 42, a drain electrode 44, a gate electrode 46 and a substrate of semiconductor material 48. The source electrode 42 is connected to a point of reference potential shown as ground. The drain electrode 44 is connected through a resistor 56 to the positive terminal of a source of bias potential 60. The negative terminal of the bias potential source 60 is connected to ground.

In the present instance the electrode 44 is physically spaced farther from the gate electrode 46 than electrode 42 and hence is identified as the drain electrode. The electrode 42 positioned closer to the gate electrode is identified as the source electrode. It should be noted that the electrode 44 could be connected to function as the source electrode, and the electrode 42 as the drain electrode, but without the benefits gained by the offset spacing arrangement.

The gate electrode 46 is biased to a desired bias potential from a source of bias potential (not shown) connected to terminal 54 and through a resistor 52. It is to be understood that (1) the source of bias potential for the gate electrode 46 may comprise the source 60 with an appropriate voltage divider network, and (2) the resistor 52 may be grounded depending on the drain current v. drain voltage characteristic of the transistor used and the desired operating region of the transistor.

Input signals are coupled to the gate electrode 46 through a coupling capacitor 50 from a signal source (not shown). Output signals are derived across the resistor 56 and coupled through a coupling capacitor 58 to a utilization circuit (not shown). The substrate 48 is connected to the source electrode 42.

The transistor 40 is an insulated offset gate field effect transistor, as shown in FIGURES 1 and 2. With the gate electrode closer to the source electrode, the inherent capacitance between the gate electrode and the drain electrode is decreased and consequently the inherent feedback through this capacitance is reduced so that operating stability is obtained throughout a wide range of frequencies without using a neutralizing network. At very high frequencies, some neutralization may be required, but the criticality of design of such neutralizing circuit is substantially reduced because of the reduced output-to-input electrode capacitance. It is to be noted that the gate electrode 46 is insulated from the substrate 48 and from the source and drain electrodes 42 and 44 so that there is

substantially no flow of gate current.

Another advantage obtained by having the gate electrode 46 closer to the source electrode 42 is that most of the intrinsic opposition to current flow in the conductive channel 61 (which connects the drain and source electrodes 44 and 42 and which may be described as resistive) is placed in the drain or output circuit of the transistor 40. This increases the gain of the amplifier circuit by overcoming the intrinsic degeneration of the device.

Stated in other terms, the offset gate electrode places more of the channel resistance on the drain side of the gate electrode, thereby reducing the amount of channel resistance effectively in circuit between the gate and source electrodes. By reducing the amount of resistance between the gate and source electrodes (input electrodes), the amount of signal degeneration is reduced. Furthermore, since the series input resistance is reduced, the speed of the circuits is increased permitting higher frequency of operation.

It is to be noted that the circuits shown in FIGURES 5, 6, 7, 8, 9 and 10 include field effect transistors having offset gates and hence all the circuits have the advantage of higher intrinsic gain as a result of having substantially reduced intrinsic degeneration.

Referring now to FIGURE 6, there is shown a signal translating circuit in the form of a tuned amplifier circuit employing a field effect transistor 64 which is similar to the one shown in FIGURES 1 and 2 having gate, source and drain electrodes 66, 68 and 70, respectively.

A tuned output circuit is coupled to the drain electrode 70. The output circuit includes a transformer 72 having a primary winding 74 and a secondary winding 76. One end of the primary winding 74 is directly connected to the drain electrode 70, and the other end thereof is coupled through a fixed capacitor 78 to ground. The source electrode 68 is grounded.

A circuit including a resistor 80 and a feedthrough capacitor 82 is connected to the primary winding 74 to apply a positive bias potential to the drain electrode 70 from a source of direct-current voltage (not shown). The gate electrode 66 is biased to a desired bias potential from a suitable source of bias potential (not shown) through a circuit including a resistor 84 and the feedthrough capacitor 86.

Input signals are applied through the coupling capacitor 88 from a source of input signals (not shown). A capacitor 90 is coupled between the gate electrode 66 and the lower end of the primary winding 74 of transformer 72 to provide neutralization.

The neutralizing network comprises a bridge circuit including the inherent gate-to-drain capacitance, the drain-to-ground capa-

citance, the capacitor 78 and the neutralizing capacitor 90. Because the inherent gate-to-drain capacitance of the transistor 64 is very small due to the offsetting of the gate electrode 66 towards the source electrode 68, the criticality of neutralization is reduced. Thus, the problem of the design and building of a neutralized circuit, which can be easily reproduced, is greatly diminished.

10 Reference is now made to the signal translating circuit in the form of an amplifier circuit schematically shown in FIGURE 7 in which two insulated gate field effect transistors 100 and 102 are connected in parallel.

15 The respective drain electrodes 104 and 106 of transistors 100 and 102 are connected to each other. Also, the respective source electrodes 108 and 110 are connected together.

The gate electrodes 112 and 114 of the respective transistors 100 and 102 are a.c. (alternating current) coupled through a coupling capacitor 116 which is of low impedance at signal frequencies and which isolates the gate electrodes from each other for direct 25 current. The substrates of semiconductor material 111 and 113 of semiconductor devices 100 and 102 have terminals 115 and 117.

Input signals from a source, not shown, 30 are coupled through a coupling capacitor 124 to a tunable input circuit comprising grounded variable capacitors 118 and 120 coupled to each other by an inductor 122 to form a resonant circuit. Input signals developed in the input circuit are coupled to the gate electrode 112 of transistor 100.

A tunable output circuit is coupled to the drain electrodes 104 and 106. The tunable output circuit comprises the variable capacitor 126 and the fixed capacitor 128 which resonate with the inductor 130 at the desired signal frequency.

The output signals from the amplifier circuit are derived from inductor 131 which is 45 inductively coupled to the inductor 130 in the tuned output circuit. The source electrodes 108 and 110 are connected to the negative terminal (—) of a suitable bias source potential *B* (not shown) through a feed-through capacitor 138. The positive 50 terminal of the bias potential source *B* is grounded. Current flows from ground through feedthrough capacitor 134, resistor 132, inductor 130, the drain electrodes 104 55 and 106, the source electrodes 108 and 110 to the negative terminal of the source of bias potential *B*.

Neutralization of the amplifier is obtained by means of a variable capacitor 140, connected between capacitors 120 and 128, in 60 the manner described in reference to the neutralization of the amplifier circuit shown in FIGURE 6.

The gate electrodes 112 and 114 are separately 65 biased to different values of bias

potential from suitable bias potential sources (not shown) through bias circuits including resistors 142 and 146 and feedthrough capacitors 148 and 150, respectively. Resistor 142 and capacitor 148 are coupled to gate 70 electrode 112, and resistor 146 and feedthrough capacitor 150 are coupled to gate electrode 114.

The field effect transistors 100 and 102 each have a sharp cut-off transconductance 75 versus gate voltage characteristic as shown by curve *A* in FIGURE 11. By connecting separately biasing the respective gate electrodes to different bias potentials, a composite remote cut-off transconductance versus gate voltage characteristic is obtained 80 as shown by curve *B* in FIGURE 11. Curves *A* and *B* in FIGURE 11 show the logarithmic change in transconductance (g_m) from a point of maximum value of transconductance at a given gate-to-source bias voltage 85 to other values of transconductance for increasingly negative gate-to-source bias voltage.

The transconductance is defined as the 90 change in drain current divided by the change in input signal voltage at a given gate-to-source bias voltage. Curve *A* of FIGURE 11 shows that the g_m versus gate-to-source bias voltage characteristic has a 95 first portion *a*, which is substantially flat, and a second portion *b* which has a substantially sharp slope. The first portion *a* starts from the point of maximum transconductance and is substantially flat to a point in which the 100 drain current versus drain voltage curves start getting closer to each other.

By connecting two field effect transistors in parallel and by biasing the gate electrodes as previously described, the g_m vs. gate voltage characteristic may be modified to be 105 substantially linear as shown by curve *B* in FIGURE 11. This improves the performance of the unit in that cross-modulation distortion is reduced. It has been found that 110 the circuit described gives better results than an amplifier circuit employing a junction transistor in that cross-modulation distortion is substantially less than in the circuit using the junction transistor. 115

Reference is now made to the signal translating circuit shown in FIGURE 8. There is shown an r-f amplifier stage 136 coupled to a converter stage 141, which is in turn coupled to the first i-f stage 143 of a signal 120 receiver.

The r-f amplifier stage 136 includes an insulated gate field effect transistor 144, similar to the ones shown in FIGURES 1 and 2. The field effect transistor 144 has gate, 125 source and drain electrodes 147, 148 and 149, and a substrate of semiconductor material shown connected to a terminal s_{ss} . The source and drain regions *S* and *D*, shown in FIGURE 2, are doped (N+) and the sub- 130

strate of silicon body is P-type so that a pair of rectifying junctions 152 and 154 are formed between the drain and source regions respectively and the substrate. The substrate side of these diodes operates effectively as the anode.

The drain electrode 149 of transistor 144 is connected through a series circuit including an inductor 156 and a resistor 158 to a B+ terminal which is in turn connected to the positive terminal of a source of bias potential (not shown). The resistor 158 is coupled through a capacitor 160 to ground. The drain electrode 149 is coupled through a coupling capacitor 162 to the converter stage 141.

It is to be understood that the poling of the rectifying junctions 152 and 154 is representative of a transistor of the type described in connection with FIGURES 1 and 2 wherein the substrate is of P-type material relative to the source and drain electrodes. However, the transistor device can be fabricated where the substrate is of N-type material relative to the source and drain electrodes. In devices of the latter type the rectifying junctions would be oppositely poled such that the anode side of the rectifying junction appears at the source and drain electrodes, and the cathode side of these junctions appears at the substrate electrode. The description herein will be restricted to the type of device described in connection with FIGURES 1 and 2 wherein the substrate electrode is of P-type material relative to the source and drain electrodes. This would include materials which were N-type but P-type relative to the more heavily doped (N+) type source and drain.

Input signals are coupled from a signal source (not shown) through a coupling capacitor 166 to the gate electrode 147 of the field effect transistor 144. A variable capacitor 168 is connected between the drain electrode and the gate electrode of the field effect transistor 144 to provide neutralization in the manner described in connection with FIGURES 6 and 7. The source electrode 148 is coupled through a resistor 170 to ground. The source electrode circuit is bypassed to ground for signal frequencies by the bypass capacitor 172 which is connected across the resistor 170. A capacitor 173 couples the terminal S_u to ground. A resistor 174 is coupled between the gate electrode 147 and the source electrode 148 in order to reference the potential of the gate electrode 147 to the potential at the source electrode 148.

The output of the converter stage 141 is coupled by means of a coupling capacitor 176 to the input of the first i-f stage 143. The first i-f stage comprises an insulated gate field effect transistor 178 similar to the field effect transistor 144. The transistor 178 in-

cludes gate, source and drain electrodes 180, 182 and 184, respectively. The drain electrode 184 is connected through an inductor 186 and a resistor 188 to a B+ terminal of a source of bias potential (not shown), which may be the same source of bias potential used to bias the drain electrode 149 of the transistor 144. Resistor 188 is bypassed by a capacitor 200 to ground. Since the terminal 183 is not connected to a source of bias potential the substrate of semiconductor material of the insulated gate field effect transistor 178 is left floating.

The output signals from the first i-f stage 143 are coupled to a utilization circuit (not shown) through a capacitor 212. AGC (automatic gain control) signals which vary as a function of average signal level are applied through a resistor 210 to the gate electrode 180 of the transistor 178. The drain electrode 184 of the transistor 178 is coupled to the terminal S_u of the transistor 144 to apply an AGC voltage to the r-f amplifier stage 136 by a conductor 214 which is connected to the junction between the inductor 186 and the resistor 188.

The AGC signals which are derived from any suitable source, (not shown) become more negative as signal level increases to decrease the source-drain current of the transistor 178, and thereby reduce its gain. The potential of the junction between resistor 188 and inductor 186 becomes more positive as the drain current of the transistor 178 decreases and is applied to the substrate terminal S_u by conductor 214. If desired, an isolating resistor can be connected in series with the conductor 214.

When the potential at the terminal S_u becomes more positive than the potential of the source and drain electrodes 148 and 149, rectifying junctions 154 and 152 are respectively rendered conductive. When the potential at the terminal S_u becomes more positive than the potential at the source electrode 148, the rectifying junction 154 is rendered conductive, thus increasing the current flow through the resistor 170. However, the relative bias voltage between the gate electrode 147 and the source electrode 148 remains the same because the gate electrode is referred to the source electrode through the resistor 174.

When the potential of the terminal S_u becomes more positive than the potential at the drain electrode 149, then the rectifying junction 152 is rendered conductive. The conduction of the rectifying junction 152 effectively connects the drain electrode 149 to ground for signal frequencies through the rectifying junctions 152 and 154 and the capacitor 173 whereby the gain of the r-f amplifier stage is reduced.

FIGURE 9 shows a signal translating circuit in the form of an r-f amplifier stage 136

which is similar to the r-f amplifier stage 136 described in connection with FIGURE 8. The elements in the r-f amplifier stage 136' which are substantially the same as the elements of the r-f amplifier stage 136 of FIGURE 8 are identified by the same numerals. The main difference between the stages 136 and 136' is the biasing of the gate electrodes 147 and 147' respectively. In the r-f amplifier stage 136' the gate electrode 146' is coupled through a resistor 216 to a point of bias potential shown as ground.

As signal level increases, the feedback voltage applied on conductor 214' to the terminal S_u of the field effect transistor 144' becomes more positive. When the potential of terminal S_u of the field effect transistor 144' becomes more positive than the bias potential of the source electrode 148' the rectifying junction 154' is rendered conductive, which in turn increases the amount of current flow through the self biasing resistor 170'. Since the voltage across the resistor 170' appears between the source and gate electrodes, the operating point of the transistor is changed due to the added current from the rectifying junction 154'. When the bias potential between the source and gate electrodes reaches a preselected value the field transistor 144' is rendered substantially non-conductive.

In another embodiment of the invention the gate electrode 147' may be biased at a fixed bias potential other than ground such as to a fixed positive potential relative to ground. In such case, more current through the rectifying junction 154' may be required to cut off the transistor 144'.

Both the r-f amplifier stages 136 and 136' shown in FIGURES 8 and 9 respectively have a built in voltage delay feature in addition to the AGC feature described above. The voltage delay in the circuit shown in FIGURE 8 is the voltage required at the terminal S_u required to overcome the bias voltage at the drain electrode 149 to change the impedance of the rectifying junction 152. In the circuit shown in FIGURE 9, the voltage delay is the required voltage at the S_u terminal to change the impedance of the rectifying junction 154'.

Referring now to FIGURE 10, there is shown a signal translating circuit in the form of a high frequency amplifier circuit comprising a field effect transistor 220 having a gate electrode 222, a source electrode 224, a drain electrode 226, and a substrate of semiconductor material 227. The gate and drain electrodes 222 and 226 are respectively biased through resistors 228 and 230 to desired bias potentials by a source of bias potential (not shown). Input signals are coupled to the gate electrode 222 through a coupling capacitor 232 from a signal source (not shown). The output signals of the am-

plifier circuit are derived across the resistor 230, and a capacitor 234 couples the output signals to an utilization circuit (not shown).

As previously described in reference to FIGURES 1, 2, 8 and 9 the source and drain regions S and D , shown in FIGURE 2, are doped (N^+) and the substrate of silicon body 12 is effectively doped (N) so that a pair of rectifying junctions are formed between the source and drain regions respectively and the substrate. The rectifying junctions 236 and 238, shown in FIGURE 10, are connected to ground.

The source electrode 224 is connected to ground through a resistor 240 in order to provide self bias for the amplifier circuit. The resistor 240 is connected in parallel with a bypass capacitor 244. As the current flows from the drain electrode 226 through the conductive channel 242, the source electrode 224, and the resistor 240 to ground, the potential at the source electrode 224 becomes positive with respect to ground and thus back biases the rectifying junction 236. The capacitance of the rectifying junction 236 is reduced which reduces the total output capacitance of the field effect transistor 220 and hence the high frequency response characteristic of the amplifier is improved.

WHAT WE CLAIM IS:

1. A semiconductor device with a substrate of semiconductive material having a first conductivity, said substrate having two major surfaces, spaced drain and source regions arranged on one of said major surfaces of said substrate defining the ends of a conductive channel in said one major surface, said drain and source regions and said channel being of different resistivity from and/or of opposite conductivity type to said substrate, said drain and source regions effectively forming respective rectifying junctions with said substrate, a gate region being formed of insulating material and extending over at least a portion of said channel in said major surface of said substrate, electrodes respectively arranged on said source, drain and gate regions and adapted to have current flowing in said channel when a difference of potential is applied between said source and drain electrodes with no charge being present from said gate electrode or gate region, and electrical connecting means arranged on said other major surface of said substrate.

2. A signal translating circuit including a semiconductor device as claimed in Claim 1 and including means connecting said gate source and drain electrodes as a signal translating circuit, and means for applying a potential to said substrate to control the efficiency of translation of said circuit.

3. A signal translating circuit including a semiconductor device as claimed in Claim 1, said drain and source regions being of

which is similar to the r-f amplifier stage 136 described in connection with FIGURE 8. The elements in the r-f amplifier stage 136' which are substantially the same as the elements of the r-f amplifier stage 136 of FIGURE 8 are identified by the same numerals. The main difference between the stages 136 and 136' is the biasing of the gate electrodes 147 and 147' respectively.

10 In the r-f amplifier stage 136' the gate electrode 146' is coupled through a resistor 216 to a point of bias potential shown as ground.

As signal level increases, the feedback voltage applied on conductor 214' to the terminal S_u' of the field effect transistor 144' becomes more positive. When the potential of terminal S_u' of the field effect transistor 144' becomes more positive than the bias potential of the source electrode 148' the rectifying junction 154' is rendered conductive, which in turn increases the amount of current flow through the self biasing resistor 170'. Since the voltage across the resistor 170' appears between the source and gate electrodes, the operating point of the transistor is changed due to the added current from the rectifying junction 154'. When the bias potential between the source and gate electrodes reaches a preselected value the field transistor 144' is rendered substantially non-conductive.

In another embodiment of the invention the gate electrode 147' may be biased at a fixed bias potential other than ground such as to a fixed positive potential relative to ground. In such case, more current through the rectifying junction 154' may be required to cut off the transistor 144'.

Both the r-f amplifier stages 136 and 136' shown in FIGURES 8 and 9 respectively have a built in voltage delay feature in addition to the AGC feature described above. The voltage delay in the circuit shown in FIGURE 8 is the voltage required at the terminal S_u required to overcome the bias voltage at the drain electrode 149 to change the impedance of the rectifying junction 152. In the circuit shown in FIGURE 9, the voltage delay is the required voltage at the S_u' terminal to change the impedance of the rectifying junction 154'.

Referring now to FIGURE 10, there is shown a signal translating circuit in the form of a high frequency amplifier circuit comprising a field effect transistor 220 having a gate electrode 222, a source electrode 224, a drain electrode 226, and a substrate of semiconductor material 227. The gate and drain electrodes 222 and 226 are respectively biased through resistors 228 and 230 to desired bias potentials by a source of bias potential (not shown). Input signals are coupled to the gate electrode 222 through a coupling capacitor 232 from a signal source 65 (not shown). The output signals of the am-

plifier circuit are derived across the resistor 230, and a capacitor 234 couples the output signals to an utilization circuit (not shown).

As previously described in reference to FIGURES 1, 2, 8 and 9 the source and drain regions S and D , shown in FIGURE 2, are doped ($N+$) and the substrate of silicon body 12 is effectively doped (N) so that a pair of rectifying junctions are formed between the source and drain regions respectively and the substrate. The rectifying junctions 236 and 238, shown in FIGURE 10, are connected to ground.

The source electrode 224 is connected to ground through a resistor 240 in order to provide self bias for the amplifier circuit. The resistor 240 is connected in parallel with a bypass capacitor 244. As the current flows from the drain electrode 226 through the conductive channel 242, the source electrode 224, and the resistor 240 to ground, the potential at the source electrode 224 becomes positive with respect to ground and thus back biases the rectifying junction 236. The capacitance of the rectifying junction 236 is reduced which reduces the total output capacitance of the field effect transistor 220 and hence the high frequency response characteristic of the amplifier is improved.

WHAT WE CLAIM IS:

1. A semiconductor device with a substrate of semiconductive material having a first conductivity, said substrate having two major surfaces, spaced drain and source regions arranged on one of said major surfaces of said substrate defining the ends of a conductive channel in said one major surface, said drain and source regions and said channel being of different resistivity from and/or of opposite conductivity type to said substrate, said drain and source regions effectively forming respective rectifying junctions with said substrate, a gate region being formed of insulating material and extending over at least a portion of said channel in said major surface of said substrate, electrodes respectively arranged on said source, drain and gate regions and adapted to have current flowing in said channel when a difference of potential is applied between said source and drain electrodes with no charge being present from said gate electrode or gate region, and electrical connecting means arranged on said other major surface of said substrate.

2. A signal translating circuit including a semiconductor device as claimed in Claim 1 and including means connecting said gate source and drain electrodes as a signal translating circuit, and means for applying a potential to said substrate to control the efficiency of translation of said circuit.

3. A signal translating circuit including a semiconductor device as claimed in Claim 1, said drain and source regions being of



negative conductivity type, said gate electrode being disposed between said source and drain regions in a position closer to said source region, said gate electrode being effective to control the current between said source and drain regions, an input circuit being connected between said gate and source electrodes, and an output circuit and a source of unidirectional potential having positive and negative terminals being coupled between said source and drain electrodes with the negative terminal of said unidirectional potential being coupled to said source electrode.

4. A signal translating circuit as claimed in Claim 2, wherein said means for applying said potential to said substrate reduces said efficiency of translation as said potential applied to said substrate is made positive relative to the potential of said source or drain electrodes.

5. A signal translating circuit as claimed in Claim 2 wherein said means for applying said potential to said substrate reduces said efficiency of said translation of said circuit as the potential applied to said substrate forward biases said rectifying junctions between said source and drain regions and said substrate.

6. A signal translating circuit as claimed in Claim 2, each of said source and drain regions being coupled to said substrate of semiconductor material by separate current paths having non-linear impedance characteristics that are a function of the relative potential between said substrate of semiconductor material and said source and drain electrodes, and including circuit means coupled to said gate electrode for applying input signals to be amplified, output circuit means coupled between said drain and source electrodes for deriving amplified output signals, and circuit means coupled to said substrate of semiconductor material for applying a voltage having an amplitude that varies as a function of the average amplitude of said input signals to vary the relative potential between said substrate of semiconductor material and each of said drain and source electrodes whereby the impedance presented by said current paths vary as a function of the amplitude of said input signal and the gain of said translating circuit is reduced when said average amplitude of said input signals increases.

7. A signal translating circuit as claimed in Claim 2 said circuit including a first and a second of said semiconductor devices, each having a gate electrode, a drain electrode and a source electrode, and each having a sharp cut-off transconductance versus bias voltage characteristic, tunable input circuit means coupled to said gate electrode of said first semiconductor device, circuit means for coupling said source electrodes of said first

and second semiconductor devices to each other, means for coupling said drain electrodes of said first and second semiconductor devices to each other so that said semiconductor devices are connected in parallel, capacitive coupling means converted between said gate electrodes of said first and second semiconductor devices, output circuit means coupled to said drain electrodes to derive output signals, and separate biasing means connected to said gate electrodes of said field effect semiconductor devices to bias said gate electrodes to different bias potentials respectively, so that said transconductance versus gate bias voltage characteristics are combined in a composite transconductance versus gate bias voltage characteristic which has remote-cut-off.

8. A signal translating circuit as claimed in Claim 2 said device being an insulated gate field effect semiconductor device, input circuit means are coupled between said gate and source electrodes for applying input signals to said circuit, output circuit means are coupled between said drain and source electrodes to derive translated output signals, and means are coupled to said substrate of semiconductor material for applying a signal voltage which varies as a function of the amplitude of said input signals to said substrate of semiconductor material to control the amplitude of said output signals.

9. A signal translating circuit as claimed in Claim 2 or Claim 8 said source and drain electrodes being coupled to said substrate of semiconductor material, and said voltage applying means being AGC circuit means coupled to said substrate of semiconductor material for applying a variable bias potential to said substrate of semiconductor material whereby when said variable bias potential is positive with respect to the bias potential of said drain and source electrodes, current flows between said substrate and each of said drain and source electrodes, and when said variable bias potential is negative with respect to the bias potential of said source and drain electrodes there is no current flow between each of said source and drain electrodes and said substrate.

10. A signal translating circuit as claimed in Claim 2 said semiconductor device being an insulated gate field effect transistor wherein each of said source and drain electrodes has a respective effect current path with said substrate of semiconductor material which varies as a function of the relative potential between said substrate of semiconductor material and the corresponding one of said source and drain electrodes, and including circuit means coupled to said gate electrode for applying input signals to be amplified, output circuit means coupled between said drain and source electrodes for deriving translated output signals, and circuit



means coupled to said substrate of semiconductor material for varying the relative potential between said substrate of semiconductor material and at least one of said drain and source electrodes.

11. A signal translating circuit as claimed in Claim 2, said gate electrode being disposed between said source and drain electrodes in a manner to control current through said conducting channel, and said gate electrode being offset in a direction closer to the one of said source and drain electrodes to which the negative terminal of said unidirectional source is connected so that the degeneration produced by the resistance of said conducting channel is reduced.

12. A signal translating circuit as claimed in Claim 8 said output circuit means being tunable and neutralizing circuit means being coupled between said output and input circuit means including a variable capacitor for feeding back energy 180° out of phase with the energy fed back through the inherent capacitance between said gate and drain electrodes.

13. A signal translating circuit as claimed in Claim 3 wherein said conductive channel connecting said source and drain electrodes allows current flow from one of said drain and source electrodes to the other of said electrodes in accordance with the polarity of the respective potentials of said electrodes, said gate electrode being effective to control the current flow between said source and drain electrodes, said input circuit being coupled to said gate electrode for applying input signals to said signal translating circuit to vary the flow of current through said conducting channel in accordance with the amplitude of said input signals, whereby conventional current flows from said drain to said source electrode and due to the closer proximity of said control electrode to said source electrode the intrinsic opposition to current flow in said conducting channel is substantially all in said output circuit.

14. A signal translating circuit as claimed in Claim 2 said substrate of semiconductor material being formed from silicon and said gate electrode being insulated from said silicon substrate and located so that the distance between said gate electrode and said drain electrode is longer than the distance between said gate electrode and said source electrode, said conductive channel providing a path for current flow between said pair of electrodes in a direction corresponding to the relative polarity of the potential between said electrodes, and an output circuit including a d.c. voltage source connected between said source and drain electrodes so that said drain electrode is biased positively relative to said source electrode and the signal feed back through the inherent capacitance between said gate electrode and said drain

electrode is reduced because of the offsetting of said gate electrode toward the source electrode.

15. A signal translating circuit as claimed in Claim 2 said substrate being made from nearly intrinsic semiconductor material, and said source and drain electrodes effectively operating as a pair of rectifying junctions connected between said substrate and between said source and drain electrodes, respectively, a resistor being coupled between said source electrode and a point of reference potential, an output circuit including a source of unidirectional potential coupled between said drain electrode and said point of reference potential, means being coupled to said gate electrode for biasing said gate electrode to a desired bias potential with respect to said point of reference potential, and means connecting said substrate of semiconductor material to said point of reference potential so that the rectifying junction effectively connected between said substrate and said source electrode is back-biased whereby the effective capacitance of said rectifying junction is reduced thereby reducing the output capacitance of said field effect semiconductor device and thus increasing the frequency response of said signal translating circuit.

16. A signal translating circuit as claimed in Claim 3 including first and second insulated field effect semiconductor devices each having gate, drain and source electrodes respectively and each having a non-linear log transconductance versus gate bias voltage characteristic, tunable input circuit means coupled to said gate electrode of said first field effect semiconductor device, circuit coupling means for connecting said drain electrodes and said source electrodes of said first and second field effect semiconductor devices to each other respectively, so that said first and second field effect semiconductor devices are connected in parallel, separate bias circuit means for biasing said gate electrodes of said first and second field effect semiconductor devices to different bias potentials respectively, means for coupling said input circuit to said gate electrode of said second field effect semiconductor device whereby said log transconductance versus gate bias voltage characteristics are combined into a composite log transconductance versus gate bias voltage characteristics which is substantially linear, tunable output circuit means coupled to said drain electrodes of said first and second field effect semiconductor devices, and a variable capacitor coupled between said output and input circuits for neutralizing the energy fed back from said output circuit to said input circuit through the inherent capacitance of each of said first and second field effect semiconductor device.

17. A semiconductor device substantially



as herein described and illustrated in Figures 1 and 2 of the accompanying drawings.

18. A signal translating circuit substantially as herein described and illustrated in any 5 of Figures 5 to 10 of the accompanying drawings.

ANDREW CLARK,
Chartered Patent Agents,
5, Stone Buildings,
Lincoln's Inn,
London W.C.2.

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