

BIPOLAR JUNCTION TRANSISTOR WITH VERTICALLY INTEGRATED RESISTOR

BACKGROUND

- [0001] The present invention relates to integrating passive electrical devices with transistors.
5 More specifically, the invention relates to integrating a resistor with a bipolar junction transistor in a vertical structure.
- [0002] A resistor is a well-known electrical component that limits or regulates the flow of electrical current in an electronic circuit. Resistors can be active resistors (e.g. diode-connected transistors) or passive resistors.
- 10 [0003] Compared to active resistors, passive resistors have higher temperature stability, higher linearity (i.e. higher bias stability), and lower noise. Therefore, passive resistors are preferred for applications such as biasing high-gain amplifiers or analog computation units where small variations in bias may significantly drift the output. Integrating passive resistors with transistors is fundamental in many circuit applications.
- 15 [0004] However, a major issue associated with the monolithic integration of passive resistors with transistors in circuitry is the large area these passive resistors use in the circuit floor plan. Since passive resistor resistance values are generally larger or much larger than the ON resistance of transistors, more material and therefore larger circuit surface areas is used by these passive resistors.
- 20 [0005] Bipolar junction transistors (BJTs) have a high drive current at a given operation voltage. This gives BJTs an advantage when used in certain applications like ultra-low-power systems. Further, BJTs are used in many standard circuit building blocks. For example, BJTs are used in common-collector circuits (e.g. analog voltage buffers), common-emitter circuits (e.g. analog voltage amplifiers or digital inverters/NOT gates), and emitter-degenerate circuits (e.g. analog voltage amplifiers or digital inverters).
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- [0006] Accordingly, there is a need to integrate passive resistors with active components like BJTs where the passive resistor uses a minimum of surface area in the circuitry.

SUMMARY

- 5 [0007] According to the present invention, a plurality of embodiments of vertical bipolar junction transistors (VBJTs), each with one or more resistors connected in a circuit, are disclosed. The VBJT and VBJT circuitry has an emitter substructure that includes an emitter layer made from an emitter semiconductor, a collector made of a collector semiconductor, an intrinsic base made of an undoped semiconductor or a moderately doped semiconductor, one or more doped epitaxy regions made of a highly doped semiconductor, and one or more resistors. The intrinsic base, the doped epitaxy region(s), and the resistor(s) are stacked upon one another in a channel in different configurations between the emitter layer and the collector.
- 10 [0008] Various circuit configurations and structures are described including a common-collector circuit, a common-emitter circuit, and an emitter-degenerate circuit. Methods of making these configuration/structures are disclosed.

BRIEF DESCRIPTION OF THE DRAWINGS

- 15 [0009] Various embodiments of the present invention will be described below in more detail, with reference to the accompanying drawings, now briefly described. The Figures show various apparatus, structures, and related method steps of the present invention.
- [0010] Figure 1 is a cross section view of an interim multi-layer stack structure used to form a passive resistor (e.g. resistor) vertically stacked with a bipolar junction transistor (BJT) in a common-collector circuit.
- 20 [0011] Figure 2 is a cross section view of an interim multi-layer stack structure of the initial interim common-collector circuit embodiment of Figure 1, after a trench is etched and a thin oxide layer is formed on dummy layer surfaces exposed to the trench opening.
- [0012] Figure 3 is a cross section view of an interim multi-layer stack structure of the common-collector circuit embodiment after a resistor body and transistor intrinsic base is grown from the emitter layer surface within the trench.
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- [0013] Figure 4 is a cross section view of an interim multi-layer stack structure of the common-collector circuit embodiment after addition of dielectric to a cap dielectric layer, a chemical-mechanical polishing, and deposition of a base mask.
- 5 [0014] Figure 5 is a cross section view of an interim multi-layer stack structure of the common-collector circuit embodiment after removal of a dummy layer.
- [0015] Figure 6 is a cross section view of an interim multi-layer stack structure of the common-collector circuit embodiment after removal of a thin oxide layer and an epitaxial growth of an extrinsic base layer.
- 10 [0016] Figure 7 is a cross section view of an interim multi-layer stack structure of the common-collector circuit embodiment after a base masked etch and deposition of an interlayer dielectric (IDL).
- [0017] Figure 8 is a cross section view of an interim multi-layer stack structure of the common-collector circuit embodiment after removal of the base region hard mask and deposition of a collector mask.
- 15 [0018] Figure 9 is a cross section view of an interim multi-layer stack structure of the common-collector circuit embodiment after a collector masked etch.
- [0019] Figure 10 is a cross section view of an interim multi-layer stack structure of the common-collector circuit embodiment after deposition of a collector.
- [0020] Figure 11 is a cross section view of an interim multi-layer stack structure of the common-collector circuit embodiment after removal of the collector mask.
- 20 [0021] Figure 12 is a cross section view of a common-collector circuit embodiment of a vertical BJT with a stacked vertical resistor including external contacts.
- [0022] Figure 13A is a cross section view of a common-collector circuit embodiment of a vertical BJT with a stacked emitter resistor.

- [0023] Figure 13B is a top view of the common-collector circuit embodiment of the vertical BJT with a stacked emitter resistor shown in Figure 13A.
- [0024] Figure 14 is a circuit diagram of the common-collector circuit embodiment of a vertical BJT with a stacked emitter resistor.
- 5 [0025] Figure 15 is a cross section view of an interim multi-layer stack structure used to form a passive resistor (e.g. resistor) vertically stacked with a bipolar junction transistor (BJT) in a common-emitter circuit.
- [0026] Figure 16 is a cross section view of an interim multi-layer stack structure used to form a passive resistor (e.g. resistor) vertically stacked with a bipolar junction transistor (BJT) in
10 the common-emitter circuit embodiment after formation of intrinsic and extrinsic base and collector resistor.
- [0027] Figure 17 is a cross section view of a common-emitter circuit embodiment of a vertical BJT with a stacked vertical collector resistor including external contacts.
- [0028] Figure 18A is a cross section view of a common-emitter circuit embodiment of a vertical
15 BJT with a stacked collector resistor.
- [0029] Figure 18B is a top view of the common-emitter circuit embodiment of the vertical BJT with a stacked collector resistor shown in Figure 18A.
- [0030] Figure 19 is a circuit diagram of the common-emitter circuit embodiment of a vertical BJT with a stacked collector resistor.
- 20 [0031] Figure 20 is a cross section view of an interim multi-layer stack structure used to form an upper and a lower passive resistor (e.g. resistors) vertically stacked with a bipolar junction transistor (BJT) in an emitter-degenerate circuit.
- [0032] Figure 21 is a cross section view of an interim multi-layer stack structure used to form the two resistors vertically stacked in a channel with a bipolar junction transistor (BJT) in the
25 emitter-degenerate circuit embodiment.

- [0033] Figure 22A is a cross section view of an emitter-degenerate circuit embodiment of a vertical BJT with a stacked first/emitter resistor, R_e , a stacked second/collector resistor, R_c , and external connections.
- [0034] Figure 22B is a top view of an emitter-degenerate circuit embodiment of Figure 22A.
- 5 [0035] Figure 23 is a circuit diagram of the emitter-degenerate circuit embodiment of a vertical BJT with a stacked first/emitter resistor, R_e , and the second/collector resistor, R_c .
- [0036] Figure 24 is a flow chart of a process of making a vertical BJT with one or more stacked resistors.

DETAILED DESCRIPTION

- 10 [0037] It is to be understood that embodiments of the present invention are not limited to the illustrative methods, apparatus, structures, systems and devices disclosed herein but instead are more broadly applicable to other alternative and broader methods, apparatus, structures, systems and devices that become evident to those skilled in the art given this disclosure.
- [0038] In addition, it is to be understood that the various layers, structures, and/or regions shown
15 in the accompanying drawings are not drawn to scale, and that one or more layers, structures, and/or regions of a type commonly used may not be explicitly shown in a given drawing. This does not imply that the layers, structures, and/or regions not explicitly shown are omitted from the actual devices.
- [0039] In addition, certain elements may be left out of a view for the sake of clarity and/or
20 simplicity when explanations are not necessarily focused on such omitted elements. Moreover, the same or similar reference numbers used throughout the drawings are used to denote the same or similar features, elements, or structures, and thus, a detailed explanation of the same or similar features, elements, or structures may not be repeated for each of the drawings.
- 25 [0040] The semiconductor devices, structures, and methods disclosed in accordance with embodiments of the present invention can be employed in applications, hardware, and/or electronic systems. Suitable hardware and systems for implementing embodiments of the

invention may include, but are not limited to, personal computers, communication networks, electronic commerce systems, portable communications devices (e.g., cell and smart phones), solid-state media storage devices, expert and artificial intelligence systems, functional circuitry, neural networks, etc. Systems and hardware incorporating the semiconductor devices and structures are contemplated embodiments of the invention.

[0041] As used herein, “height” refers to a vertical size of an element (e.g., a layer, trench, hole, opening, etc.) in the cross-sectional views measured from a bottom surface to a top surface of the element, and/or measured with respect to a surface on which the element is located.

[0042] Conversely, a “depth” refers to a vertical size of an element (e.g., a layer, trench, hole, opening, etc.) in the cross-sectional views measured from a top surface to a bottom surface of the element. Terms such as “thick”, “thickness”, “thin” or derivatives thereof may be used in place of “height” where indicated.

[0043] As used herein, “lateral,” “lateral side,” “side,” and “lateral surface” refer to a side surface of an element (e.g., a layer, opening, etc.), such as a left or right-side surface in the drawings.

[0044] As used herein, “width” or “length” refers to a size of an element (e.g., a layer, trench, hole, opening, etc.) in the drawings measured from a side surface to an opposite surface of the element. Terms such as “thick”, “thickness”, “thin” or derivatives thereof may be used in place of “width” or “length” where indicated.

[0045] As used herein, terms such as “upper”, “lower”, “right”, “left”, “vertical”, “horizontal”, “top”, “bottom”, and derivatives thereof shall relate to the disclosed structures and methods, as oriented in the drawing figures. For example, as used herein, “vertical” refers to a direction perpendicular to the top surface of the substrate in the views, and “horizontal” refers to a direction parallel to the top surface of the substrate in the views.

[0046] As used herein, unless otherwise specified, terms such as “on”, “overlying”, “atop”, “on top”, “positioned on” or “positioned atop” mean that a first element is present on a second element, wherein intervening elements may be present between the first element and the second element. As used herein, unless otherwise specified, the term “directly” used in connection with the terms “on”, “overlying”, “atop”, “on top”, “positioned on” or

“positioned atop,” “disposed on,” or the terms “in contact” or “direct contact” means that a first element and a second element are connected without any intervening elements, such as, for example, intermediary conducting, insulating or semiconductor layers, present between the first element and the second element.

5 [0047] It is understood that these terms might be affected by the orientation of the device described. For example, while the meaning of these descriptions might change if the device was rotated upside down, the descriptions remain valid because they describe relative relationships between features of the invention.

[0048] Disclosed are structures, devices, and methods for monolithic integration of vertical
10 passive resistors with vertical bipolar junction transistors (VBJT). The invention substantially reduces area consumption of the passive resistors used in this circuitry.

[0049] The resistance value of a passive resistor is given by $R_L = \rho L/A$, where ρ is the resistivity of the material of the passive resistor, L the length of the resistor in the direction of current flow, and A the cross-sectional area of the resistor perpendicular to current flow. The
15 vertical structure of the present invention allows L (i.e. height of the resistor structure) to be arbitrarily large, while A (i.e. the footprint of the resistor/transistor pair) to be small, both large L and small A simultaneously favoring large R .

[0050] When used in large scale circuits, the invention provides huge space savings compared to the planar (i.e. horizontal oriented) resistors used in prior art. In addition, the length of
20 passive resistor can be designed according to resistive needs, e.g. made taller or shorter, without having impact on device footprint. In some embodiments, epitaxial growth of the resistive region enables multiple ways to tune the resistor to the desired resistance, e.g. by controlling dopant species, co-dopants, doping level, and epitaxy thickness and size. Embodiments of the invention include vertically oriented or stacked devices with four
25 terminals.

[0051] Figure 1 is a cross section view of an interim multi-layer stack structure 100 used to form a passive resistor (e.g. resistor) vertically stacked with a bipolar junction transistor (BJT) in a common-collector circuit.

- [0052] The common-collector circuit interim multi-layer stack structure embodiment 100 includes a supporting substrate 103, with a supporting substrate thickness 13; a punch through stop (PTS) layer 104 (doped with a dopant opposite to that of the emitter region layer 105), with a PTS layer thickness 14, disposed on the supporting substrate 103; and a heavily doped emitter region layer 105, with a emitter region layer thickness 15 (in some embodiments connected to ground). The emitter region layer (or emitter layer) 105 is disposed atop the PTS layer 104.
- [0053] The material making the supporting substrate 103 includes one or more semiconductor materials, e.g. bulk semiconductor materials. Non-limiting examples of suitable supporting substrate 103 materials include Si (silicon), strained Si, Si:C (carbon doped silicon), Ge (germanium), SiGe (silicon germanium), SiGe:C (carbon doped silicon-germanium), Si alloys, Ge alloys, III-V semiconductor materials (e.g., GaAs (gallium arsenide), InAs (indium arsenide), InP (indium phosphide), or Indium Gallium Arsenide (InGaAs), or any combination thereof.
- [0054] The supporting substrate 103 has a supporting substrate thickness 13 between 600 and 1000 microns. Other thicknesses 13 are envisioned.
- [0055] The PTS layer 104 can be formed on the upper surface of the supporting substrate 103 by ion implantation or by epitaxial growth in combination with “in situ” doping or ion implantation. The PTS layer 104 thickness 14 can be between 50 nanometers (nm) to 150 nm.
- [0056] The emitter layer 105 is made from a semiconductor material. In some embodiments, the emitter layer 105 is formed epitaxial growth in combination in situ doping. In some embodiments, the emitter layer 105 thickness 15 is between about 10 nm to about 100 nm.
- [0057] In some embodiments, the emitter layer 105 is an epitaxial grown layer made of a silicon material like n-doped silicon. The emitter layer 105 is highly doped with an n-type dopant selected from a group of phosphorus (P), arsenic (As) and antimony (Sb). In a non-limiting example, the dopant concentration ranges between $4 \times 10^{20} \text{ cm}^{-3}$ and $2.5 \times 10^{21} \text{ cm}^{-3}$.

- [0058] Figures 1, 15, and 20 each disclosed an initial interim multi-layer stack structure 100/1500/2000. These related but different stack structures 100/1500/2000 are used to create three respective alternative structures/devices of the invention.
- [0059] In addition, the structures disclosed 100/1500/2000 are based on Group IV semiconductors. Given this disclosure, similar structures can be made with III-V compound semiconductors using known MOCVD growth techniques that are contemplated without loss of generality but not disclosed in detail here.
- [0060] Each of these structures 100/1500/2000 is formed on an emitter substructure 103/104/105, just described, i.e. the supporting substrate 103, the PTS layer 104, and the emitter layer 105. Each of the alternative structures/devices has different ordering and selection of layers disposed on the emitter substructure 103/104/105, as described below. Other embodiments are envisioned.
- [0061] The description of the common-collector circuit embodiments starting with the structure 100 of Figure 1 now continues.
- 15 [0062] Continuing with the description of common-collector circuit interim multi-layer stack structure 100, interim resistor substructure 132A/135A/137A layers are disposed on the emitter substructure. The interim resistor substructure 132A/135A/137A is made of a resistor lower spacer 132A, with a resistor lower spacer thickness 131; a resistor dielectric layer 135A, with a resistor dielectric layer 135A thickness 136; and a resistor upper spacer 137A, with a resistor upper spacer 137A thickness 138.
- 20 [0063] In this embodiment, the resistor lower spacer 132A is disposed on the emitter layer 105, the resistor dielectric layer 135A is disposed on the resistor lower spacer 132A, and the resistor upper spacer 137A is disposed on the resistor dielectric layer 135A.
- [0064] Each of the resistor lower spacer 132A, the resistor dielectric layer 135A, and the resistor upper spacer 137A is made of a dielectric material like an oxide (e.g. SiO_x) or a nitride (e.g., silicon nitride, Si_xN_y) or dielectric oxynitride (e.g. SiOCN, or SiBC). Other dielectric materials employed in semiconductor devices are also envisioned.
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- [0065] In some embodiments, the layers/spacers 132A/135A/137A are made of a silicon nitride or oxynitride deposited by a process like chemical vapor deposition (CVD) or physical vapor deposition (PVD) or plasma enhanced chemical vapor deposition (PECVD).
- [0066] The composition of these dielectric layers 132A/135A/137A can be selected to provide for selective etching between these layers 132A/135A/137A and/or the adjacent and/or other layers in the initial interim multi-layer stack structure 100/1500/2000. (“Selective etching” means that one material is removed by an etching step while another material is selectively and substantially not etched by the same etching step.)
- [0067] The resistor lower spacer 132A thickness 131 and the resistor upper spacer 137A thickness 138 are approximately between 5 nm and 20 nm, with 6 nm to 12 nm a preferred thickness.
- [0068] The resistor dielectric layer 135A thickness 136 depends on the length of the resistor. Accordingly, for the same cross section are of the resistor dielectric layer 135A, the resistance of the resistor can be increased/decreased by increasing/decreasing the length R_L 136 of the resistor as determined by thickness 136 of the resistor dielectric layer 135A.
- In some alternative embodiments, the resistor length R_L 136 is measured as the distance between the center lines (not shown) of the resistor lower spacer 132A and the resistor upper spacer 137A.
- [0069] In this common-collector circuit interim multi-layer stack structure 100 embodiment, a dummy contact layer 140 is deposited on the resistor upper spacer 137A. The dummy contact layer 140 is made of a sacrificial material that is removed selectively from the dummy layer 115, as described below.
- [0070] The dummy contact layer 140 is deposited by known processes like CVD, PVD, PECVD, atomic layer deposition (ALD), metal organic chemical vapor deposition (MOCVD), room temperature chemical vapor deposition (RTCVD), high density plasma chemical vapor deposition (HDPCVD) and combinations thereof.
- [0071] In some embodiments, the dummy contact layer 140 is made of a silicon material like amorphous silicon, α -Si, or amorphous germanium, α -Ge, or amorphous silicon-

germanium, α -SiGe, and has a dummy contact layer thickness 141 approximately between 10 and 60 nm.

- 5 [0072] In this common-collector circuit interim multi-layer stack structure 100 embodiment, a “tri-layer dummy stack” 110/115/120 is deposited on the metal contact layer 140. The tri-layer dummy stack 110/115/120 is made of a base lower spacer 110 (with a base lower spacer 110 thickness 111), a dummy layer 115 (with a dummy layer 115 thickness 116), and a base upper spacer 120 (with a base upper spacer 120 thickness 121).
- 10 [0073] The materials making the base lower spacer 110 and base upper 120 spacer are selectively etchable from the material of the dummy layer 115. For example, the tri-layer dummy stack 110/115/120 can be made by layering the base lower spacer 110 made of silicon nitride (Si_xN_y), then layering the dummy layer 115 made of silicon oxide (SiO_x), then layering the base upper spacer 120 made of silicon nitride (Si_xN_y). In alternative
- 15 embodiments, the order can be changed, for example, the base lower spacer 110 (SiO_x), dummy layer 115 (Si_xN_y), and base upper spacer 120 (SiO_x). The dummy layer 115 is a sacrificial layer that is selectively etchable from the material making the metal contact layer 140.
- 20 [0074] In some embodiments, the resistor lower spacer 132A, the resistor upper spacer 137A, the base lower spacer 110, and base upper 120 spacer are made of the same materials. Non-limiting examples of these materials include low-k materials. Here, the term “low-k” denotes a dielectric material having a dielectric constant equal to the dielectric constant of silicon oxide (SiO_2) or less. Examples of low-k dielectric material suitable for spacers
- 25 include diamond like carbon (DLC), organosilicate glass (OSG), fluorine doped silicon dioxide, carbon doped silicon dioxide, carbon doped silicon nitride, porous silicon dioxide, porous carbon doped silicon dioxide, boron doped silicon nitride (SiBN), carbon boron doped silicon nitride (SiBCN), SiOCN , SiCN , SiOC , spin-on organic polymeric dielectrics (e.g., SILK^{TM}), spin-on silicone based polymeric dielectric (e.g., hydrogen silsesquioxane
- 30 (HSQ) and methylsilsesquioxane (MSQ), and combinations thereof.

- 5 [0075] The base lower spacer 110, dummy layer 115, and base upper layer spacer 120 materials are deposited by known deposition processes, including as non-limiting examples, CVD, PVD, ALD, MOCVD, RTCVD, HDPCVD, plasma enhanced chemical vapor deposition (PECVD), inductively coupled plasma chemical vapor deposition (ICP CVD), or any combination thereof.
- 10 [0076] The base lower spacer 110 thickness 111 and base upper layer spacer 120 thickness 121 are approximately between 5 nanometers (nm) and 20 nm or 6 nm and 12 nm. The dummy layer 115 has a thickness 116 between 50 nm and 300 nm.
- 15 [0077] A cap dielectric layer 24 is formed on the base upper layer spacer 120. The cap dielectric layer 24, as a non-limiting example, is made of an oxide, such as silicon oxide (SiO_x). In some embodiments, the cap dielectric layer 24 is made of a material that can be removed by an etch process selective to the base upper layer spacer 120. The base upper layer spacer 120 protects the sacrificial dummy layer 115 from being etched by the process steps that remove the cap dielectric layer 24. Non-limiting examples of other materials used to make the cap dielectric layer 24 include oxides like tetraethylorthosilicate (TEOS) oxide, high aspect ratio plasma (HARP) oxide, high temperature oxide (HTO), and high-density plasma (HDP) oxide.
- 20 [0078] Figure 2 is a cross section view of an interim multi-layer stack structure 200 of the common-collector circuit embodiment of Figure 1 after a trench is etched to/through the resistor lower spacer 132A and a thin oxide layer 215 is formed on dummy layer 115 surfaces exposed to the trench opening 250.
- 25 [0079] In some embodiments, the trench 250 is etched using a process, e.g. a reactive ion etch (RIE) or a series of RIE steps, that is (are) selective to the layers being etched away by the (series of) etching(s). Etching of trenches 250 is known.
- [0080] The initial etch (or etch steps) etches the trench 250 down to and selective to the resistor lower spacer 132A, i.e. the etching stops at the surface and does not remove (not shown) the portion of the resistor lower spacer 132A within the trench 250.

- [0081] As a non-limiting example illustrating the trench 250 etch, a first etch (selective to the dummy layer 115 material) removes the portion of the cap dielectric layer 24 and base upper layer spacer 120 material within the trench 250, a second etch (selective to the base lower layer spacer 110 material) removes the portion of the dummy layer 115 within the trench 250, a third etch (selective to the resistor upper spacer 137A) removes the portion of the metallic layer 140 within the trench 250, and a forth etch (selective to the resistor lower spacer 132A) removes the portion of the resistor dielectric layer 135A within the trench 250.
- [0082] The surfaces 275 of the trench 250 are then exposed to an oxidation process, e.g. like a plasma oxidation or other known oxidation method. The oxidation step proceeds with parameters (e.g. time, temperature, etc.) to form a thin oxide layer 215 on the surface of the poly crystalline silicon layer 115 that is part of trench 250 surface 275 and a thin oxide layer 240 on the surface of the dummy contact layer 140 that is also part of the trench 250 surface. The thickness of the thin oxide layers 215/240 is between 2 nm and 3 nm. An oxide layer does not form on the surfaces 275 of dielectric layers 135A/137A/110/120/24 or on the resistor lower spacer 132A.
- [0083] After formation of the thin oxide layer 215, the etch continues to remove the portion of the resistor lower spacer 132A within the trench 250 and to expose the emitter layer 105 surface 225 within the trench 250. This etch step is selective to the material in the emitter layer 105, i.e. the etch stops at the exposed emitter layer 105 surface 225.
- [0084] The width of the trench (trench width) 251 can be about 6 nm to about 250 nm, or about 6 nm to about 100 nm.
- [0085] Figure 3 is a cross section view of an interim multi-layer stack structure 300 of the common-collector circuit embodiment after a resistor body 325 and transistor base 350 is grown from the emitter layer surface 225 within the trench 250. This growth is an epitaxial growth done in stages. There is no epitaxial growth from the dielectric surfaces, e.g. the side-wall/surfaces 275 of the trench 250, e.g. 132A/135A/137A/240/110/215/120/24.

- [0086] The terms “epitaxial growth and/or deposition” and “epitaxially formed and/or grown,” mean the growth of a semiconductor material (crystalline material) on a deposition surface of another semiconductor material (crystalline material), e.g. the emitter layer 105, in which the semiconductor material being grown (crystalline over layer) has substantially the same crystalline characteristics as the semiconductor material of the deposition surface (seed material). In an epitaxial deposition process, the chemical reactants provided by the source gases are controlled, and the system parameters are set so that the depositing atoms arrive at the deposition surface of the semiconductor substrate with sufficient energy to move about on the surface such that the depositing atoms orient themselves to the crystal arrangement of the atoms of the deposition surface. Therefore, an epitaxially grown semiconductor material has substantially the same crystalline characteristics as the deposition surface on which the epitaxially grown material is formed. The epitaxial deposition process may employ the deposition chamber of a chemical vapor deposition type apparatus, such as a PECVD apparatus.
- 15 [0087] In some embodiments, the gas source for the deposition of an epitaxially formed in situ doped n-type semiconductor material may include silicon (Si) deposited from silane, disilane, trisilane, tetrasilane, hexachlorodisilane, tetrachlorosilane, dichlorosilane, trichlorosilane, methylsilane, dimethylsilane, ethylsilane, methylidisilane, dimethylidisilane, hexamethylidisilane and combinations thereof. In other examples, when the semiconductor material includes germanium (Ge), a germanium gas source may be selected from the group consisting of germane, digermane, halogermane, dichlorogermane, trichlorogermane, tetrachlorogermane and combinations thereof. The temperature for epitaxial silicon germanium deposition typically ranges from 450°C to 900°C. Although higher temperature typically results in faster deposition, the faster deposition may result in crystal defects and film cracking. An epitaxial silicon germanium alloy layer can be formed utilizing a combination of such gas sources. Carrier gases like hydrogen, nitrogen, or helium can be used.
- [0088] The body 325 of the passive resistor 325 is epitaxially grown in the trench 250 on the emitter layer surface 225. The epitaxial resistor portion 325 can be made of doped silicon,

germanium, or silicon germanium. The doping type is the same as the emitter/collector doping type.

[0089] The dimensions, material composition, dopant species, and dopant concentration of the resistor 325 is selected to provide the resistance properties of the resistor 325 for the design parameters of the circuit. The cross-section area, A , of the resistor 325 is determined by the trench width 251. The resistor length, R_L , 320 of the resistor 325 is determined by the resistor dielectric layer 135A thickness 136 and, in some embodiments, the resistor lower spacer 132A thickness 131 and the resistor upper spacer 137A thickness 138. Additionally, in-situ carbon doping can be used at tool to fine-tune resistivity, independent of the polarity of the resistor structure.

[0090] The cross-section area, A , is perpendicular to the direction of current flow and the resistor length, R_L , 320 is in the direction of current flow. The vertical structure 300 allows the resistor length, R_L , 320 to be arbitrarily large, while A (e.g., the footprint of the resistor/transistor pair) to be small. Both a large L value and a small A value simultaneously favor a large resistance, R . The resistor length, R_L , 320, of the passive resistor 325 can be increased to increase the resistance of the passive resistor 325. The resistor length, R_L , 320, can be a function of the length of time of the epitaxial growth process for forming the passive resistor 325.

[0091] The resistor cross-section area, A , of the resistor 325 affects the resistance of the resistor 325. The cross-section area, A , is a function of the trench width 215, e.g. between 6 nm and 100 nm, and the length of the trench (not shown), e.g. between 20 nm and 100 nm. The resistor length, R_L , 320, is between 10 nm and 200 nm and the resistor 325 is made from the semiconductor materials mentioned above having a with doping type the same as the respective emitter/collector and with a doping concentration between $1 \times 10^{17} \text{ cm}^{-3}$ and $1 \times 10^{19} \text{ cm}^{-3}$. Additionally, in-situ carbon doping can be used at tool to fine-tune resistivity, independent of the polarity of the resistor structure. When carbon doping is used, the carbon doping concentration is between $1 \times 10^{16} \text{ cm}^{-3}$ and $8 \times 10^{20} \text{ cm}^{-3}$.

- [0092] The resistor typically has a resistor length, R_L , 320 extending from the top surface 225 of the emitter layer 105 to the approximate center line (not shown) of the resistor lower spacer 132A. However, the resistor 320 can extend a little below or above the resistor lower spacer 132A in some embodiments. The resistor 325 length, R_L , 320 is also determined by the resistor dielectric layer 135A thickness 136.
- [0093] The resistor 325 has to remain within the lower 132A and upper 137A resistor spacers. In some embodiments, the resistor length, R_L , 320, is between 5 nm and 100 nm and the resistance of the resistor is between 10 Ω (ohms) and 10 M Ω (mega-ohms). The resistor layer 325 is lightly or moderately doped with a doping level in the range of 10^{17} to 10^{19} cm⁻³ in some embodiments.
- [0094] After the resistor 325 has epitaxially grown to the resistor length, R_L , 320 (e.g. where the parameters like time and temperature of growth are typically determined experimentally), the epitaxial growth conditions change to form the first doped epitaxy region 330. The first doped epitaxy region 330 later will serve as part of an external electrical connection to a voltage output produced across the resistor 325.
- [0095] The first doped epitaxy layer 330 is made of a semiconductor material (e.g. silicon, or silicon-germanium) that is high doped with the polarity of doping as the emitter/collector doping type and with a doping concentration of between 4×10^{20} cm⁻³ and 1.5×10^{21} cm⁻³. Accordingly, the first doped epitaxy layer 330 is highly conductive. In some embodiments, the doping concentration of the first doped epitaxy layer 330 is graded, with doping levels in the range of 4×10^{20} cm⁻³ and 1.5×10^{21} cm⁻³ in the vicinity of the first resistive region 1625, and relatively lower doping levels in the range of 10^{19} and 4×10^{20} cm⁻³ in the vicinity of the intrinsic base region 350 (e.g. to reduce bandgap narrowing and Auger recombination within the doped epitaxy layer in the vicinity of the intrinsic base region 350, as known in the art). Similarly, the doping concentration of the second doped epitaxy layer 2130 may be graded, with doping levels in the range of 4×10^{20} cm⁻³ and 1.5×10^{21} cm⁻³ in the vicinity of the second resistive region 2125, and relatively lower doping levels in the range of 10^{19} and 4×10^{20} cm⁻³ in the vicinity of the intrinsic base region 350. (Refer to the description of Figure 21 below.)

- [0096] The first doped epitaxy layer 330 continues to grow to fill the region in the trench 250 approximately between the resistor upper spacer 137A and the base lower layer spacer 110. As a result, the first doped epitaxy layer 330 has a thickness approximately equal to the resistor dielectric layer 135A thickness 136. At this point in the process, the first doped epitaxy layer 330 is in contact with the thin oxide layer 240.
- [0097] After the first doped epitaxy region 330 is grown, the epitaxial gas chemistry is changed in-situ to grow the intrinsic base 350 which continues to grow in the trench 250. The intrinsic base material 350 grows filling the remainder of the trench 250 until the intrinsic base material 350 forms a base cap 355 over the top surface of the cap dielectric layer 24.
- [0098] The intrinsic base 350 is made of a semiconductor material like silicon (Si), silicon-germanium (SiGe), that is lightly or moderately doped with a dopant type opposite to that of the emitter 105, collector 1050, first doped epitaxy 330, second doped epitaxy 2130, first resistive region 1625 and resistive region 2125, and with a doping concentration between 10^{17} and 10^{19} cm⁻³ in some embodiments. (Refer to the description of Figures 16 and 21 below.)
- [0099] For example, in one embodiment where the bipolar junction transistor is an n-p-n transistor, the emitter 105, collector 1050, first doped epitaxy 330, second doped epitaxy 2130, first resistive region 1625 and resistive region 2125, are doped n-type, whereas the intrinsic base 350 and the extrinsic base 650 are doped p-type. In another embodiment where the bipolar junction transistor is a p-n-p transistor, the emitter 105, collector 1050, first doped epitaxy 330, second doped epitaxy 2130, first resistive region 1625 and resistive region 2125, are doped p-type, whereas the intrinsic base 350 and the extrinsic base 650 are doped n-type. In preferred embodiments, the intrinsic base 350 is comprised of a material having a lower bandgap than that of the first and/or second doped epitaxy regions 330 and 2130. For example, the intrinsic base 350 may be comprised of SiGe with a higher Ge content than that of the doped epitaxy regions 330 and 2130. As known in the art, a relatively lower

bandgap is desired for the intrinsic base to improve transistor gain, reduce switching voltage and/or enhance carrier collection.

5 **[0100]** In some embodiments, the intrinsic base material 350 is made of a material that is latticed matched to the emitter layer 105. In some embodiments, the emitter layer 105 is made of silicon (Si), the collector 1050 is made of silicon (Si), (see Figure 10 description), and the intrinsic base material 350 is made of silicon-germanium (SiGe).

10 **[0101]** As disclosed, the dopant and dopant concentration used to create the epitaxial growth of the resistor 325 may be selected to provide the resistive properties of the passive resistor 325 then changed to form the first doped epitaxy region 330, then changed again to form the intrinsic base 350 with the appropriate semiconductor properties. The parameters of the epitaxial growth for each of these regions 325/330/350, e.g. growth time, temperature, etc. is determined by experimentation.

15 **[0102]** The passive resistor 325, first doped epitaxy region 330, and intrinsic base 350 can be epitaxially grown in the trench 250 using the same epitaxial deposition chamber. The epitaxial growth within the trench 250 creates a monolithic structure 325/330/350. Here the term “monolithic” denotes that the passive resistor 325, first doped epitaxy region 330, and intrinsic base material 350 are composed of the same semiconductor material, albeit with different doping levels.

20 **[0103]** Being grown within the trench 250, the resistor 325, the first doped epitaxy region 330, and the intrinsic base 350 are in vertical alignment and therefore the cross-section area, A, is minimized for each device on the surface of the supporting substrate 103.

25 **[0104]** Figure 4 is a cross section view of an interim multi-layer stack structure 400 of the common-collector circuit embodiment after removal of the base cap 355 (e.g. by a chemical-mechanical polishing, CMP), adding more dielectric 424 to the cap dielectric layer 24 (to form a thicker cap dielectric layer), performing another CMP, and depositing a base mask 450.

- [0105] CMP techniques are known. The dielectric 424 added to the top of the cap dielectric layer 24 can be any dielectric. In some embodiments, the dielectric is same dielectric 424 as that of the cap dielectric layer 24 deposited by methods described above.
- 5 [0106] The base mask 450 is a hard mask. The base mask 450 covers the trench 250/intrinsic base 350 and extends over to cover part of the dummy layer 115 around the trench 250/intrinsic base 350.
- 10 [0107] The base mask 450 is made of a protective, dielectric material, e.g. a lithographic protective material, including but not limited to any one of the following materials: silicon nitride (SiN), siliconborocarbonitride (SiBCN), silicon oxycarbonitride (SiOCN), and silicon oxynitride (SiON). The base mask 450 is deposited by standard techniques including CVD, PVD, ALD, and/or other lithographic processes.
- [0108] Figure 5 is a cross section view of an interim multi-layer stack structure of the common-collector circuit embodiment 500 after a directional etch and removal of the dummy layer 115, leaving a voided region 515.
- 15 [0109] The directional etch, e.g. a first base directional etch, uses known chemistries to remove material that is not protected by the base mask 450 to form a narrower cap dielectric layer 524 region below the base mask 450 and to narrow the base upper layer spacer 120. Material in the dummy layer 115 not protected by the base mask 450 may or may not be removed by the base directional etch but the first base direction etch will not proceed past the base lower spacer 110.
- 20 [0110] In some embodiments, a dummy etch is then performed that removes the remaining material in the dummy layer 115 but is selective (does not substantially remove) the cap dielectric layer 524, base upper layer spacer 120, thin oxide layer 215, and base lower spacer 110. The second etch leaves a void 515 in place of the dummy layer 115.
- 25 [0111] The first base directional etch and the dummy etch can be performed in either order.

- [0112] Figure 6 is a cross section view of an interim multi-layer stack structure of the common-collector circuit embodiment 600 after removal of a thin oxide layer 215 and an epitaxial growth of an extrinsic base layer 650.
- [0113] The thin oxide liner 215 can be removed using a dry etch, (e.g. a SiCoNiTM etch), a short hydrofluoric acid (HF) etch, or any other suitable pre-clean process.
- [0114] The extrinsic base layer 650 is epitaxially grown on the intrinsic base 350 and fills the void 515 left by the removal of the dummy layer 115.
- [0115] Due to the shape and access to the void 515 and the epitaxial growth along multiple spacer 110/120 surfaces the epitaxy will be defective, containing dislocations and stacking faults. That will not diminish the function as an extrinsic base material, since typical extrinsic bases of BJT are formed by polycrystalline semiconductor materials. The grown defective epitaxial material will resemble polycrystalline properties, but with much larger grains (areas of perfect epitaxy), accordingly forming a large grain polycrystalline material (LGP) extrinsic base layer 650. Therefore, in some embodiments, the extrinsic base layer 650 is a polycrystalline material 650 that may contain defects such as large grains in the many crystal structure 40, e.g. forming a large grain polycrystalline material (LGP) extrinsic base layer 650.
- [0116] In some embodiments, the extrinsic base 650 is an in situ doped epitaxy. The extrinsic base 650 may have a doping level in the range of 10^{19} and $4 \times 10^{20} \text{ cm}^{-3}$. In preferred embodiments, the extrinsic base 650 is comprised of a material with higher bandgap than that of the intrinsic base 350. For example, when the intrinsic base 350 is comprised of SiGe, the extrinsic base 650 may be comprised of polysilicon. As known in the art, a higher bandgap for the extrinsic base 650 compared to that of the intrinsic base 350 may be beneficial in reducing the base current and therefore improving the transistor gain in some embodiments.
- [0117] Figure 7 is a cross section view of an interim multi-layer stack structure of the common-collector circuit embodiment 700 after a second base directional etch. The second base directional etch removes some of the extrinsic base layer 650 material not protected by the

base mask 450. As a result, the sides of the cap dielectric layer 524, base upper layer spacer 120, and extrinsic base layer 650 are surfaces in the same plane determined by the shape of the base mask 450.

5 [0118] After the second base direction etch, an interlayer dielectric (ILD) 750 material is deposited to fill any remaining spaces in the structure 700. The ILD 750 is made from, for example, a low-k dielectric material (with $k < 4.0$), including but not limited to, silicon oxide, spin-on-glass, a flowable oxide, a high-density plasma oxide, borophosphosilicate glass (BPSG), or any combination thereof. The ILD 750 is deposited by a deposition process, including, but not limited to CVD, PVD, PECVD, ALD, evaporation, chemical solution
10 deposition, or like processes.

[0119] Figure 8 is a cross section view of an interim multi-layer stack structure of the common-collector circuit embodiment 800 after removal of the base mask 450 (and some of the IDL 750 top surface) and deposition of a collector mask 850. The collector mask 850 has a collector mask opening 851 approximately centered over the intrinsic base 350.

15 [0120] The base mask 450 is removed by known techniques like a CMP or a masked etch.

[0121] The collector mask 850 is a hard mask and can be made of the same materials and deposited by the methods as the base mask 450.

[0122] Figure 9 is a cross section view of an interim multi-layer stack structure of the common-collector circuit embodiment 900 after a collector masked etch.

20 [0123] The collector masked etch creates a collector cavity 925 by removing material from the cap dielectric layer 524 and part of the intrinsic base 350 in a region not protected by the collector mask 850. A shorter intrinsic base 950 results with a base top surface 951 exposed to the collector cavity 925. The collector masked etch is selective to the base upper layer spacer 120.

25 [0124] Figure 10 is a cross section view of an interim multi-layer stack structure of the common-collector circuit embodiment 1000 after deposition of a collector 1050.

- [0125] The collector 1050 is epitaxially grown, to fill the collector cavity 925 and contacts the base top surface 951 of the intrinsic base 950. The collector 1050 can be made of any known collector material compatible with the intrinsic base 950 and is deposited by known techniques like those described above, e.g. CVD and PVD.
- 5 [0126] In some embodiments, the collector 1050 is made from a doped silicon doped with a dopant type of the same as the emitter layer 105 and a dopant concentration of between $4 \times 10^{20} \text{ cm}^{-3}$ and $2.5 \times 10^{21} \text{ cm}^{-3}$.
- [0127] Figure 11 is a cross section view of an interim multi-layer stack structure of the common-collector circuit embodiment 1100 after removal of the collector mask 850 by known
10 methods like a CMP or a masked etch.
- [0128] Figure 12 is a cross section view of a common-collector circuit embodiment of a vertical BJT with a stacked vertical resistor 1200 including external contacts 1225/1250/1275.
- [0129] The external contacts 1225/1250/1275 are made with known methods. Non-limiting methods of forming external contacts 1225/1250/1275 include forming a via, e.g. with a
15 laser, patterning one or more trenches with a masked etch, etc.
- [0130] The dummy contact layer 140 and the thin oxide layer 240 are removed and replaced with a metal contact layer 340.
- [0131] In some embodiments, the dummy contact layer 140 is removed from between the resistor upper spacer 137A and the base lower layer spacer 110 by a wet etch using hot ammonia.
20 The etching material contacts the dummy contact layer 140 through one or more drilled holes and/or by lateral access. The wet etch removes the dummy contact layer 140 selectively while leaving resistor upper spacer 137A, the base lower layer spacer 110, and the thin oxide layer 240 substantially intact. The thin oxide liner 240 is then removed using a dry etch, (e.g. a $\text{SiCoNi}^{\text{TM}}$ etch), a short hydrofluoric acid (HF) etch, or any other suitable pre-clean process. A $\text{SiCoNi}^{\text{TM}}$ etch is a plasma-assisted dry etch process that involves
25 simultaneous exposure of a substrate to hydrogen, NF_3 and NH_3 plasma by-products.

- [0132] Accordingly, a cavity is formed, bordered by the resistor upper spacer 137A, the base lower layer spacer 110, and the first doped epitaxy region 330. After a silicide, typically 1240, is formed on the first doped epitaxy region 330, the cavity left by the dummy contact layer 140 removal is filled with a metal to create the metal contact layer 340. Non-limiting examples of metals making the metal contact layer 340 are cobalt (Co), or tungsten (W), and other metals like nickel (Ni), platinum (Pt), titanium (Ti), and molybdenum (Mo) which are deposited by known deposition techniques like CVD, PVD, ALD, etc. The metal contact layer 340 is in direct contact with the silicide layer 1240 which is in direct contact with the surface of the first doped epitaxy region 330.
- 10 [0133] The vias/trenches are long enough to electrically connect to the respective internal contact of the device 1200 to external circuitry. Removal of material from the cap dielectric layer 524, base upper layer spacer 120, collector 1050, extrinsic base layer 650, base lower spacer 110, and/or metal contact layer 340 creates the respective via/trench.
- 15 [0134] The base contact 1225 passes through the cap dielectric layer 524 and base upper layer spacer 120 to contact the extrinsic base layer 650 and base 950. The collector contact 1250 directly contacts the collector 1050. The output contact 1275 contacts the metal contact layer 340. Note that an insulating layer 1280 is first deposited in via containing the output contact 1275 to prevent the output contact 1275 from electrical shorting to the extrinsic base layer 650.
- 20 [0135] The vias/trenches are filled with a conductive material, e.g., a metal, or a combination of conductive materials. Non-limiting examples of conductive material are a conductive metal, aluminum (Al), platinum (Pt), gold (Au), tungsten (W), titanium (Ti), cobalt (Co) or any combination thereof. The conductive material may be deposited by a suitable deposition process, for example, CVD, PECVD, PVD, plating, thermal or e-beam evaporation, or sputtering.
- 25 [0136] Figure 13A is a cross section view of a common-collector circuit embodiment 1300 of a vertical BJT with a stacked emitter resistor 325. The contacts 1225/1250/1275 are made as described above.

- [0137] Figure 13B is a top view of the common-collector circuit embodiment 1350 of the vertical BJT with a stacked emitter resistor 1300 shown in Figure 13A. In some embodiments, the collector contact 1250 can be a single contact or a plurality of contacts 1250, as shown. In some embodiments, the base contacts 1225 are multiple contacts 1225 on one side of the structure 1300/1350 and the output contacts 1275 are multiple contacts 1275 on another side of the structure 1300/1350, as shown. In some embodiments, the emitter contacts 1305 are multiple contacts in the front and/or the back of the structure 1300/1350 as shown in the top view 1350 but not visible in the cross-section view 1300.
- [0138] Figure 14 is a circuit diagram of the common-collector circuit embodiment of a vertical BJT with a stacked emitter resistor 1400.
- [0139] The circuit input, V_{in} , is the external base connection 1225 and the circuit output, V_{out} , is external connection 1275. In this circuit, the external emitter connection 1305 is connected to ground (or alternatively, to the emitter supply voltage V_{ss}). The external collector connection 1250 is connected to the collector supply voltage V_{dd} .
- [0140] Figure 15 is a cross section view of an interim multi-layer stack structure used to form a resistor (e.g. resistor) vertically stacked with a bipolar junction transistor (BJT) in a common-emitter circuit embodiment 1500.
- [0141] The layers in the common-emitter embodiment of the interim multi-layer stack structure 1500 are the same as those in the common-collector embodiment 100, however the order is different. As with the common-collector embodiment 100, there is an emitter substructure 103/104/105. However, in the common-emitter embodiment 1500, the “tri-layer dummy stack” 110/115/120 is deposited on the emitter substructure first. The dummy contact layer 140 is deposited on the tri-layer dummy stack, e.g. on the base upper spacer 120. The interim resistor substructure 132B/135B/137B is deposited on the dummy contact layer 140. The cap dielectric layer 24 is deposited on the interim resistor substructure 132B/135B/137B, e.g. on and the resistor upper spacer 137B. See the description of Figure 1 for the material composition, thicknesses, and methods of deposition of these layers.

- [0142] Figure 16 is a cross section view of an interim multi-layer stack structure used to form a passive resistor (e.g. resistor) vertically stacked with a bipolar junction transistor (BJT) in the common-emitter circuit embodiment 1600 after formation of intrinsic 350 and extrinsic base and resistor 1625.
- 5 [0143] This structure 1600 is formed by performing the steps of etching the trench 250 and oxidizing the thin oxide layers 215/240. The trench/opening 250 is then filled by an epitaxial growth in the following epitaxial deposition time-controlled formation order: intrinsic base 350, first doped epitaxy region 330, and collector resistor 1625. The base mask 450 is deposited.
- 10 [0144] A directional etch is performed, e.g. a first base/collector directional etch, using known chemistries to remove material that is not protected by the base mask 450. The first base/collector direction etch removes material down/selective to the base lower spacer 110.
- [0145] In some embodiments, a dummy etch is then performed that removes the remaining material in the dummy layer 115 but is selective (does not substantially remove) the cap dielectric layer 524, base upper layer spacer 120, thin oxide layer 215, and base lower spacer 110. The second etch leaves a void in place of the dummy layer 115. The thin oxide layer 215 is removed.
- 15 [0146] The extrinsic base layer 650 is epitaxially grown on the intrinsic base 350 and fills the void left by the removal of the dummy layer 115. The ILD 750 is deposited.
- 20 [0147] See the description of Figures 2 - 7 for more detail about the materials used and process steps performed to create structure 1600.
- [0148] Figure 17 is a cross section view of a common-emitter circuit embodiment of a vertical BJT with a stacked vertical collector resistor 1700 including external contacts.
- [0149] Starting with the structure 1600, the base mask 450 is removed and collector mask 850 is deposited. The collector cavity 925 is formed and the collector 1050 is epitaxially grown. The collector mask 850 is then removed. The dummy contact layer 1640B is removed and the silicide, typically 1740, is formed. The metal contact layer 1740B replaces the void left
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by the removed dummy contact layer 1640B and the external contacts 1725/1750/1775/1805 are formed.

- 5 [0150] The base contact 1725 passes through the cap dielectric layer 524, the resistor upper spacer 137A, the resistor dielectric layer 135B, the resistor lower spacer 132B, the metal contact layer 1740B, and the base upper layer spacer 120 to contact the extrinsic base layer 650 and base 350. Note that an insulating layer 1730 is first deposited in via/trench containing the base contact 1725 to prevent the base contact 1725 from electrical shorting to the metal contact layer 1740B.
- 10 [0151] The collector contact 1750 directly contacts the collector 1050. The output contact 1775 contacts the metal contact layer 1740B.
- [0152] See the description of Figures 8 – 12 for more detail about the materials used and process steps.
- [0153] Figure 18A is a cross section view of a common-emitter circuit embodiment of a vertical BJT with a stacked collector resistor 1800.
- 15 [0154] The contacts 1725/1750/1775 are made as described above.
- [0155] Figure 18B is a top view of the common-emitter circuit embodiment of the vertical BJT with a stacked emitter resistor 1850 shown in Figure 18A.
- 20 [0156] In some embodiments, the collector contact 1750 can be a single contact or a plurality of contacts 1750, as shown. In some embodiments, the base contacts 1725 are multiple contacts 1725 on one side of the structure 1800/1850 and the output contacts 1775 are multiple contacts 1775 on another side of the structure 1800/1850, as shown. In some embodiments, the emitter contacts 1805 are multiple contacts in the front and/or the back of the structure 1800/1850 as shown in the top view 1850 but not visible in the cross-section view 1800 and connect to emitter layer 105.
- 25 [0157] Figure 19 is a circuit diagram of the common-emitter circuit embodiment of a vertical BJT with a stacked collector resistor 1900.

- [0158] The circuit input, V_{in} , is the external base connection 1725 and the circuit output, V_{out} , is external connection 1775. In this circuit, the external emitter connection 1805 is connected to ground (or alternatively, to the emitter supply voltage such as V_{ss}). The collector resistor, R_c , 1625 is connected 1750 to the collector supply voltage V_{dd} .
- 5 [0159] Figure 20 is a cross section view of an interim multi-layer stack structure 2000 used to form an upper/collector and a lower/emitter resistors vertically stacked with a bipolar junction transistor (BJT) in a emitter-degenerate circuit embodiment. Adding an emitter degeneracy to a common-emitter circuit (i.e. adding R_E) reduces the voltage gain but increases the linearity and stability of the circuit.
- 10 [0160] The layers in the emitter-degenerate embodiment of the interim multi-layer stack structure 2000 are the same as those in the common-emitter embodiment 1500, however, a first/emitter resistor lower spacer 2032 and a first/emitter resistor dielectric layer 2035 are inserted between the emitter layer 105 and the tri-layer dummy stack 110/115/120. The first/emitter resistor lower spacer 2032 is disposed on emitter layer 105 and the first/emitter resistor dielectric layer 2035 is disposed on the first/emitter resistor layer spacer 2032. The first/emitter resistor dielectric layer 2035 will become the emitter resistor R_E .
- 15 [0161] The “tri-layer dummy stack” 110/115/120 is deposited on the first resistor dielectric layer 2035. The dummy contact layer 140 is deposited on the tri-layer dummy stack, e.g. on base upper spacer 120. The interim resistor substructure 132B/135B/137B is deposited on the dummy contact layer 140. The cap dielectric layer 24 is deposited on the interim resistor substructure 132B/135B/137B, e.g. on and the resistor upper spacer 137B. See the description of Figure 1 for the material composition, thicknesses, and methods of deposition of these layers.
- 20 [0162] Figure 21 is a cross section view of an interim multi-layer stack structure used to form the two resistors vertically stacked with a bipolar junction transistor (BJT) in the emitter-degenerate circuit embodiment 2100 after formation of intrinsic 350 and extrinsic base 650 and first/emitter resistor, R_E , 2125 and the second/collector resistor, R_c 1625.
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- [0163] This structure 2100 is formed by performing the steps of etching the trench 250 down to the base lower spacer 110 and oxidizing the thin oxide layers 215/240. The trench 250 etch then continues until the emitter layer 105 is reached.
- 5 [0164] The trench 250 is then filled with an epitaxial growth in the following formation order: first/emitter resistor, Re, 2125, bottom doped epitaxy region 2130, intrinsic base 350, top doped epitaxy region 330, and second/collector resistor 1625. The base mask 450 is deposited.
- 10 [0165] A directional etch is performed, e.g. a first base/collector directional etch, using known chemistries to remove material that is not protected by the base mask 450. The first base/collector direction etch removes material down/selective to the base lower spacer 110.
- 15 [0166] In some embodiments, a dummy etch is then performed that removes the remaining material in the dummy layer 115 but is selective (does not substantially remove) the cap dielectric layer 524, base upper layer spacer 120, thin oxide layer 215, and base lower spacer 110. The second etch leaves a void in place of the dummy layer 115. The thin oxide layer 215 is removed.
- [0167] The extrinsic base layer 650 is epitaxially grown on the intrinsic base 350 and fills the void left by the removal of the dummy layer 115. The ILD 750 is deposited.
- [0168] See the description of Figure 2 - 7 for more detail about the materials used and process steps performed to create structure 2100.
- 20 [0169] In some embodiments, the materials and methods are the same for the first/emitter resistor, Re, 2125, and the second/collector resistor 1625. In addition, the materials and methods are the same for the bottom doped epitaxy region 2130 and the top doped epitaxy region 330. No silicide contacts need to be form on the bottom doped epitaxy region 2130.
- 25 [0170] Figure 22A is a cross section view of a emitter-degenerate circuit embodiment 2200 of a vertical BJT with a stacked first/emitter resistor, Re, 2125 and the second/collector resistor, Rc 1625 completed and with the external connections 1730/1750/1775/1805, metal contact layer 1740B, and silicide 1740 included.

- 5 [0171] Starting with the structure 2100, the base mask 450 is removed and collector mask 850 is deposited. The collector cavity 925 is formed and the collector 1050 is deposited. The collector mask 850 is then removed, the dummy contact layer 1640B is removed, and the silicide, typically 1740, is formed. The metal contact layer 1740B fills the void left by the dummy contact layer 1640B removal and the external contacts 1725/1750/1775/1805 are completed.
- 10 [0172] The base contact 1725 passes through the cap dielectric layer 524, the resistor upper spacer 137A, the resistor dielectric layer 135B, the resistor lower spacer 132B, the metal contact layer 1740B, and the base upper layer spacer 120 to contact the extrinsic base layer 650 and base 350. Note that an insulating layer 1730 is first deposited in via/trench containing the base contact 1725 to prevent the base contact 1725 from electrical shorting to the metal contact layer 1740B.
- [0173] The collector contact 1750 directly contacts the collector 1050. The output contact 1775 contacts the metal contact layer 1740B.
- 15 [0174] See the description of Figures 8 – 12 for more detail about the materials used and the method steps performed.
- [0175] Figure 22B is a top view of the common-emitter circuit embodiment of the vertical BJT with a with a stacked first/emitter resistor, R_e , 2125 and the second/collector resistor, R_c 1625.
- 20 [0176] In some embodiments, the collector contact 1750 can be a single contact or a plurality of contacts 1750, as shown. In some embodiments, the base contacts 1725 are multiple contacts 1725 on one side of the structure 2200/2250 and the output contacts 1775 are multiple contacts 1775 on another side of the structure 2200/2250, as shown. In some embodiments, the emitter contacts 1805 are multiple contacts in the front and/or the back of the structure 2200/2250 that connect to emitter layer 105, as shown in the top view 2250 but not visible in the cross-section view 2200.
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- [0177] Figure 23 is a circuit diagram 2300 of the emitter-degenerate circuit embodiment 2200 of a vertical BJT with a stacked first/emitter resistor, R_e , 2125 and the second/collector resistor, R_c 1625.
- [0178] The circuit input, V_{in} , is the external base connection 1725 and the circuit output, V_{out} , is external connection 1775. In this circuit, the external emitter connection 1805 is connected to ground (or to the emitter supply voltage V_{ss}). The collector resistor, R_c , 1625 is connected 1750 to the collector supply voltage V_{dd} .
- [0179] Figure 24 is a flow chart of a process 2400 of making a vertical BJT with one or more stacked resistors.
- 10 [0180] The process begins with step 2405 by creating an interim multi-layer stack 100/1500/2000 depending on the respective circuit embodiments that are being made, e.g. common-collector, a common-emitter, or an emitter-degenerate circuit. See the descriptions in Figures 1, 15, and 20.
- [0181] In step 2410, the trench 250 is etched and epitaxial growth of the layers in the trench forms the first/emitter resistor, R_e , 2125, bottom doped epitaxy region 2130, intrinsic base 350, top doped epitaxy region 330, and/or the second/collector resistor 1625. See the respective descriptions of Figures 2 -3, 16, and 21.
- 15 [0182] In step 2515, dummy material is removed and replaced. For example, the dummy contact layer 140 is removed and replaced with metal contact layer 340/1740B and the dummy layer 115 is removed and replaced with the extrinsic base layer 650. See description of Figures 3A through 7, 16, 21, and 22A.
- 20 [0183] In step 2420 the extrinsic base 640 is grown and the collector 1050 is deposited. See the description in Figures 7 – 11, 17, and 22A.
- [0184] In step 2425, the external contacts are formed. See descriptions of Figures 12, 13A, 13B, 17, 18A, 18B, 22A, and 22B.
- 25 [0185] The descriptions of the various embodiments of the present invention have been presented for purposes of illustration but are not intended to be exhaustive or limited to the

embodiments disclosed. Many modifications and variations will be apparent to those of ordinary skill in the art without departing from the scope of the described embodiments. For example, the semiconductor devices, structures, and methods disclosed in accordance with embodiments of the present invention can be employed in applications, hardware, and/or electronic systems. Suitable hardware and systems for implementing embodiments of the invention may include, but are not limited to, personal computers, communication networks, electronic commerce systems, portable communications devices (e.g., cell and smart phones), solid-state media storage devices, expert and artificial intelligence systems, functional circuitry, etc. Systems and hardware incorporating the semiconductor devices are contemplated embodiments of the invention.

[0186] The terminology used herein was chosen to explain the principles of the embodiments and the practical application or technical improvement over technologies found in the marketplace or to otherwise enable others of ordinary skill in the art to understand the embodiments disclosed herein. Devices, components, elements, features, apparatus, systems, structures, techniques, and methods described with different terminology that perform substantially the same function, work in the substantial the same way, have substantially the same use, and/or perform the similar steps are contemplated as embodiments of this invention.

CLAIMS

We claim:

1. A vertical bipolar junction transistor (VBJT) comprising:
 - an emitter substructure, the emitter substructure having an emitter layer made from an emitter semiconductor;
 - a collector made of a collector semiconductor;
 - an intrinsic base, the intrinsic base made of one of a lightly doped or moderately doped semiconductor;
 - one or more doped epitaxy regions made of a highly doped semiconductor; and
 - one or more resistors,wherein the intrinsic base, the doped epitaxy region, and the resistors are stacked upon one another in a channel between the emitter layer and the collector.
2. The VBJT, as in Claim 1, where doped epitaxy regions have a doping concentration of between $4 \times 10^{20} \text{ cm}^{-3}$ and 2.5×10^{21} .
3. The VBJT, as in Claim 1, where the emitter semiconductor is doped with an n-type dopant with an emitter dopant concentration between $4 \times 10^{20} \text{ cm}^{-3}$ and $2.5 \times 10^{21} \text{ cm}^{-3}$.
4. The VBJT, as in Claim 1, where an extrinsic base made of an extrinsic base semiconductor and surrounds the intrinsic base.
5. The VBJT, as in Claim 1, further comprising one or more metal contact layers each metal contact layer encompassing one or more of the doped epitaxy regions and one or more of the metal contact layers being connected to an external connection.
6. The VBJT, as in Claim 1, where a resistor dielectric thickness of the resistor determines a resistor length of the respective resistor.
7. The VBJT, as in Claim 6, where the resistor length is between 5 nanometers (nm) and 100 nm.

8. The VBJT, as in Claim 1, where the resistor has resistor dopant with a resistor dopant concentration between $1 \times 10^{17} \text{ cm}^{-3}$ and $1 \times 10^{19} \text{ cm}^{-3}$ and is made of one of the following materials: a type IV semiconductor, silicon, germanium, silicon-germanium, and a type III semiconductor.

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9. The VBJT, as in Claim 8, where resistor dopant type is the same dopant type used in the emitter layer and collector.

10. The VBJT, as in Claim 8, where the resistor has a carbon doping in addition.

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11. The VBJT, as in Claim 9, where the carbon doping has a carbon doping concentration between 1×10^{17} and $8 \times 10^{20} \text{ cm}^{-3}$.

12. The VBJT, as in Claim 1, where the doped epitaxy region is bottom doped epitaxy region and the resistor is a emitter resistor and the emitter resistor is disposed on the emitter layer, the emitter bottom doped epitaxy region is disposed on the emitter resistor, and the intrinsic base is disposed on the emitter resistor to form a common-collector VBJT circuit.

13. The VBJT, as in Claim 1, where the doped epitaxy region is a top doped epitaxy region and the resistor is a collector resistor and the intrinsic base is disposed on the emitter layer, the top doped epitaxy region is disposed on the intrinsic base, and the collector resistor is disposed on the top doped epitaxy region to form a common-emitter VBJT circuit.

14. The VBJT, as in Claim 1, where the one or more doped epitaxy regions comprise a bottom doped epitaxy region and a top doped epitaxy region and the one or more resistor that comprise an emitter resistor and a collector resistor and the emitter resistor disposed on the emitter layer, the bottom doped epitaxy region is disposed on the emitter resistor dielectric, the intrinsic base is disposed on the bottom doped epitaxy region, the top doped epitaxy region is disposed on the intrinsic base, and the collector resistor is disposed on the top doped epitaxy region to form a emitter-degenerate circuit VBJT circuit.

15. A vertical bipolar junction transistor (VBJT) emitter-degenerate circuit comprising:
- an emitter substructure, the emitter substructure having an emitter layer made from an emitter semiconductor;
 - an emitter resistor disposed on the emitter layer;
 - 5 a bottom doped epitaxy region disposed on the emitter resistor;
 - an intrinsic base disposed on the bottom doped epitaxy region, the intrinsic base made of one of an undoped semiconductor or a lightly doped semiconductor;
 - a top doped epitaxy region disposed on the intrinsic base
 - a collector resistor disposed on the top doped epitaxy region; and
 - 10 a collector made of a collector semiconductor, disposed on the collector resistor,
- wherein the emitter resistor, the bottom doped epitaxy region, the intrinsic base, the top doped epitaxy region, and the collector resistor are stacked in a channel between the emitter layer and the collector.
- 15 16. The VBJT emitter-degenerate circuit, as in Claim 15, wherein the emitter resistor, the bottom doped epitaxy region, the top doped epitaxy region, the collector resistor, and the collector are all doped with the same dopant type.
17. A method of making a vertical bipolar junction transistor (VBJT) circuit comprising the steps of:
- 20 creating an interim multi-layer stack by creating an emitter substructure, the emitter substructure having an emitter layer and depositing on the emitter layer the following layers: one or more interim resistor substructures, a dummy contact layer, and a tri-layer dummy stack;
 - etching a trench in the interim multi-layer stack;
 - 25 epitaxially growing in the channel the following:
 - one or more resistors, each resistor surrounded by a resistor dielectric layer of one of the respective interim resistor substructures;
 - a doped epitaxy region surrounded by the dummy contact layer; and
 - an intrinsic base surrounded by a dummy layer in the tri-layer dummy stack;
 - 30 removing the dummy contact layer and replacing the dummy contact layer by depositing a metal contact layer;

removing the dummy layer and replacing the dummy layer with an epitaxially grown an extrinsic base layer; and

depositing a collector on the intrinsic base.

- 5 18. The method, as in Claim 17, where the layers deposited on the emitter layer in the following order:

the interim resistor substructure, being an emitter resistor substructure;

the dummy contact layer; and

the tri-layer dummy stack.

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19. The method, as in Claim 17, where the layers deposited on the emitter layer in the following order:

the tri-layer dummy stack;

the dummy contact layer; and

- 15 the interim resistor substructure, being a collector resistor substructure.

20. The method, as in Claim 17, where the layers deposited on the emitter layer in the following order:

one of the interim resistor substructures, being a first, emitter resistor substructure;

- 20 the tri-layer dummy stack;

the dummy contact layer; and

one of the interim resistor substructures, being a second, collector resistor substructure.