METHOD FOR PLANARIZED SELF-ALIGNED FLOATING GATE TO ISOLATION

ABSTRACT

A method for forming floating gate regions in non-volatile memory cells (10) each having a floating gate (26) and a control gate is disclosed. First, a plurality of isolation structures (20) in a substrate (22) extending above and below a surface of the substrate (22) is formed. Second, a floating gate layer (26) on the substrate over and between at least a portion of the isolation structures (20) is formed. Finally, the floating gate layer (26) is planarized down to the isolation structures (20) for forming a plurality of the floating gate regions (26) isolated by the isolation structures.

Fig.1

This Sheet Has Been Replaced



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