SOLID STATE LIGHTING DEVICES AND ASSOCIATED METHODS OF MANUFACTURING

TECHNICAL FIELD

[0001] The present technology is directed generally to solid state lighting (SSL) devices and associated methods of manufacturing.

BACKGROUND

[0002] SSL devices generally use semiconductor light emitting diodes (LEDs), organic light-emitting diodes (OLED), and/or polymer light-emitting diodes (PLED) as sources of illumination rather than electrical filaments, a plasma, or a gas. Figure 1A is a cross-sectional diagram of a portion of a conventional indium-gallium nitride (InGaN) LED 10. As shown in Figure 1A, the LED 10 includes a silicon substrate 12, an N-type gallium nitride (GaN) material 14, an InGaN material 16 (and/or InGaN/GaN multiple quantum wells), and a P-type GaN material 18 on one another in series. The LED 10 also includes a first contact 20 on the P-type GaN material 18 and a second contact 22 on the N-type GaN material 14.

[0003] One drawback of the LED 10 in Figure 1A is that the thermal expansion coefficients (TECs) between GaN/InGaN materials 14, 16, and 18 and the silicon substrate 12 are different and may cause the LED 10 to bow and/or otherwise flex under thermal stress. Such bowing or flexing can cause the GaN/InGaN materials 14, 16, and 18 of the LED 10 to crack and/or have other structural defects.

[0004] Another drawback of the LED 10 is that the silicon substrate 12 typically includes silicon wafers with a Si(1,1,1) lattice orientation instead of those with a Si(1,0,0) lattice orientation. Figure 1B is a schematic perspective view of a portion of a silicon lattice illustrating both the Si(1,1,1) and Si(1,0,0) lattice orientations. It is believed that the epitaxial growth of the GaN/InGaN materials 14, 16, and 18 prefers a hexagonal lattice structure provided by the Si(1,1,1) wafers. However, Si(1,1,1) wafers are more expensive than commonly available Si(1,0,0) wafers. Accordingly, several improvements in reliably and cost-effectively manufacturing LEDs may be desirable.

BRIEF DESCRIPTION OF THE DRAWINGS

[0005] Figure 1A is a cross-sectional view of a portion of an LED in accordance with the prior art.

[0006] Figure 1B is a schematic perspective view of a portion of a silicon lattice illustrating Si(1,1,1) and Si(1,0,0) lattice orientations.

[0007] Figures 2A-2C are cross-sectional views of a portion of a microelectronic substrate undergoing a process of surface modification in accordance with embodiments of the technology.

[0008] Figures 3A-3C are cross-sectional views of a portion of a microelectronic substrate undergoing a process of forming non-planar LED structures in accordance with embodiments of the technology.

[0009] Figures 4A-4C are cross-sectional views of a portion of a microelectronic substrate undergoing a process of forming partially planar LED structures in accordance with embodiments of the technology.

[0010] Figures 5A and 5B are cross-sectional views of a portion of a microelectronic substrate undergoing a process of forming additional LED structures in accordance with embodiments of the technology.

DETAILED DESCRIPTION

[0011] Various embodiments of microelectronic substrates having LEDs formed thereon and associated methods of manufacturing are described below. The term "microelectronic substrate" is used throughout to include substrates upon which and/or in which microelectronic devices, micromechanical devices, data storage elements, read/write components, and other features are fabricated. The term "silicon" generally refers to a single crystalline silicon material having a face-centered diamond cubic structure with a lattice spacing of 5.430710Å. The term "silicon(1,0,0)" and the term "silicon(1,1,1)" generally refer to crystal lattice orientations of (1,0,0) and (1,1,1) as defined by the Miller index, respectively. A discussion of the Miller index can be found in *Handbook of Semiconductor Silicon Technology* by William C. O'Mara, the disclosure of which is incorporated herein in its entirety. A person skilled in the relevant art will also understand that the technology may have additional embodiments, and that the technology

may be practiced without several of the details of the embodiments described below with reference to Figures 2A-5B.

[0012] Figures 2A and 2B are cross-sectional views of a portion of a microelectronic substrate 100 undergoing a process of surface modification in accordance with embodiments of the technology. In the embodiment shown in Figures 2A and 2B, the microelectronic substrate 100 includes a silicon material having the Si(1,0,0) orientation. In other embodiments, the microelectronic substrate 100 may include sapphire (Al_2O_3), silicon nitride (SiN), and/or other suitable substrate materials in addition to or in lieu of the silicon material having the Si(1,0,0) orientation.

[0013] As shown in Figure 2A, an initial stage of the process can include depositing a mask material 102 on a surface 101 of the microelectronic substrate 100. In one embodiment, the mask material 102 includes silicon oxide (SiO_2) and/or silicon nitride (SiN) formed on the surface 101 via thermal oxidation, chemical vapor deposition (CVD), atomic layer deposition (ALD), and/or other suitable techniques. In other embodiments, the mask material 102 can include a photoresist and/or other suitable mask materials deposited via spin coating and/or other suitable deposition techniques.

[0014] The process can then include patterning the deposited mask material 102 via photolithography and/or other suitable techniques. Subsequently, certain portions of the patterned mask material 102 may be removed via wet etching, plasma etching, laser ablation, and/or other material removal techniques. As shown in Figure 2A, removing the selected portions of the mask material 102 forms a mask having openings 104 through which selected portions of the surface 101 of the microelectronic substrate 100 are exposed.

[0015] As shown in Figure 2B, the process can include forming hexagonal lattice planes on the surface 101 of the microelectronic substrate 100 by removing material from the exposed portions of the surface 101 (e.g., etching the microelectronic substrate 100 via the openings 104). In the illustrated embodiment, the microelectronic substrate 100 includes a Si(1,0,0) wafer that can react with an alkaline anisotropic etchant (e.g., with a pH greater than about 12) as follows:

$$Si + 4(OH^-) \rightarrow Si(OH)_4 + 4e^-$$

Examples of the anisotropic etchant can include tetra-methyl-ammonium hydroxide (TMAH), potassium hydroxide (KOH), ammonium hydroxide (NH_4OH), ethylenediamine pyrocatechol

(EDP), and/or another suitable anisotropic etchant. In other embodiments, the process can include treating the exposed portions of the surface 101 with other suitable types of etchants based on the specific materials of the microelectronic substrate 100.

[0016] Without being bound by theory, it is believed that TMAH and the other anisotropic etchants can etch silicon substrates at different material removal rates along different crystal planes. For example, it is believed that TMAH can remove silicon material from the Si(1,0,0) planes much faster than that from the Si(1,1,1) planes due, at least in part, to the differences in bonding energy for silicon atoms in these planes. As a result, the Si(1,1,1) planes can act as an etch stop while the silicon material in the Si(1,0,0) planes are etched. Accordingly, treating the exposed portions of the surface 101 of the microelectronic substrate 100 with the alkaline etchant can form a plurality of indentations 111 having Si(1,1,1) planes 106. The mask material 102 can then be removed via wet etching, laser ablation, and/or other suitable techniques.

[0017] The indentations 111 may have certain profiles by controlling various parameters of the material removal operation. For example, as shown in Figure 2B, the individual indentations 111 can include two adjacent Si(1,1,1) planes 106 extending from the surface 101 toward the microelectronic substrate 100 and intercepting each other at a junction 107 to form a "zigzag" pattern when a long etching period is used. The two adjacent Si(1,1,1) planes 106 can form an angle of about 72°. In other embodiments, as shown in Figure 2C, the individual indentations 111 can include two adjacent Si(1,1,1) planes 106 extending from the surface 101 toward the microelectronic substrate 100 and a Si(1,0,0) plane 105 between the two Si(1,1,1) planes 106 if the etching period is shortened. The first and second planes 106 form an angle of about 54° and 126° relative to the Si(1,0,0) plane 105. In any of the foregoing embodiments, the individual indentations 111 can extend into the microelectronic substrate 100 at a depth *d* from the surface 101.

[0018] In certain embodiments, the process includes adjusting etching parameters to control the depth *d* and/or the final shape of the individual indentations 111. The etching parameters can include a concentration of the etchant, an etching temperature, an etching period, addition of suitable additives, and/or other suitable etching parameters. In certain embodiments, the depth *d* can be large enough (e.g., greater than about 100 microns) such that later formed GaN/InGaN materials 116 and 118 (Figures 3A-3C) do not coalesce on the microelectronic substrate 100, as discussed in more detail below with reference to Figures 3A-3C. For example, each of the GaN/InGaN materials 116 and 115 can have independent, generally constant

thicknesses in such embodiments. In other embodiments, the depth *d* can be small enough (e.g., less than about 1 micron) such that later formed GaN/InGaN materials do coalesce on the microelectronic substrate 100, as discussed in more detail below with reference to Figures 4A-4C. In such embodiments, one or more of the GaN/InGaN materials can have a thickness that varies. In further embodiments, the depth *d* can have other desired values such that later formed GaN/InGaN materials partially coalesce.

[0019] Figures 3A-3C are cross-sectional views of a portion of the microelectronic substrate 100 undergoing a process of forming non-planar LED structures in accordance with embodiments of the technology. As shown in Figure 3A, the process can include forming an LED structure 108 on the surface 101 of the microelectronic substrate 100 with the indentations 111. In one embodiment, forming the LED structure 108 can include depositing an N-type GaN material 114 (e.g., silicon doped), an InGaN material 116, and a P-type GaN material 118 (e.g., magnesium doped) on the microelectronic substrate 100 in series. In other embodiments, forming the LED structure 108 can also include depositing at least one of gallium arsenide (GaAs), aluminum gallium arsenide (AlGaAs), gallium arsenide phosphide (GaAsP), aluminum gallium indium phosphide (AlGaInP), gallium(III) phosphide (GaP), zinc selenide (ZnSe), boron nitride (BN), aluminum nitride (AlN), aluminum gallium nitride (AlGaN), aluminum gallium indium nitride (AlGaInN), and/or other suitable semiconductor materials. Techniques for forming the LED structure 108 can include metal organic CVD (MOCVD), molecular beam epitaxy (MBE), liquid phase epitaxy, and/or other suitable techniques.

[0020] In the illustrated embodiment of Figure 3A, the LED structure 108 includes non-planar first and second surfaces 120 and 122 that individually have a zigzag pattern. The first and second surfaces 120 and 122 generally conform to the zigzag pattern of the Si(1,1,1) planes 106 on the surface 101 of the substrate. Without being bound by theory, it is believed that the zigzag pattern of the first and second surfaces 120 and 122 can at least reduce flexing of the GaN/InGaN materials 114, 116, and 118 relative to the microelectronic substrate 100 under thermal stress. It is believed that the difference in TEC of the GaN/InGaN materials 114, 116, and 118 and the substrate 100 can create tensile stress (as indicated by the arrows 124a and 124b) along the first and second surfaces 120 and 122. As shown in Figure 3A, the zigzag pattern forces the tensile stress 124a and 124b to be at least partially opposite each other along two sides of the zigzag pattern. As a result, the tensile stress 124a and 124b can at least partially

cancel each other (e.g., in the horizontal plane X) to reduce bowing and/or otherwise flexing of the GaN/InGaN materials 114, 116, and 118.

[0021] As shown in Figure 3B, the process can then include removing a bottom portion 103 of the microelectronic substrate 100 via mechanical processes, such as back grinding, and/or other suitable techniques. As shown in Figure 3C, the process can also include removing the remaining microelectronic substrate 100 from the LED structure 108 via wet etching, dry etching, and/or other suitable techniques. The process can further include forming the first and second contacts 20 and 22 for the P-type GaN material 118 and the N-type GaN material 114, respectively, and/or other subsequent processing operations.

[0022] Figures 4A and 4B are cross-sectional views of a portion of the microelectronic substrate 100 undergoing a process of forming partially planar LED structures in accordance with embodiments of the technology. Figure 4C is a partially enlarged cross-sectional view of a portion of the planar LED in Figure 4B. As shown in Figure 4A, the process can include forming an LED structure 108 on the microelectronic substrate 100 by depositing an N-type GaN material 114 (e.g., silicon doped), an InGaN material 116, and a P-type GaN material 118 (e.g., magnesium doped) on the microelectronic substrate 100 in series. In the illustrated embodiment, the N-type GaN material 114 coalesced while being formed on the microelectronic substrate 100. As a result, the thickness of the N-type GaN material 114 is not constant such that it has a generally planar surface 115 opposite the microelectronic substrate 100. In other embodiments, the InGaN material 116 and/or the P-type GaN material 118 may coalesce to have a generally planar surface (not shown). The process can then include removing a bottom portion of the microelectronic substrate 100 via back grinding and removing the remaining microelectronic substrate 100 from the LED structure 108 via wet etching, dry etching, and/or other suitable techniques, as discussed above with reference to Figures 3B and 3C to yield the LED structure 108 as shown in Figure 4B.

[0023] It is believed that coalescing at least one of the GaN/InGaN materials 114, 116, and 118 can reduce a dislocation density in the LED structure 108. The term "dislocation" generally refers to a crystallographic defect, or irregularity, within a crystal structure. For example, as shown in Figure 4C, the N-type GaN material 114 includes a first dislocation 126a and a second dislocation 126b on two sides of the zigzag pattern. It is believed that during deposition of the N-type GaN material 114, surface tension and/or other physical/chemical interactions may cause the first and second dislocations 126a and 126b to bend toward each other and form a loop if the

Burgers vectors of these two dislocations 126a and 126b have different signs. As a result, none of the first and second dislocations 126a and 126b would extend all the way to the surface 115 of the N-type GaN material 114 thus reducing the dislocation density of the N-type GaN material 114.

[0024] Several embodiments of the LED 108 discussed above with reference to Figures 2A-5B can have increased light emitting surface areas compared to conventional LEDs. For example, as shown in Figures 2B and 2C, the indentations 111 can increase the surface area upon which the LED structure 108 (Figures 3A-3C) can be formed. As a result, the LED structure 108 can have an increased light emitting area without increasing the footprint of the LED structure 108.

[0025] Even though the LED structures 108 are discussed above as having at least one surface with a zigzag pattern, in other embodiments, the LED structures 108 can also have other surface patterns. For example, as shown in Figure 5A, by adjusting a width of the mask material 102 (Figures 2A and 2B), the indentations 111 may be separated from one another by a planar portion 115 of the N-type GaN material 114, and the InGaN and P-type GaN materials 116 and 118 may generally conform to the N-type GaN material 114. As a result, the LED structure 108 can include non-planar first and second surfaces 120 and 122. In another embodiment, as shown in Figure 5B, at least one of the InGaN and P-type GaN materials 116 and 118 may coalesce on the N-type GaN material 114. As a result, the LED structure 108 can include a generally planar first surface 120 and a non-planar second surface 122. In other embodiments, the LED structures 108 may have other suitable surface patterns.

[0026] In certain embodiments, the process can also include forming a mirror layer (e.g., aluminum, not shown) and a support structure (e.g., a silicon and/or silicon oxide material, not shown) on first surface 120 of the LED structures 108 (Figure 3A-3C). In further embodiments, the process can include depositing buffer materials (e.g., aluminum oxide, aluminum nitride, etc.) and/or other suitable materials on the surface of the microelectronic substrate 100 (Figure 3A) before the N-type GaN material 114 is formed on the microelectronic substrate 100.

[0027] From the foregoing, it will be appreciated that specific embodiments of the technology have been described herein for purposes of illustration, but that various modifications may be made without deviating from the disclosure. Many of the elements of one embodiment may be combined with other embodiments in addition to or in lieu of the elements

of the other embodiments. Accordingly, the disclosure is not limited except as by the appended claims.

CLAIMS

We claim:

1. A method for processing a silicon substrate, comprising:

applying an anisotropic etchant to a surface of the silicon substrate, the silicon substrate having a Si(1,0,0) lattice orientation at the surface;

forming an indentation on the surface of the silicon substrate with the applied anisotropic etchant, the indentation being defined by at least one plane with a Si(1,1,1) lattice orientation; and

forming a light emitting diode structure on the at least one plane with the Si(1,1,1) lattice orientation of the indentation.

2. The method of claim 1 wherein

the method further includes:

depositing a mask material on the surface of the silicon substrate; and

patterning the mask material to form a plurality of openings to the surface of the silicon substrate;

applying an anisotropic etchant includes applying a solution containing at least one of tetra-methyl-ammonium hydroxide (TMAH), potassium hydroxide (KOH), ammonium hydroxide (NH_4OH), and ethylenediamine pyrocatechol (EDP) to the surface of the silicon substrate via the openings;

forming an indentation includes forming a plurality of indentations individually having a first Si(1,1,1) plane and a second Si(1,1,1) plane both extending toward the silicon substrate from the surface to a depth, the first and second Si(1,1,1) planes forming a zigzag pattern;

the method further includes adjusting at least one of a concentration of the anisotropic etchant, an etching temperature, and an etching period to achieve a value of the depth that is greater than about 100 microns; and

forming a light emitting diode structure includes depositing an N-type gallium nitride (GaN) material, an indium gallium nitride (InGaN) material, and a P-type GaN material on the first and second Si(1,1,1) planes in sequence via metal organic

chemical vapor deposition (MOCVD), the N-type GaN, InGaN, and P-type GaN materials having surfaces generally conforming to the zigzag pattern of the first and second Si(1,1,1) planes.

3. The method of claim 1 wherein

the method further includes:

depositing a mask material on the surface of the silicon substrate; and

patterning the mask material to form a plurality of openings to the surface of the silicon substrate;

applying an anisotropic etchant includes applying a solution containing at least one of tetra-methyl-ammonium hydroxide (TMAH), potassium hydroxide (KOH), ammonium hydroxide (NH_4OH), and ethylenediamine pyrocatechol (EDP) to the surface of the silicon substrate via the openings;

forming an indentation includes forming a plurality of indentations individually having a first Si(1,1,1) plane and a second Si(1,1,1) plane both extending toward the silicon substrate from the surface to a depth, the first and second Si(1,1,1) planes forming a zigzag pattern;

the method further includes adjusting at least one of a concentration of the anisotropic etchant, an etching temperature, and an etching period to achieve a value of the depth that is less than about 1 micron; and

forming a light emitting diode structure includes:

depositing an N-type gallium nitride (GaN) material, an indium gallium nitride (InGaN) material, and a P-type GaN material on the first and second Si(1,1,1) planes in sequence via metal organic chemical vapor deposition (MOCVD); and

coalescing at least one of the N-type GaN, InGaN, and P-type GaN materials during the MOCVD operation.

4. The method of claim 1 wherein

applying an anisotropic etchant includes applying a solution containing at least one of tetra-methyl-ammonium hydroxide (TMAH), potassium hydroxide (KOH),

ammonium hydroxide (NH_4OH), and ethylenediamine pyrocatechol (EDP) to the surface of the silicon substrate; and

forming a light emitting diode structure includes depositing an N-type gallium nitride (GaN) material, an indium gallium nitride (InGaN) material, and a P-type GaN material on the first and second Si(1,1,1) planes in sequence.

5. The method of claim 1 wherein forming an indentation includes forming an indentation having a first Si(1,1,1) plane, a second Si(1,1,1) plane, and a Si(1,0,0) plane extending between the first and second Si(1,1,1) planes.

6. The method of claim 1 wherein forming an indentation includes forming an indentation having a first Si(1,1,1) plane and a second Si(1,1,1) plane intercepting the first Si(1,1,1) plane at a junction.

7. The method of claim 1 wherein forming a light emitting diode structure includes depositing an N-type GaN material, an InGaN material, and a P-type GaN material on the at least one plane of the indentation in sequence, the plane having the Si(1,1,1) lattice orientation.

8. The method of claim 1 wherein:

forming an indentation includes forming an indentation extending toward the silicon substrate from the surface to a depth; and

the method further includes adjusting at least one of a concentration of the anisotropic etchant, an etching temperature, and an etching period to achieve a desired value of the depth.

9. A method for processing a silicon substrate, comprising:

reacting a surface of a silicon substrate with an anisotropic etchant, at least a portion of the silicon substrate having a Si(1,0,0) lattice orientation at the surface;

removing silicon material from the surface of the silicon substrate along a Si(1,0,0) plane faster than along a Si(1,1,1) plane, thereby exposing the Si(1,1,1) plane; and

depositing an N-type GaN material, an InGaN material, and a P-type GaN material on the exposed Si(1,1,1) plane in sequence via epitaxial growth.

10. The method of claim 9 wherein reacting a surface of a silicon substrate with an anisotropic etchant includes reacting the surface of the silicon substrate with the anisotropic etchant as follows:

$$Si + 4(OH^-) \rightarrow Si(OH)_4 + 4e^-$$

11. The method of claim 9 wherein reacting a surface of a silicon substrate with an anisotropic etchant includes reacting the surface of the silicon substrate with at least one of tetra-methyl-ammonium hydroxide (TMAH), potassium hydroxide (KOH), ammonium hydroxide (NH_4OH), and ethylenediamine pyrocatechol (EDP).

12. The method of claim 9 wherein

reacting a surface of a silicon substrate with an anisotropic etchant includes reacting the surface of the silicon substrate with the anisotropic etchant as follows:

$$Si + 4(OH^-) \rightarrow Si(OH)_4 + 4e^-$$; and

removing silicon material includes preferentially removing the silicon material along the Si(1,0,0) plane while using the Si(1,1,1) plane as an etch stop.

13. The method of claim 9 wherein

reacting a surface of a silicon substrate with an anisotropic etchant includes reacting the surface of the silicon substrate with the anisotropic etchant as follows:

$$Si + 4(OH^-) \rightarrow Si(OH)_4 + 4e^-$$

removing silicon material includes preferentially removing the silicon material along the Si(1,0,0) plane while using the Si(1,1,1) plane as an etch stop; and

depositing an N-type GaN material, an InGaN material, and a P-type GaN material includes generally conforming the N-type GaN, InGaN, and P-type GaN materials to the Si(1,1,1) plane.

14. The method of claim 9 wherein

reacting a surface of a silicon substrate with an anisotropic etchant includes reacting the surface of the silicon substrate with the anisotropic etchant as follows:

$$Si + 4(OH^-) \rightarrow Si(OH)_4 + 4e^-$$

removing silicon material includes preferentially removing the silicon material along the Si(1,0,0) plane while using the Si(1,1,1) plane as an etch stop; and

depositing an N-type GaN material, an InGaN material, and a P-type GaN material includes depositing the N-type GaN, InGaN, and P-type GaN materials on the exposed Si(1,1,1) plane, the N-type GaN, InGaN, and P-type GaN materials individually forming a zigzag pattern.

15. The method of claim 9 wherein

reacting a surface of a silicon substrate with an anisotropic etchant includes reacting the surface of the silicon substrate with the anisotropic etchant as follows:

$$Si + 4(OH^-) \rightarrow Si(OH)_4 + 4e^-$$

removing silicon material includes preferentially removing the silicon material along the Si(1,0,0) plane while using the Si(1,1,1) plane as an etch stop; and

depositing an N-type GaN material, an InGaN material, and a P-type GaN material includes coalescing at least one of the N-type GaN material, the InGaN material, and a P-type GaN material to the Si(1,1,1) plane.

16. The method of claim 9 wherein

reacting a surface of a silicon substrate with an anisotropic etchant includes reacting the surface of the silicon substrate with the anisotropic etchant as follows:

$$Si + 4(OH^-) \rightarrow Si(OH)_4 + 4e^-$$

removing silicon material includes preferentially removing the silicon material along the Si(1,0,0) plane while using the Si(1,1,1) plane as an etch stop; and

depositing an N-type GaN material, an InGaN material, and a P-type GaN material includes depositing the N-type GaN, InGaN, and P-type GaN materials on the exposed Si(1,1,1) plane, at least one of the N-type GaN, InGaN, and P-type GaN materials having a generally planar surface.

17. A light emitting diode, comprising:

an N-type gallium nitride (GaN) material;

a P-type GaN material spaced apart from the N-type GaN material; and

an indium gallium nitride (InGaN) material directly between the N-type GaN material and the P-type GaN material;

wherein at least one of the N-type GaN, InGaN, and P-type GaN materials has a non-planar surface.

18. The light emitting diode of claim 17 wherein non-planar surface has a zigzag pattern.

19. The light emitting diode of claim 17 wherein non-planar surface has a plurality of indentations formed by a first plane and a second plane joined together at a junction.

20. The light emitting diode of claim 17 wherein non-planar surface has a plurality of indentations formed by a first plane and a second plane joined together at a junction, the first and second planes forming an angle of about 72°.

21. The light emitting diode of claim 17 wherein non-planar surface has a plurality of indentations formed by a first plane, a second plane, and a third plane extending between the first and second planes, the first and second planes forming an angle of about 54° and 126° with the third plane, respectively.

22. The light emitting diode of claim 17 wherein the N-type GaN, InGaN, and P-type GaN materials individually have a surface with a zigzag pattern.

23. The light emitting diode of claim 17 wherein at least one of the N-type GaN, InGaN, and P-type GaN materials have a first surface and a second surface opposite the first surface, the first surface being non-planar and the second surface being generally planar.

24. The light emitting diode of claim 17 wherein at least one of the N-type GaN, InGaN, and P-type GaN materials have a first surface and a second surface opposite the first surface, the first surface having a zigzag pattern and the second surface being generally planar.