METHOD TO REDUCE VARIATION IN LDD SERIES RESISTANCE

ABSTRACT

A process used to retard out diffusion of P type dopants from P type LDD regions, resulting in unwanted LDD series resistance increases, has been developed. The process features the formation of a nitrogen containing layer, placed between the P type LDD region and overlying silicon oxide regions, retarding the diffusion of boron from the LDD regions to the overlying silicon oxide regions, during subsequent high temperature anneals. The nitrogen containing layer, such as a thin silicon nitride layer, or a silicon oxynitride layer, formed during or after reoxidation of a P type polysilicon gate structure, is also formed in a region that also retards the out diffusion of P type dopants from the P type polysilicon gate structure.

Fig. 8