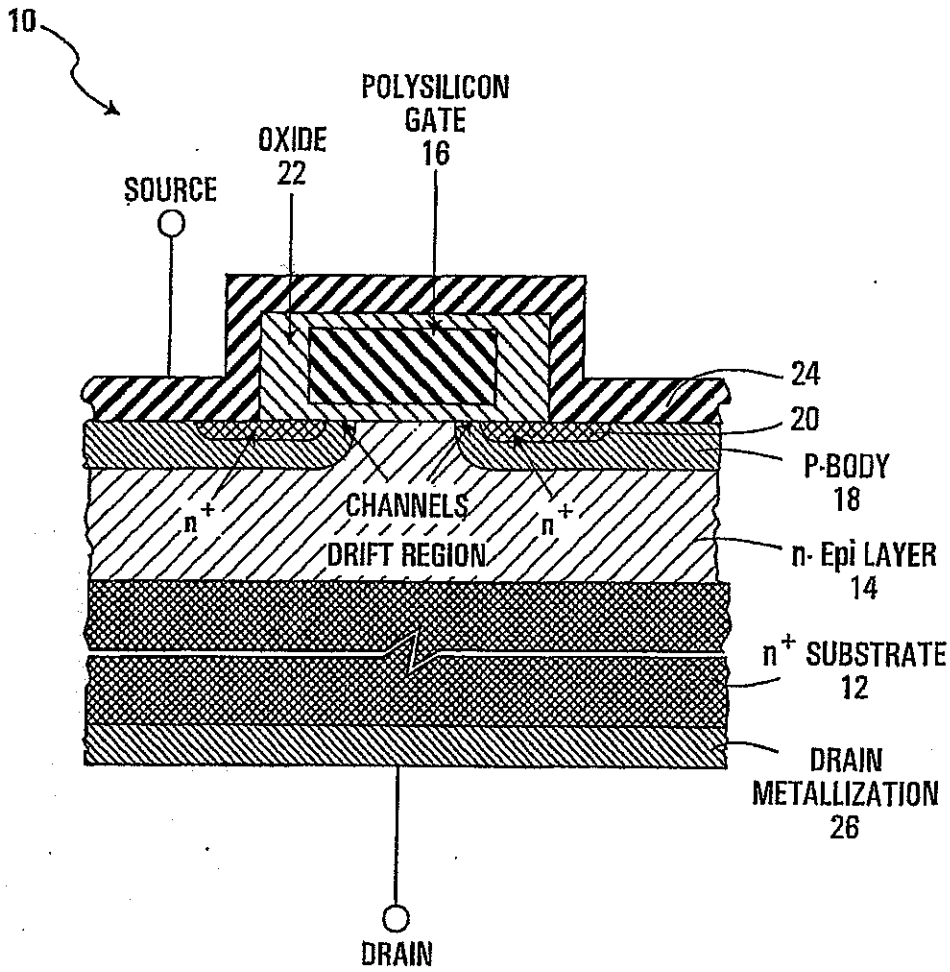

10
POLYSILICON GATE 16
OXIDE 22
SOURCE
24
20
P-BODY 18
CHANNELS
n+
n+
DRIFT REGION
n- Epi LAYER 14
n+ SUBSTRATE 12
DRAIN METALLIZATION 26
DRAIN

FIG. 1

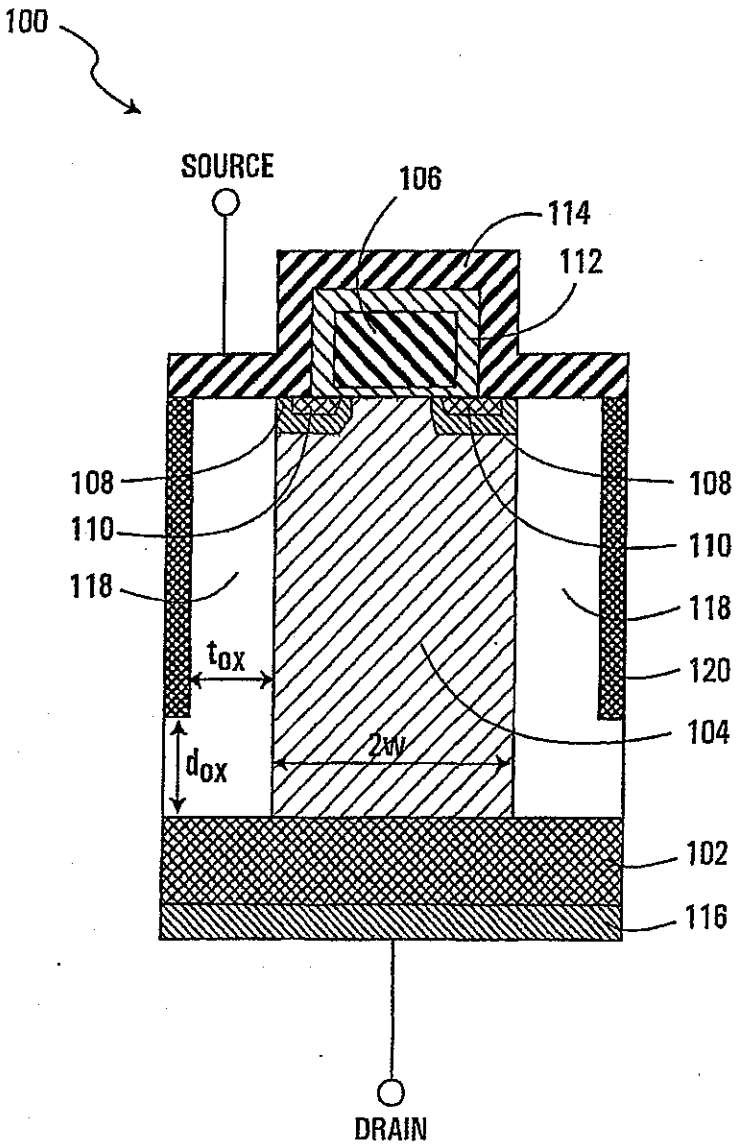

100
SOURCE
106
114
112
108
110
118
108
110
118
120
104
102
116
t_{ox}
d_{ox}
2W
DRAIN

FIG. 2A

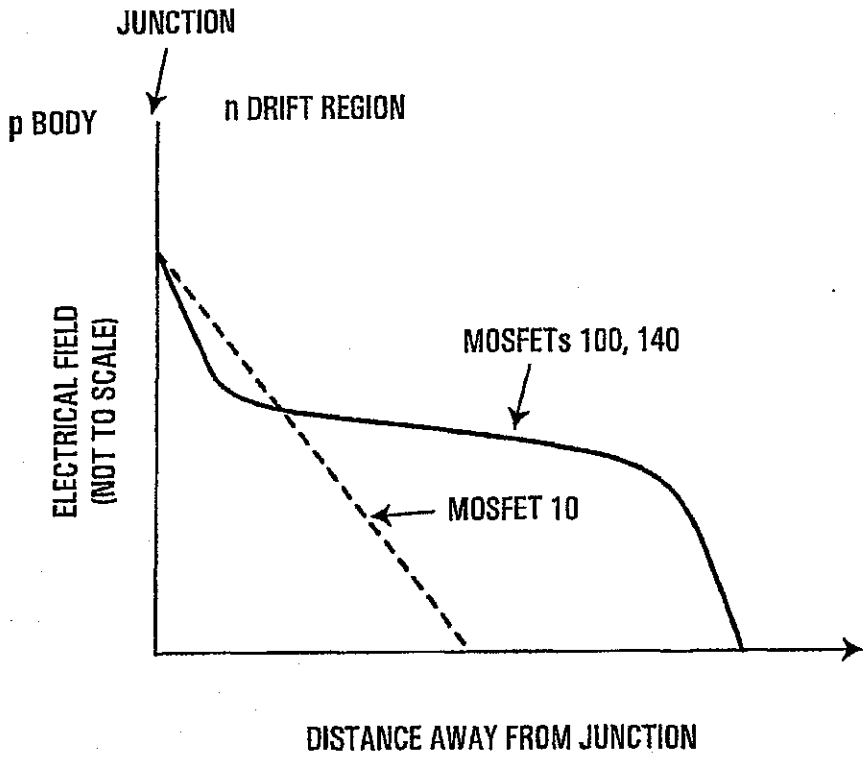

JUNCTION
p BODY
n DRIFT REGION
ELECTRICAL FIELD
(NOT TO SCALE)
MOSFETs 100, 140
MOSFET 10
DISTANCE AWAY FROM JUNCTION

FIG. 2B

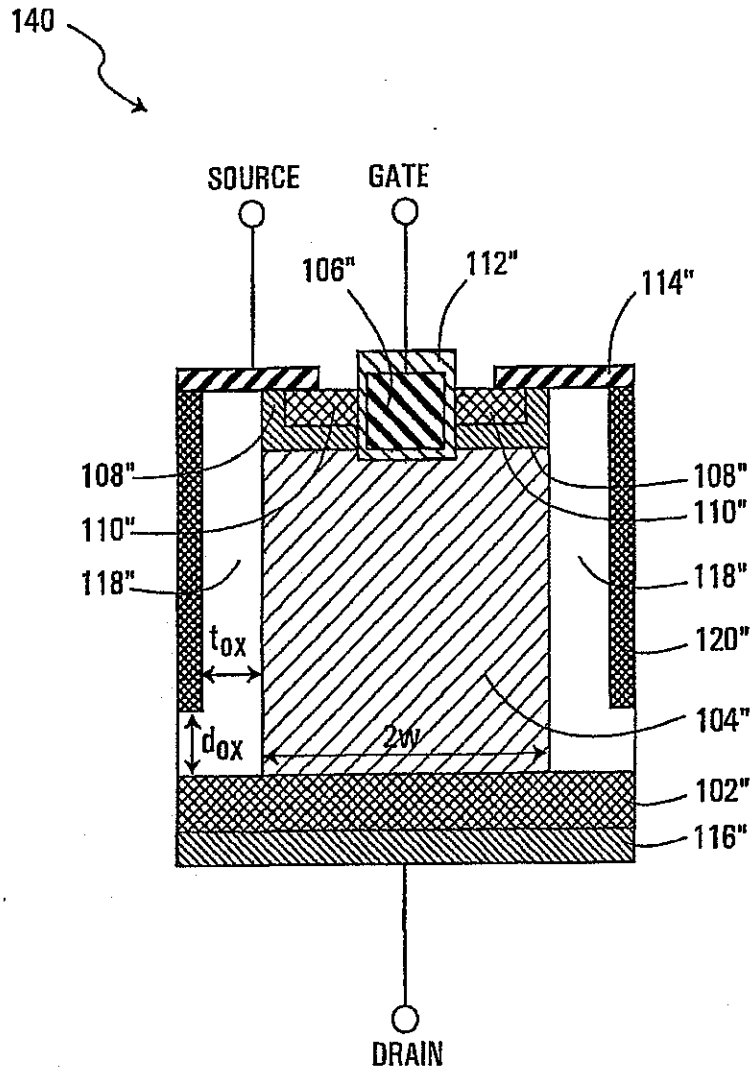

140
SOURCE
GATE
106"
112"
114"
108"
110"
118"
t_{ox}
d_{ox}
2w
108"
110"
118"
120"
104"
102"
116"
DRAIN

FIG. 3

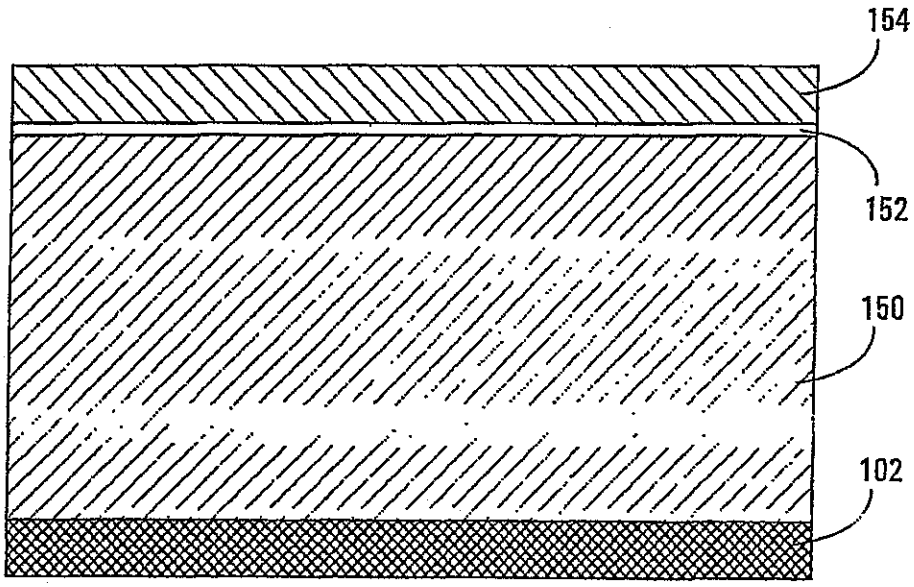


FIG. 4

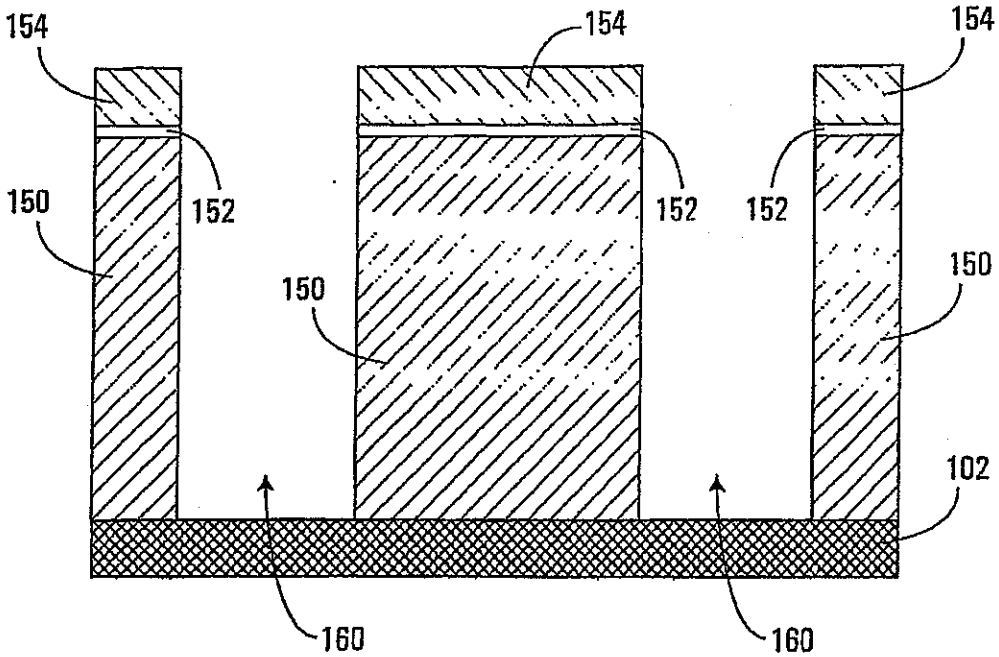

154
154
154
150
152
152
152
150
150
102
160
160

FIG. 5A

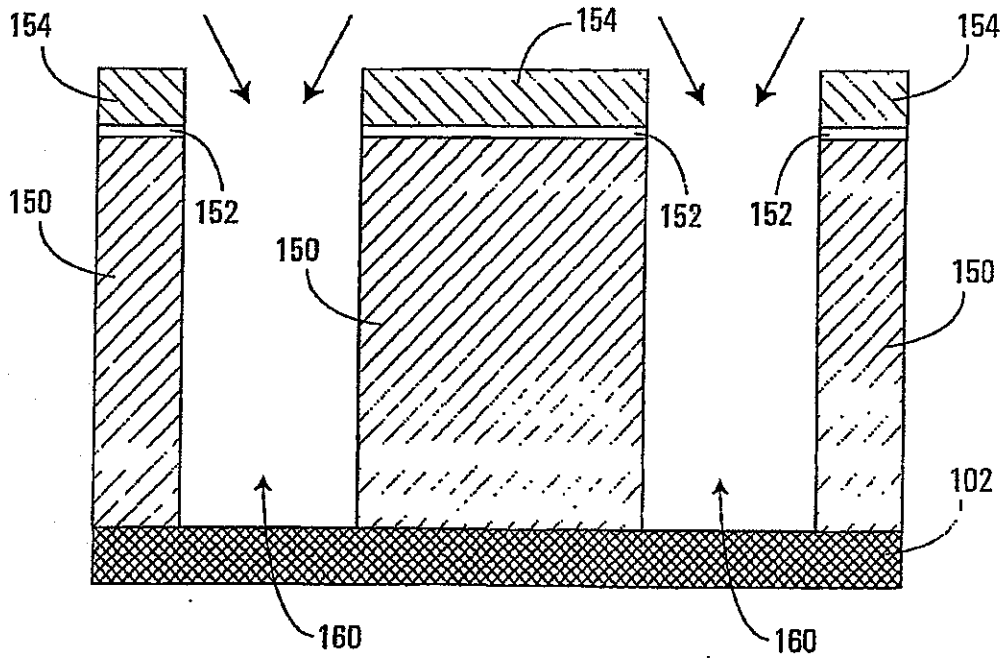

154
154
154
150
152
152
152
150
150
102
160
160

FIG. 5B

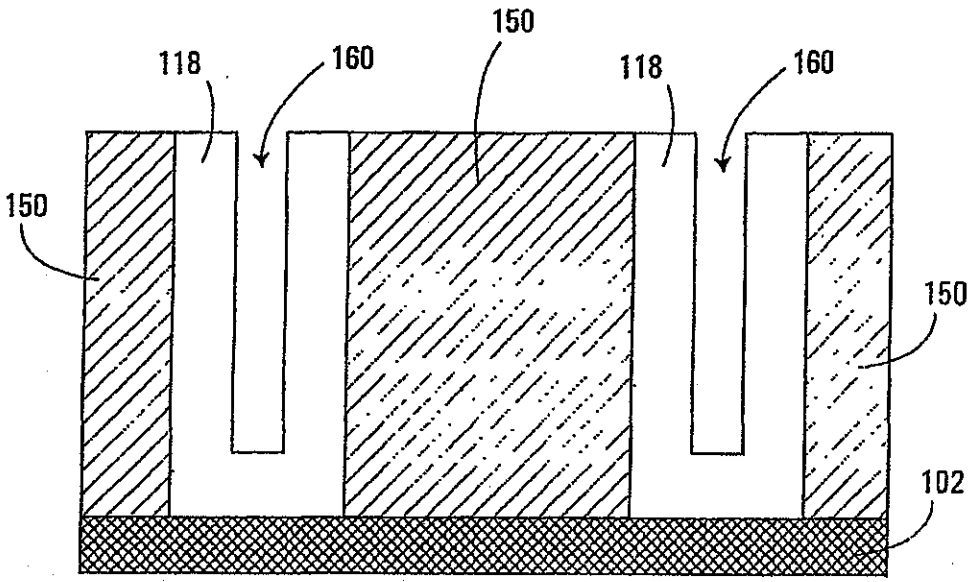


FIG. 6A

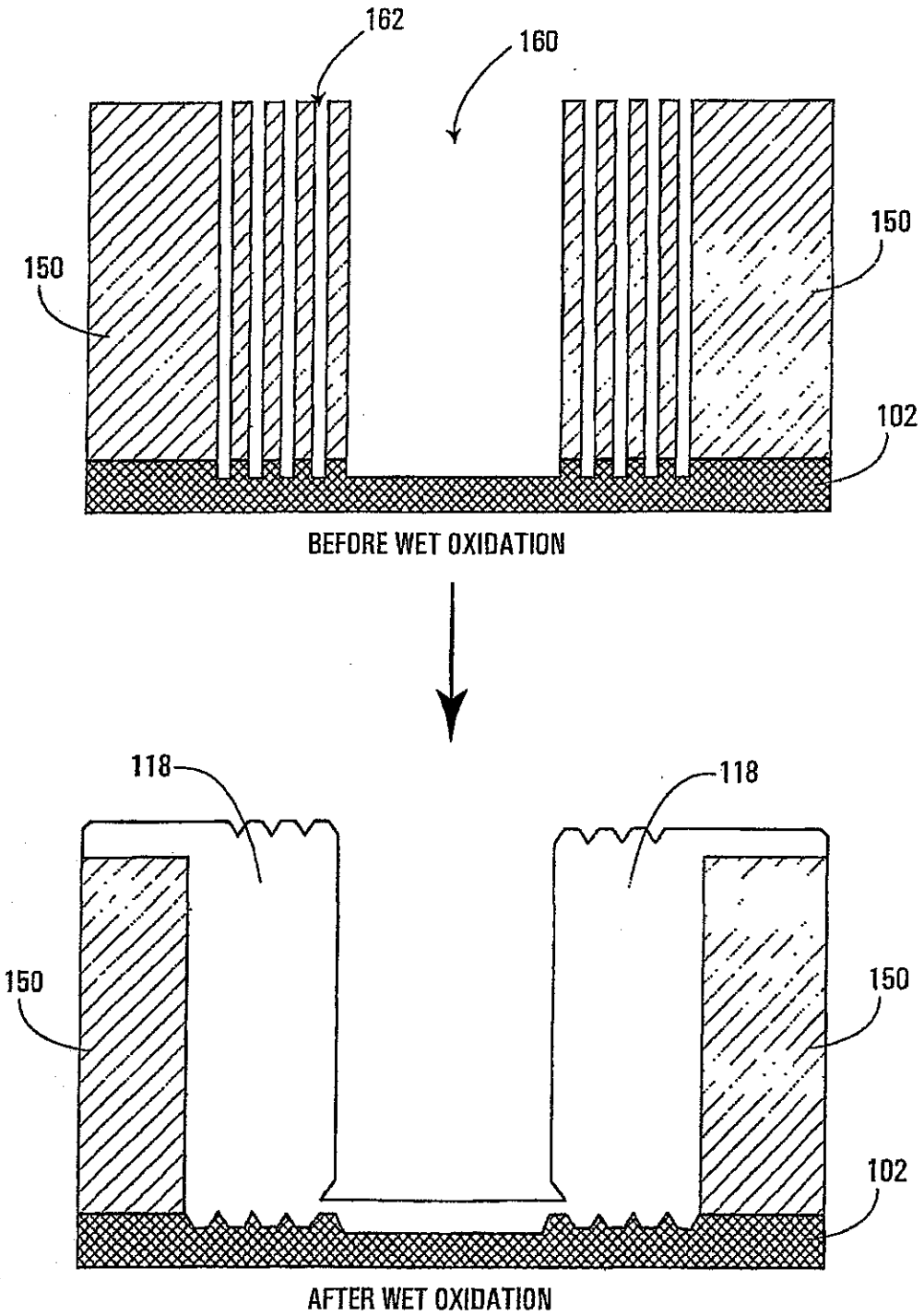

162
160
150
150
102
BEFORE WET OXIDATION
118
118
150
150
102
AFTER WET OXIDATION

FIG. 6B

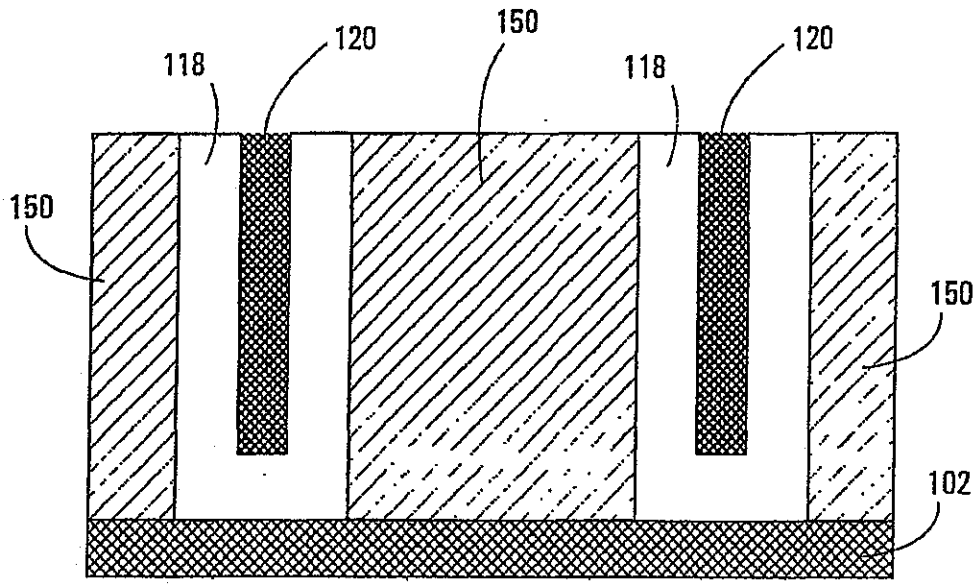


FIG. 7

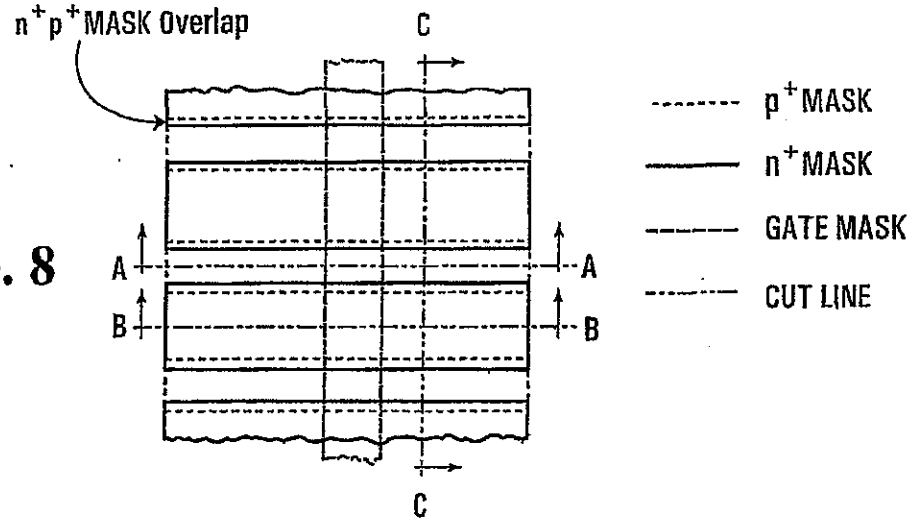


FIG. 8

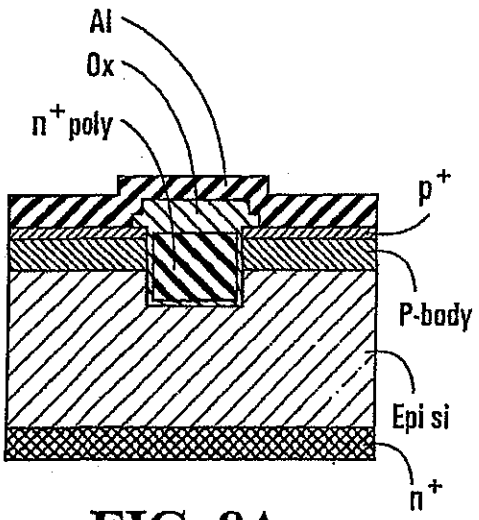


FIG. 8A

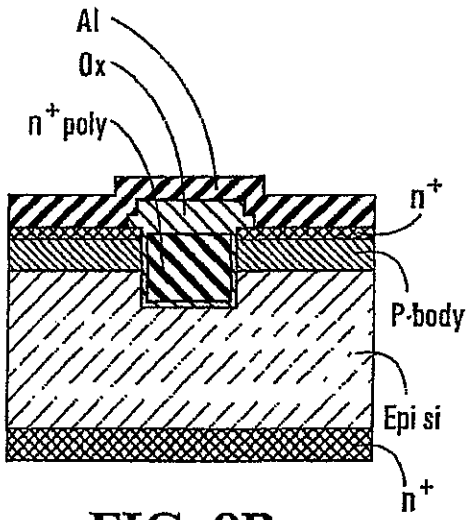


FIG. 8B

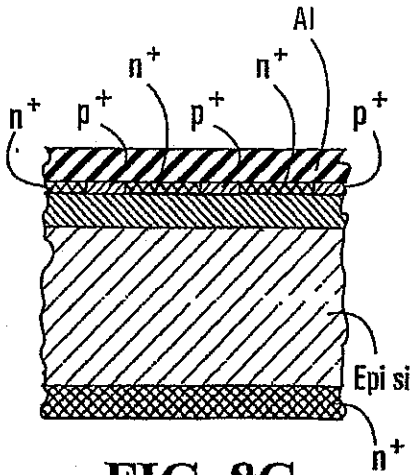


FIG. 8C

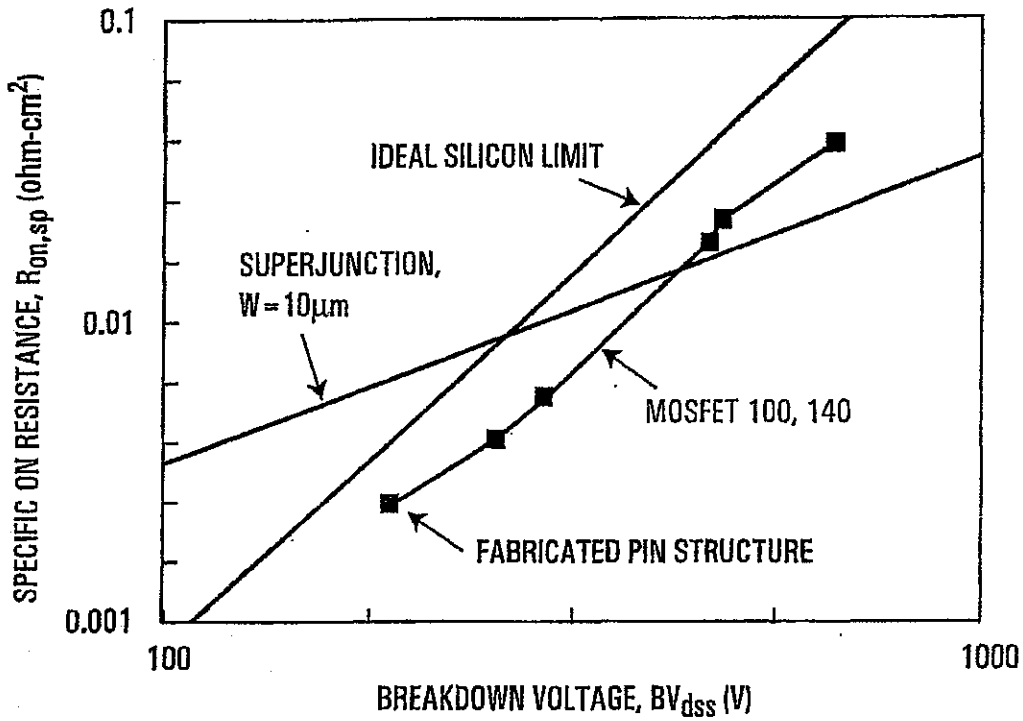

0.1
0.01
0.001
100
1000
SPECIFIC ON RESISTANCE, $R_{on,sp}$ (ohm-cm^2)
BREAKDOWN VOLTAGE, BV_{dss} (V)
IDEAL SILICON LIMIT
SUPERJUNCTION,
W = 10μm
MOSFET 100, 140
FABRICATED PIN STRUCTURE

FIG. 9

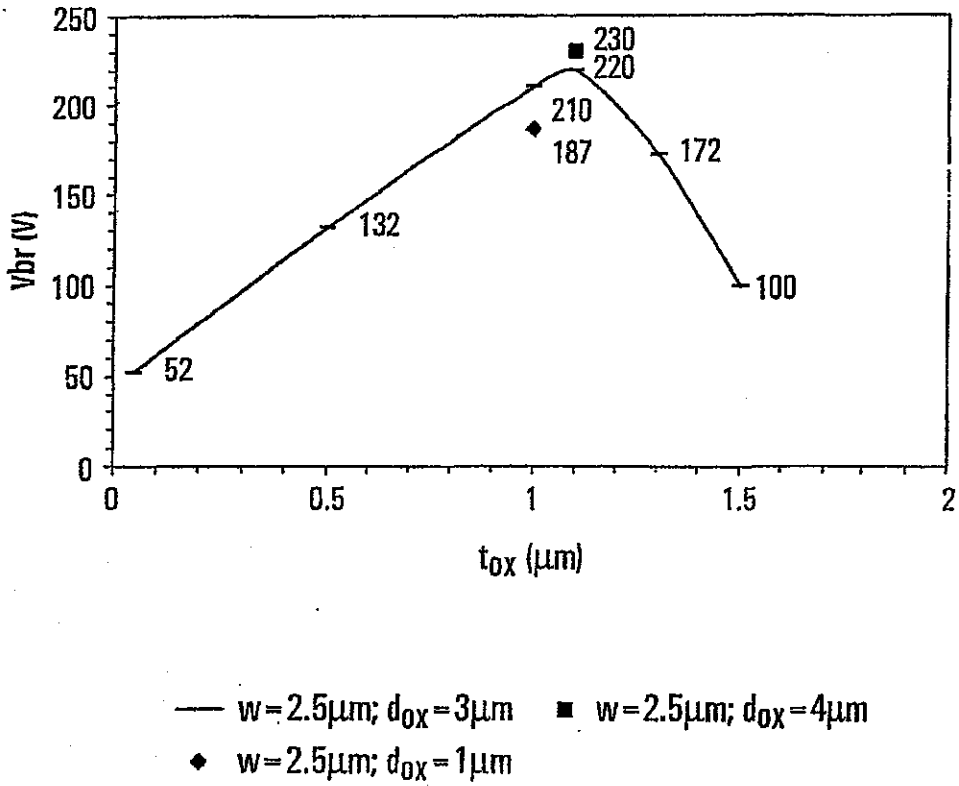

250
200
150
100
50
0
Vbr (V)
0
0.5
1
1.5
2
t_{ox} (μm)
230
220
210
187
172
132
100
52
w=2.5μm; d_{ox}=3μm
w=2.5μm; d_{ox}=4μm
w=2.5μm; d_{ox}=1μm

FIG. 10

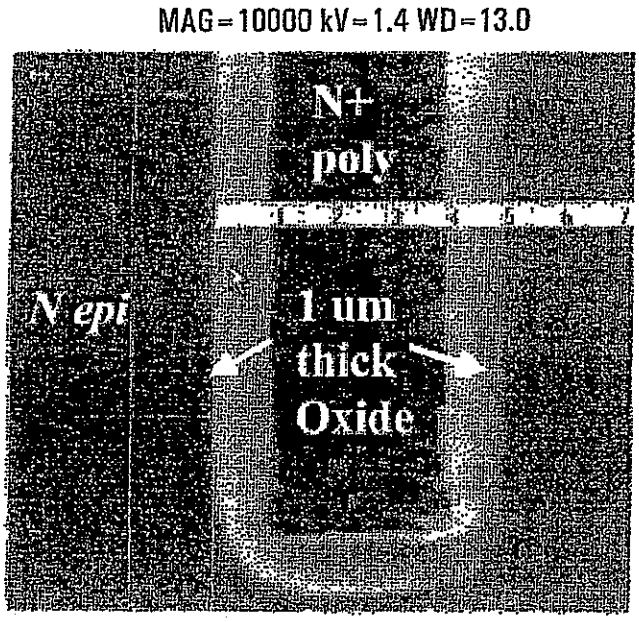


FIG. 11

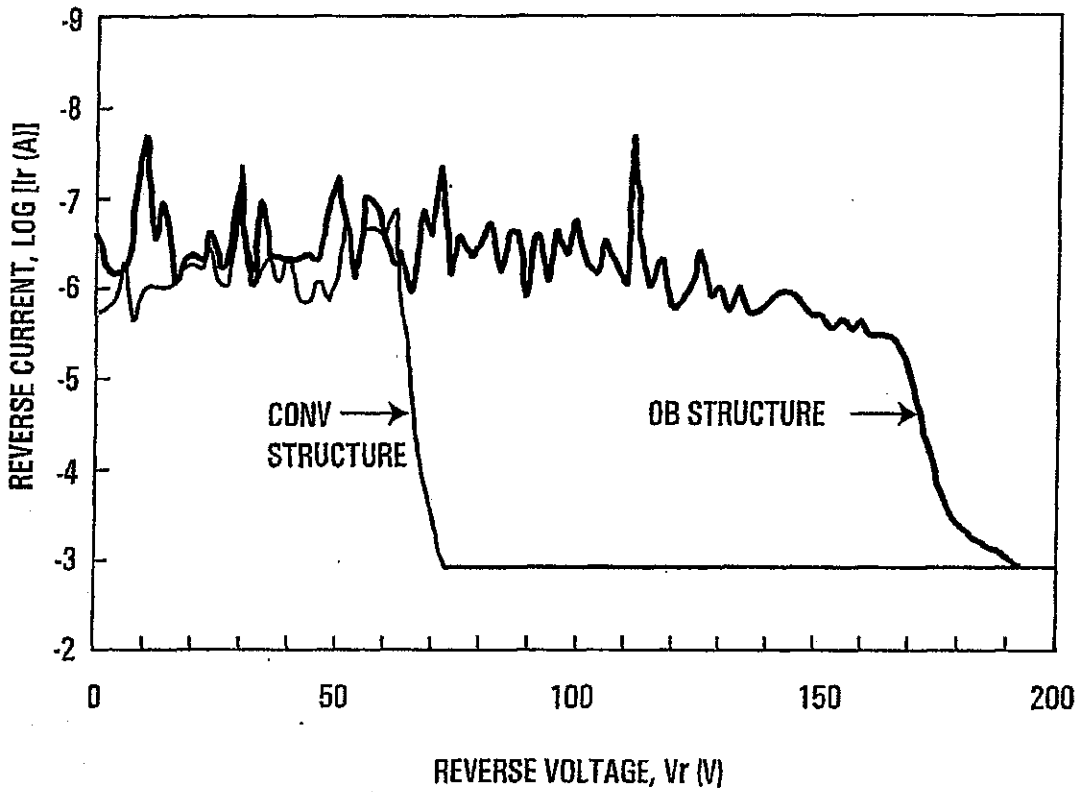

-9
-8
-7
-6
-5
-4
-3
-2
REVERSE CURRENT, LOG [Ir (A)]
CONV
STRUCTURE
OB STRUCTURE
0
50
100
150
200
REVERSE VOLTAGE, Vr (V)

FIG. 12

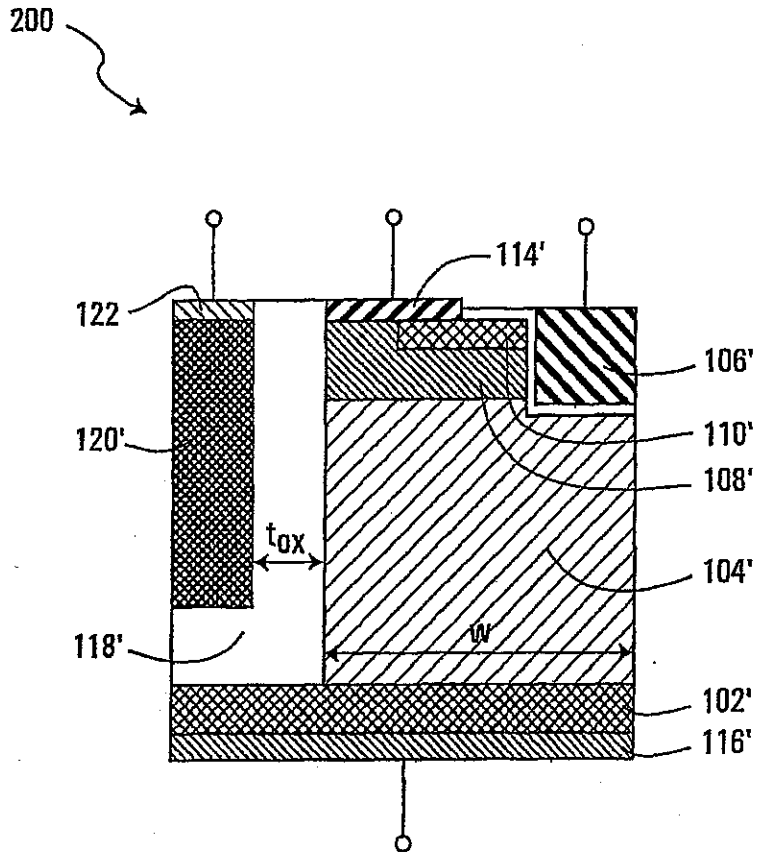


FIG. 13

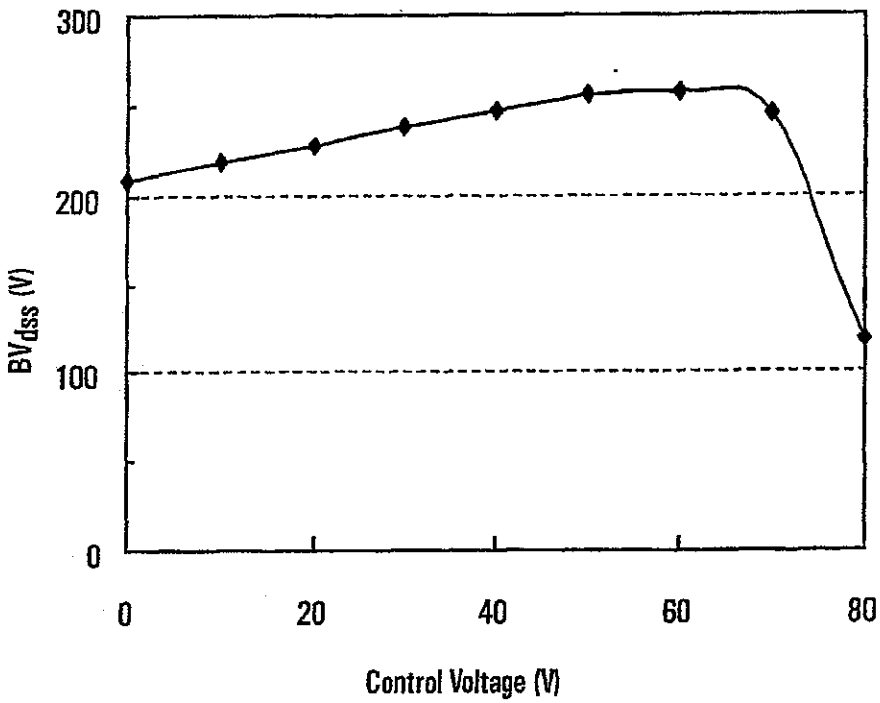


FIG. 14

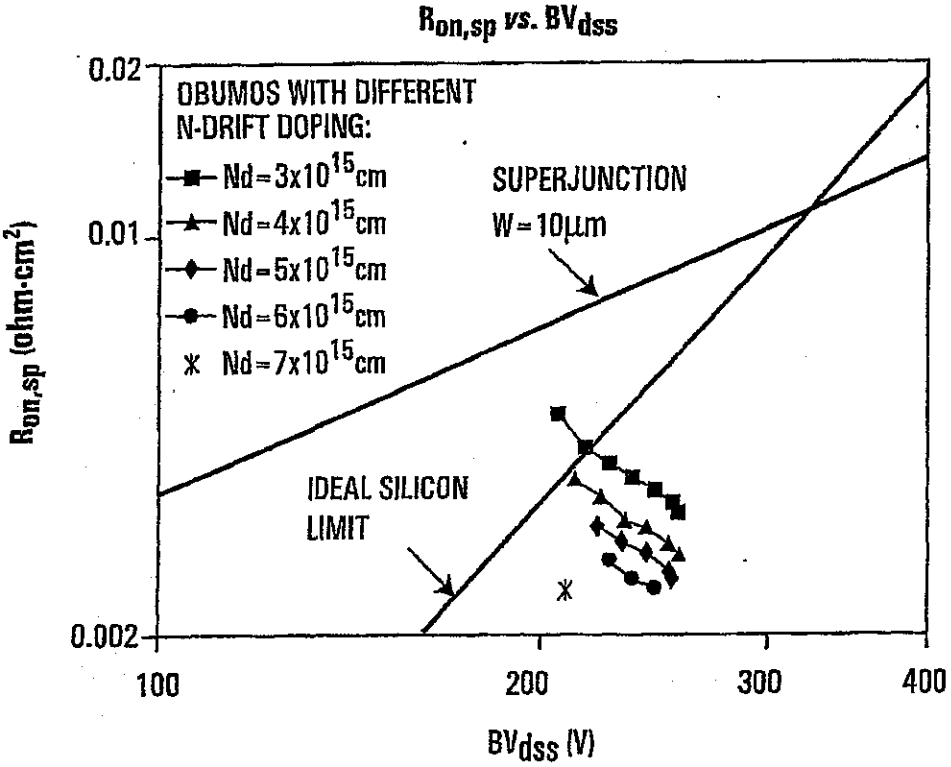

$R_{on,sp}$ vs. BV_{dss}
0.02
0.01
0.002
$R_{on,sp}$ (ohm-cm^2)
OBUMOS WITH DIFFERENT
N-DRIFT DOPING:
Nd=3x10^{15}cm
Nd=4x10^{15}cm
Nd=5x10^{15}cm
Nd=6x10^{15}cm
Nd=7x10^{15}cm
SUPERJUNCTION
W=10µm
IDEAL SILICON
LIMIT
100
200
300
400
BV_{dss} (V)

FIG. 15

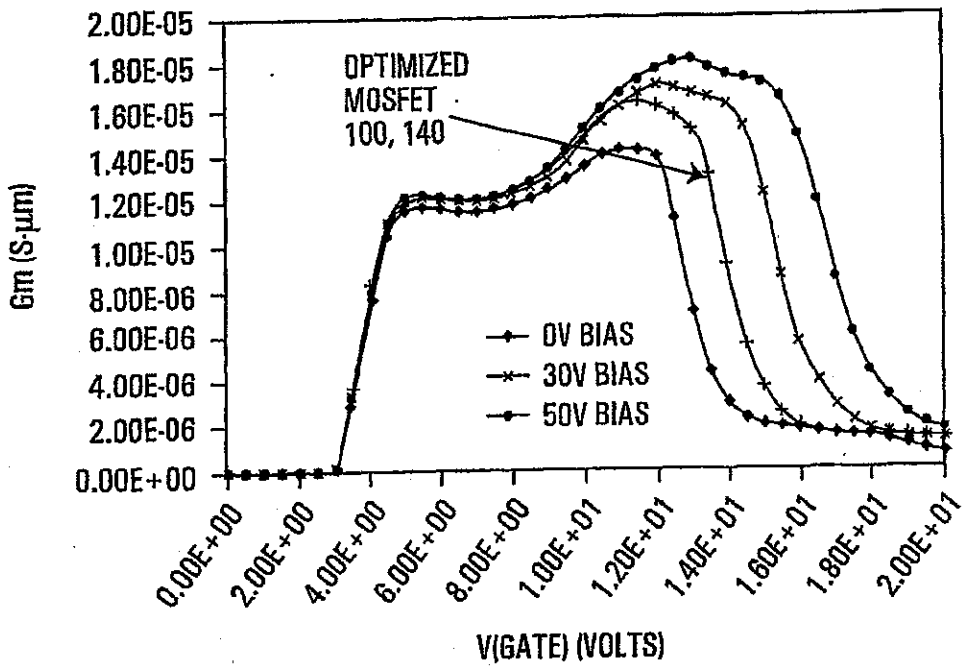

2.00E-05
1.80E-05
1.60E-05
1.40E-05
1.20E-05
1.00E-05
8.00E-06
6.00E-06
4.00E-06
2.00E-06
0.00E+00
Gm (S-µm)
OPTIMIZED
MOSFET
100, 140
0V BIAS
30V BIAS
50V BIAS
0.00E+00
2.00E+00
4.00E+00
6.00E+00
8.00E+00
1.00E+01
1.20E+01
1.40E+01
1.60E+01
1.80E+01
2.00E+01
V(GATE) (VOLTS)

FIG. 16

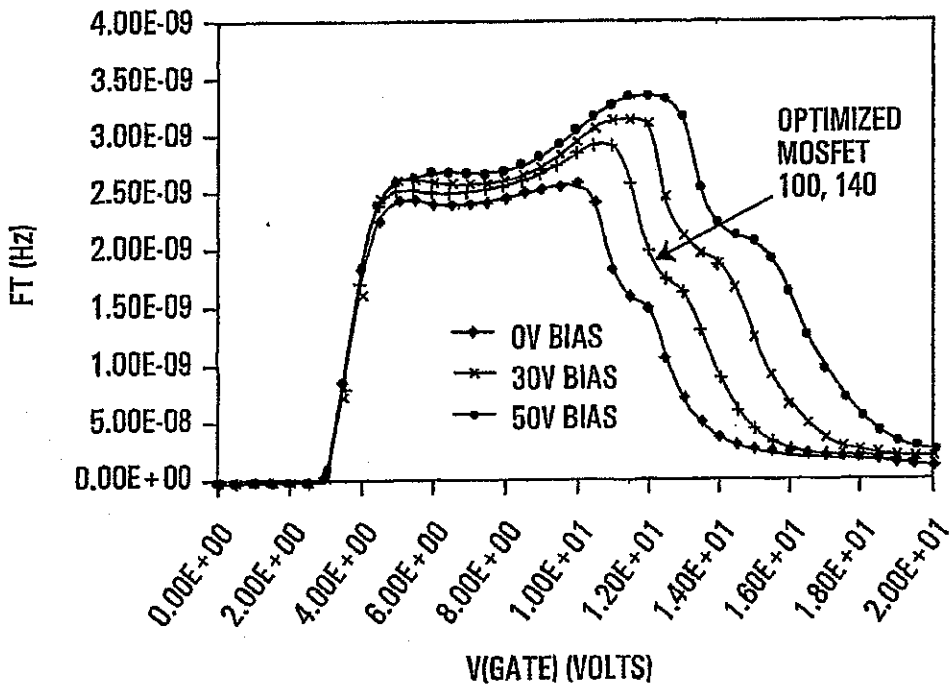

4.00E-09
3.50E-09
3.00E-09
2.50E-09
2.00E-09
1.50E-09
1.00E-09
5.00E-08
0.00E+00
FT (Hz)
OPTIMIZED
MOSFET
100, 140
0V BIAS
30V BIAS
50V BIAS
0.00E+00
2.00E+00
4.00E+00
6.00E+00
8.00E+00
1.00E+01
1.20E+01
1.40E+01
1.60E+01
1.80E+01
2.00E+01
V(GATE) (VOLTS)

FIG. 17