METHOD TO ENGINEER ETCH PROFILES IN SI SUBSTRATE FOR ADVANCED SEMICONDUCTOR DEVICES

Abstract

Structures and methods for forming keyhole shaped regions for isolation and/or stressing the substrate are shown. In a first embodiment, we form an inverted keyhole shaped trench in the substrate in the first opening preferably using a two step etch. Next, we fill the inverted keyhole trench with a material that insulates and/or creates stress on the sidewalls of the inverted keyhole trench. In a second embodiment, we form a keyhole stressor region adjacent to the gate and isolation structures. The keyhole stressor region creates stress near the channel region of the FET to improve FET performance. The stressor region can be filled with an insulator or a semiconductor material.

Figure 6