ABSTRACT OF THE DISCLOSURE

BYPASSING PIXEL CLOCK GENERATION AND CRTC CIRCUITS IN A GRAPHICS CONTROLLER CHIP

In a video processor unit, a method of providing a video data stream at a clock rate that is independent of a pixel clock rate. Receiving native video data from a video source at a native clock rate, storing the video data in a memory unit, reading selected portions of the video data at a memory clock rate, rasterizing the selected video data, packetizing the rasterized video data, sending the packetized video data to a display unit by way of a link at a link rate, wherein the link rate is directly related to the memory clock rate.