

**SnSe-BASED LIMITED REPROGRAMMABLE CELL**  
**FIELD OF THE INVENTION**

[0001] The invention relates to the field of memory devices, and particularly to memory devices which can be programmed a limited number of times.

**BACKGROUND**

[0002] Resistance variable memory elements, which include Programmable Conductive Random Access Memory (PCRAM) elements, have been investigated for suitability as semi-volatile and non-volatile random access memory elements. An exemplary PCRAM device is disclosed in U.S. Patent No. 6,348,365, which is assigned to Micron Technology, Inc.

[0003] A PCRAM device typically includes chalcogenide glass as the active switching material. A conductive material, such as silver, is incorporated into the chalcogenide glass creating a conducting channel. During operation of the device, the conducting channel can receive and expel metal ions (e.g., silver ions) to program a particular resistance state (e.g., a higher or a lower resistance state) for the memory element through subsequent programming voltages, such as write and erase voltages. After a programming voltage is removed, the programmed resistance states can remain intact for a period of time, generally ranging from hours to weeks. In this way, the typical chalcogenide glass-based PCRAM device functions as a variable resistance memory having at least two resistance states, which define two respective logic states.

[0004] One exemplary PCRAM device uses a germanium selenide (i.e.,  $\text{Ge}_x\text{Se}_{100-x}$ ) chalcogenide glass as a backbone along with silver (Ag) and silver selenide ( $\text{Ag}_{2+/-x}\text{Se}$ ). See for example U.S. Patent Application Publication No. 2004/0038432, assigned to Micron Technology, Inc.

[0005] Although the silver-chalcogenide materials are suitable for assisting in the formation of a conductive channel through the chalcogenide glass layer for silver ions to move into, other non-silver-based chalcogenide materials may be desirable because of certain disadvantages associated with silver use. For example, use of silver-containing compounds/alloys such as  $\text{Ag}_2\text{Se}$  may lead to agglomeration problems in the PCRAM device layering and Ag-chalcogenide-based devices cannot withstand higher processing temperatures, e.g., approaching  $260^\circ\text{C}$  and higher. Tin (Sn) has a reduced thermal mobility in  $\text{Ge}_x\text{Se}_{100-x}$  compared to silver and the tin-chalcogenides are less toxic than the silver-chalcogenides.

[0006] Research has been conducted into the use of thin films of SnSe (tin selenide) as switching devices under the application of a voltage potential across the film. It has been found that a  $580 \text{ \AA}$  SnSe film shows non-volatile switching between a higher resistance state (measurable in M $\Omega$ ) and a lower resistance state (measurable in k $\Omega$ ) when potentials of 5-15 V are applied by forming an Sn-rich material (e.g., a dendrite). Also, the addition of Sn to a  $\text{Ge}_x\text{Se}_{100-x}$  glass, which is a chalcogenide glass, has been found to produce memory switching if a high enough

potential, e.g., >40 V, is applied across the chalcogenide glass. However, such switching potentials are too high for a viable memory device.

[0007] One time programmable (OTP) memory cells are known and have many applications. A typical OTP memory cell may function as a fuse or an antifuse. In a memory device application, such a fuse or antifuse may be connected between a column line and a row line. In a memory cell having a fuse, a charge sent through the column line will pass through the intact fuse in a cell to a grounded row line indicating a value of 1. To change the value of a cell to 0, a specific amount of current is applied to the cell to burn out the fuse. In a cell having an antifuse, the initial unprogrammed state is 0, and the cell is programmed to a 1 state. Once the conventional OTP cells are programmed, they cannot be erased or reprogrammed.

[0008] Accordingly, it is desired to have a resistance variable memory element which can act as an OTP or OTP-like memory cell. Additionally it is desirable to have such a memory element that can be reprogrammed at least once after an initial programming.

### SUMMARY

[0009] Exemplary embodiments of the invention provide methods and apparatus for providing a memory device that can be programmed a limited number of times. According to exemplary embodiments, a memory device and its method of formation provide a first electrode, a second electrode and a layer of a chalcogenide

or germanium comprising material between the first electrode and the second electrode. The memory device further includes a tin-chalcogenide layer between the chalcogenide or germanium comprising material layer and the second electrode.

[0010] The above and other features and advantages of the invention will be better understood from the following detailed description, which is provided in connection with the accompanying drawings.

### BRIEF DESCRIPTION OF THE DRAWINGS

[0011] The foregoing and other advantages and features of the invention will become more apparent from the detailed description of exemplary embodiments provided below with reference to the accompanying drawings in which:

[0012] FIG. 1 illustrates a cross sectional view of a memory element according to an exemplary embodiment of the invention;

[0013] FIGS. 2A-2D illustrate cross-sectional views of the memory element of FIG. 1 at different stages of processing;

[0014] FIG. 3 illustrates a cross sectional view of a memory element according to another exemplary embodiment of the invention;

[0015] FIG. 4 illustrates a cross sectional view of a memory element according to another exemplary embodiment of the invention;

[0016] FIG. 5 illustrates a cross sectional view of a memory element according to another exemplary embodiment of the invention; and

[0017] FIG. 6 illustrates a processor system according to an exemplary embodiment of the invention.

### DETAILED DESCRIPTION

[0018] In the following detailed description, reference is made to various specific embodiments of the invention. These embodiments are described with sufficient detail to enable those skilled in the art to practice the invention. It is to be understood that other embodiments may be employed, and that various structural, logical and electrical changes may be made without departing from the spirit or scope of the invention.

[0019] The term "substrate" used in the following description may include any supporting structure including, but not limited to, a semiconductor substrate that has an exposed substrate surface. A semiconductor substrate should be understood to include silicon-on-insulator (SOI), silicon-on-sapphire (SOS), doped and undoped semiconductors, epitaxial layers of silicon supported by a base semiconductor foundation, and other semiconductor structures. When reference is made to a semiconductor substrate or wafer in the following description, previous process steps may have been utilized to form regions or junctions in or over the base semiconductor or foundation. The substrate need not be semiconductor-based, but

may be any support structure suitable for supporting an integrated circuit, including, but not limited to, metals, alloys, glasses, polymers, ceramics, and any other supportive materials as is known in the art.

[0020] The term "tin" is intended to include not only elemental tin, but tin with other trace metals or in various alloyed combinations with other metals as known in the semiconductor industry, as long as such tin alloy is conductive, and as long as the physical and electrical properties of the tin remain unchanged.

[0021] The term "tin-chalcogenide" is intended to include various alloys, compounds, and mixtures of tin and chalcogens (e.g., sulfur (S), selenium (Se), tellurium (Te), polonium (Po), and oxygen (O)), including some species which have a slight excess or deficit of tin. For example, tin selenide, a species of tin-chalcogenide, may be represented by the general formula  $\text{Sn}_{1 \pm x}\text{Se}$ . Though not being limited by a particular stoichiometric ratio between Sn and Se, devices of the present invention typically comprise an  $\text{Sn}_{1 \pm x}\text{Se}$  species where x ranges between about 1 and about 0.

[0022] The term "chalcogenide material," "chalcogenide glass" or "crystalline chalcogenide" is intended to include materials, including glass or crystalline materials, that comprise an element from group VIA (or group 16) of the periodic table. Group VIA elements, also referred to as chalcogens, include sulfur (S), selenium (Se), tellurium (Te), polonium (Po), and oxygen (O). Examples of

chalcogenide materials include GeTe, GeSe, GeS, InSe, and SbSe, all with various stoichiometries.

[0023] The invention is now explained with reference to the figures, which illustrate exemplary embodiments and throughout which like reference numbers indicate like features. FIG. 1 shows an exemplary embodiment of a memory element 100 constructed in accordance with the invention. The element 100 shown in FIG. 1 is supported by a substrate 10. Over the substrate 10, though not necessarily directly so, is a conductive address line 12, which serves as an interconnect for the element 100 shown and a plurality of other similar devices of a portion of a memory array of which the shown element 100 is a part. It is possible to incorporate an optional insulating layer 11 between the substrate 10 and address line 12, and this may be preferred if the substrate 10 is semiconductor-based. The conductive address line 12 can be any material known in the art as being useful for providing an interconnect line, such as doped polysilicon, silver (Ag), gold (Au), copper (Cu), tungsten (W), nickel (Ni), aluminum (Al), platinum (Pt), titanium (Ti), and other materials. Over the address line 12 is a first electrode 16, which is defined within an insulating layer 14, which is also over the address line 12. This electrode 16 can be any conductive material that will not migrate into the layer 18 described below, but is preferably tungsten (W). The insulating layer 14 can be, for example, silicon nitride ( $\text{Si}_3\text{N}_4$ ), a low dielectric constant material, an insulating glass, or an insulating polymer, but is

not limited to such materials. As shown in FIG. 1, an optional insulating layer 11 can be between the address line 12 and the substrate 10.

[0024] The memory element 100 (i.e., the portion which stores information) is formed over the first electrode 16. In the embodiment shown in FIG. 1, a chalcogenide material layer 18, for example, germanium selenide ( $\text{Ge}_x\text{Se}_{100-x}$ ) is provided over the first electrode 16. The germanium selenide may be within a stoichiometric range of about  $\text{Ge}_{33}\text{Se}_{67}$  to about  $\text{Ge}_{60}\text{Se}_{40}$ . The chalcogenide material layer 18 may be between about 100 Å and about 1000 Å thick, e.g., about 300 Å thick. Layer 18 need not be a single layer, but may also be comprised of multiple chalcogenide sub-layers having the same or different stoichiometries. The chalcogenide material layer 18 is in electrical contact with the underlying electrode 16. Alternatively, the memory element 100 can include a germanium comprising layer, which need not comprise a chalcogenide material, in place of the chalcogenide material layer 18.

[0025] Over the chalcogenide material layer 18 (or germanium comprising layer) is a layer of tin-chalcogenide 20, for example tin selenide ( $\text{Sn}_{1+x}\text{Se}$ , where x is between about 1 and 0). It is also possible that other chalcogenide materials may be substituted for selenium, such as sulfur, oxygen, or tellurium. The tin-chalcogenide layer 20 may be about 100 Å to about 400 Å thick; however, its thickness depends, in part, on the thickness of the underlying chalcogenide material layer 18. The ratio of

the thickness of the tin-chalcogenide layer 20 to that of the underlying chalcogenide material layer 18 should be less than about 4:3, e.g., between about 1:3 and about 4:3. As the ratio of the thickness of the tin-chalcogenide layer 20 to that of the underlying chalcogenide material layer 18 decreases (i.e., the tin-chalcogenide layer 20 gets thinner as compared to the chalcogenide material layer 18), the memory element 100 may act more like an OTP cell.

[0026] Still referring to FIG. 1, an optional metal layer 22 is provided over the tin-chalcogenide layer 20, with silver (Ag) being the exemplary metal. This metal layer 22 is about 500 Å thick. Over the metal layer 22 is a second electrode 24. The second electrode 24 can be made of the same material as the first electrode 16, but is not required to be so. In the exemplary embodiment shown in FIG. 1, the second electrode 24 is preferably tungsten (W). The device(s) may be isolated by an insulating layer 26.

[0027] While the invention is not to be bound by any specific theory, it is believed that upon application of a conditioning voltage, metal ions from the tin-chalcogenide layer 20 form one or more conducting channels within the chalcogenide material layer 18. Specifically, the conditioning step comprises applying a potential across the memory element structure of the device 100 such that material from the tin-chalcogenide layer 20 is incorporated into the chalcogenide glass layer 18, thereby forming a conducting channel through the chalcogenide glass

layer 18. Movement of ions from the layer 20 into or out of that conducting channel during subsequent programming forms a conductive pathway, which causes a detectible resistance change across the memory device 100.

[0028] Also, use of a tin-chalcogenide layer, such as layer 20 in this and other embodiments of the invention, offers improved temperature stability for the resulting device 100. For example, devices incorporating a tin-chalcogenide layer in accordance with the invention have been shown to function at temperatures of approximately 200 °C and can have a temperature tolerance in excess of approximately 300 °C, which devices utilizing a chalcogenide glass and silver-containing layers cannot withstand.

[0029] In the exemplary embodiment of FIG. 1, the conditioning voltage alters the resistance state of the chalcogenide layer 18 from a high resistance state to a medium resistance state. A subsequently applied write voltage with a lower energy than that of the conditioning voltage can then program the chalcogenide layer to a lower resistance state. The application of the write voltage causes available metal ions to move into the conducting channels where they remain after the write voltage is removed forming conductive pathways.

[0030] A memory element according to exemplary embodiments of the invention (e.g., memory element 100) operates as an OTP or OTP-like memory element. That is, the memory element 100 can be programmed one time only and

cannot be erased; or it can be programmed and erased a limited number of times (e.g., about 20 or fewer times).

[0031] As noted above, as the ratio of the thickness of the tin-chalcogenide layer 20 to that of the underlying chalcogenide material (or germanium) layer 18 decreases, the memory element 100 may act more like an OTP cell. It is believed that one reason this occurs is because metal, (e.g., silver) from metal layer 22 reacts with the tin from the tin-chalcogenide layer 20. The resultant alloy remains conductive, thereby promoting a low resistance state of the memory element 100.

[0032] FIGS. 2A-2D are cross sectional views of a wafer in various stages of fabrication depicting the formation of the memory element 100 according to an exemplary method embodiment of the invention. No particular order is required for any of the actions described herein, except for those logically requiring the results of prior actions. Accordingly, while the actions below are described as being performed in a general order, the order is exemplary only and can be altered if desired. Although the formation of a single memory element 100 is shown, it should be appreciated that the memory element 100 can be one memory element in an array of memory elements, which can be formed concurrently.

[0033] As shown by FIG. 2A, a substrate 10 is initially provided. As indicated above, the substrate 10 can be semiconductor-based or another material useful as a supporting structure. If desired, an optional insulating layer 11 may be formed over

the substrate 10. The optional insulating layer 11 may be silicon oxide, silicon nitride, or other insulating materials. Over the substrate 10 (and optional insulating layer 11, if desired), the conductive address line 12 is formed by depositing a conductive material, such as doped polysilicon, aluminum, platinum, silver, gold, nickel, titanium, but preferably tungsten. The conductive material is patterned, for instance with photolithographic techniques, and etched to define the address line 12. The conductive material maybe deposited by any technique known in the art, such as sputtering, chemical vapor deposition, plasma enhanced chemical vapor deposition, evaporation, or plating.

[0034] An insulating layer 14 is formed over the address line 12. The insulating layer 14 can be silicon nitride, a low dielectric constant material, or other insulators known in the art, and may be formed by any known method. Preferably, the insulating layer 14 (e.g., silicon nitride) does not allow tin ion migration. An opening 14a in the insulating layer 14 is made, for instance by photolithographic and etching techniques, exposing a portion of the underlying address line 12. A first electrode 16 is formed within the opening 14a, by forming a layer of conductive material over the insulating layer 14 and in the opening 14a. A chemical mechanical polishing (CMP) step is performed to remove the conductive material from over the insulating layer 14. Desirably, the first electrode 16 is formed of tungsten, but any suitable conductive material that will not migrate into the layer 18 can be used.

[0035] As shown in FIG. 2B, a chalcogenide material layer 18 is formed over the first electrode 16 and insulating layer 14. Formation of the chalcogenide material layer 18 may be accomplished by any suitable method, for example, by sputtering. The chalcogenide material layer 18 is formed, for example, to a thickness between about 100 Å and about 1000 Å, e.g., about 300 Å thick.

[0036] The memory element 100 can instead include a germanium comprising layer, which need not comprise a chalcogenide material, in place of chalcogenide material layer 18. In such a case, the germanium comprising layer may be formed by any known technique, for example, by sputtering.

[0037] A tin-chalcogenide layer 20 is formed over the chalcogenide material layer 18. The tin-chalcogenide layer 20 can be formed by any suitable method, e.g., physical vapor deposition, chemical vapor deposition, co-evaporation, sputtering, among other techniques. The tin-chalcogenide layer 20 is formed to a thickness of, for example, between about 100 Å to about 400 Å thick; however, its thickness depends, in part, on the thickness of the underlying chalcogenide material layer 18. The ratio of the thickness of the tin-chalcogenide layer 20 to that of the underlying chalcogenide material layer 18 is, desirably, less than about 4:3, e.g., between about 1:3 and about 4:3.

[0038] Optionally, a metal layer 22 is formed over the tin-chalcogenide layer 20. The metal layer 22 is preferably silver (Ag), or at least contains silver, and is

formed to a preferred thickness of about 300 Å to about 500 Å. The metal layer 22 may be deposited by any technique known in the art.

[0039] A conductive material is deposited over the metal layer 22 to form a second electrode 24. Similar to the first electrode 16, the conductive material for the second electrode 24 may be any material suitable for a conductive electrode. In one exemplary embodiment the second electrode 24 is tungsten.

[0040] Referring to FIG. 2C, a layer of photoresist 30 is deposited over the second electrode 24 layer, masked and patterned to define a stack 33 of the memory element 100. An etching step is used to remove portions of the layers 18, 20, 22, 24, with the insulating layer 14 used as an etch stop, leaving stack 33 as shown in FIG. 2C. The photoresist 30 is removed, leaving the structure shown in FIG. 2D.

[0041] An insulating layer 26 is formed over the stack 33 and insulating layer 14 to achieve the structure shown in FIG. 1. This isolation step can be followed by the forming of connections from the defined memory cell electrodes 16, 24 to other circuitry of the integrated circuit (e.g., logic circuitry, sense amplifiers, etc.) of which the memory element 100 is a part.

[0042] FIG. 3 shows a memory element 300 according to an exemplary embodiment of the invention. For the memory element 300, the address line 12 can

also serve as the first electrode 16. In such a case, the formation of the separate first electrode 16 is omitted.

[0043] FIG. 4 illustrates a memory element 400 according to another exemplary embodiment of the invention. The memory element 400 is predominantly defined by the position of the second electrode 24. The layers 18, 20, 22 of the memory element 400 are blanket layers formed over a combined address line and electrode structure 12/16. Alternatively, a first electrode 16 that is separate from an underlying address line 12 can be used, as with memory element 100 (FIG. 1). In FIG. 4, the second electrode 24 is shown perpendicular to the plane of the page and the address line and electrode structure 12/16 is shown parallel to the plane of the page.

[0044] The location where the second electrode 24 is directly over the address line and electrode structure 12/16 defines the position of the conductive pathway formed during operation of the memory element 400. In this way, the second electrode 24 defines the location of the memory element 400.

[0045] FIG. 5 represents a memory element 500 according to another exemplary embodiment of the invention. In the illustrated memory element 500, the chalcogenide material (or germanium), tin-chalcogenide, and optional metal layers 18, 20, 22 are formed in a via 28. The via 28 is formed in an insulating layer 14 over an address line and electrode structure 12/16. The layers 18, 20, as well as the second

electrode 24, are conformally deposited over the insulating layer 14 and within the via 28. The layers 18, 20, 22, 24 are patterned to define a stack over the via 28, which is etched to form the completed memory element 500. Alternatively, a first electrode 16 that is separate from the underlying address line 12 can be used. Such a separate electrode 16 can be formed in the via 28 prior to the formation of the chalcogenide material (or germanium) layer 18.

[0046] The embodiments described above refer to the formation of only a few possible resistance variable memory element structures in accordance with the invention, which may be part of a memory array. It must be understood, however, that the invention contemplates the formation of other memory structures within the spirit of the invention, which can be fabricated as a memory array and operated with memory element access circuits.

[0047] FIG. 6 illustrates a processor system 600 which includes a memory circuit 648, e.g., a memory device, which employs resistance variable memory elements (e.g., elements 100, 300, 400, and/or 500) according to the invention. The processor system 600, which can be, for example, a computer system, generally comprises a central processing unit (CPU) 644, such as a microprocessor, a digital signal processor, or other programmable digital logic devices, which communicates with an input/output (I/O) device 646 over a bus 652. The memory circuit 648

communicates with the CPU 644 over bus 652 typically through a memory controller.

[0048] In the case of a computer system, the processor system 600 may include peripheral devices such as a floppy disk drive 654 and a compact disc (CD) ROM drive 656, which also communicate with CPU 644 over the bus 652. Memory circuit 648 is preferably constructed as an integrated circuit, which includes one or more resistance variable memory elements, e.g., elements 100 (FIG. 1). If desired, the memory circuit 648 may be combined with the processor, for example CPU 644, in a single integrated circuit.

[0049] The above description and drawings are only to be considered illustrative of exemplary embodiments, which achieve the features and advantages of the present invention. Modification and substitutions to specific process conditions and structures can be made without departing from the spirit and scope of the present invention. Accordingly, the invention is not to be considered as being limited by the foregoing description and drawings, but is only limited by the scope of the appended claims.

## CLAIMS

[0050] What is claimed as new and desired to be protected by Letters Patent of the United States is:

1. A memory device comprising:
  - a first electrode;
  - a second electrode;
  - a material layer of a chalcogenide or semi-metal material between the first electrode and the second electrode; and
  - a tin-chalcogenide layer between the chalcogenide material layer and the second electrode, a ratio of the thickness of the tin-chalcogenide layer to the thickness of the material layer being less than about 4:3.
2. The memory device of claim 1, wherein the material layer comprises a chalcogenide glass.
3. The memory device of claim 1, wherein the material layer comprises a crystalline chalcogenide material.
4. The memory device of claim 1, wherein the material layer is a layer of germanium.
5. The memory device of claim 1, wherein the material layer comprises germanium telluride.
6. The memory device of claim 1, wherein the material layer comprises  $\text{Ge}_x\text{Se}_{100-x}$ .

7. The memory device of claim 5, wherein the  $\text{Ge}_x\text{Se}_{100-x}$  has a stoichiometry between about  $\text{Ge}_{33}\text{Se}_{67}$  to about  $\text{Ge}_{60}\text{Se}_{40}$ .
8. The memory device of claim 1, further comprising a metal layer between the tin-chalcogenide layer and the second electrode.
9. The memory device of claim 1, wherein the metal layer comprises silver.
10. The memory device of claim 1, wherein said tin-chalcogenide layer comprises  $\text{Sn}_{1+x}\text{Se}$ , where x is between about 1 and about 0.
11. The memory device of claim 1, wherein the tin-chalcogenide layer comprises layer comprises tin-telluride.
12. The memory device of claim 1, wherein at least one of the first and second electrodes comprise tungsten.
13. The memory device of claim 1, wherein the second electrode is over the metal-containing layer and comprises silver.
14. The memory device of claim 1, wherein the material layer and the tin-chalcogenide layer are provided within a via in an insulating layer.
15. The memory device of claim 1, wherein the material layer and the tin-chalcogenide layer are blanket layers over a substrate, and wherein the second electrode defines the location of a memory element.
16. The memory device of claim 1, wherein a thickness of the material layer and a thickness of the tin-chalcogenide layer are such that the memory device is programmable a limited number of times.

17. The memory device of claim 1, wherein a thickness of the material layer and a thickness of the tin-chalcogenide layer are such that once the memory device is programmed, it cannot be erased.
18. The memory device of claim 1, wherein a thickness of the material layer is about 300 Å and a thickness of the tin-chalcogenide layer is between about 100 Å to about 400 Å.
19. The memory device of claim 18, further comprising a metal layer between the tin-chalcogenide layer and the second electrode, the metal layer having a thickness of about 300 Å to about 500 Å.
20. The memory device of claim 1, wherein a thickness of the material layer is between about 100 Å and about 1000 Å.
21. The memory device of claim 1, wherein the ratio of the thickness of the tin-chalcogenide layer to the thickness of the material layer is between about 1:3 and about 4:3.
22. A memory device, comprising:
  - a substrate;
  - a conductive address line over the substrate;
  - a first electrode over the conductive address line;
  - a crystalline chalcogenide material layer over the first electrode;
  - a tin-chalcogenide layer over the crystalline chalcogenide material layer;
  - and

- a second electrode over the metal-containing layer.
23. The memory device of claim 22, further comprising a metal layer between the tin-chalcogenide layer and the second electrode.
24. The memory device of claim 22, wherein a thickness of the crystalline chalcogenide material layer and a thickness of the tin-chalcogenide layer are such that the memory device is programmable a limited number of times.
25. The memory device of claim 22, wherein the ratio of the thickness of the tin-chalcogenide layer to the thickness of the crystalline chalcogenide material layer is less than about 4:3.
26. A memory device, comprising:
- a substrate;
  - a conductive address line over the substrate;
  - a first electrode over the conductive address line;
  - a germanium layer over the first electrode;
  - a tin-chalcogenide layer over the germanium layer; and
  - a second electrode over the metal-containing layer.
27. The memory device of claim 26, further comprising a metal layer between the tin-chalcogenide layer and the second electrode.

28. The memory device of claim 26, wherein a thickness of the germanium layer and a thickness of the tin-chalcogenide layer are such that the memory device is programmable a limited number of times.
29. The memory device of claim 26, wherein the ratio of the thickness of the tin-chalcogenide layer to the thickness of the germanium layer is less than about 4:3.
30. A processor system, comprising:
  - a processor; and
  - a memory device configured to be programmable a limited number of times, the memory device comprising:
    - a first electrode;
    - a second electrode;
    - a material layer of a chalcogenide or semi-metal material between the first electrode and the second electrode; and
    - a tin-chalcogenide layer between the chalcogenide material layer and the second electrode, a ratio of the thickness of the tin-chalcogenide layer to the thickness of the material layer being less than about 4:3.
31. The processor system of claim 30, wherein the material layer comprises a chalcogenide glass.
32. The processor system of claim 30, wherein the material layer comprises a crystalline chalcogenide material.

33. The processor system of claim 30, wherein the material layer is a layer of germanium.
34. The processor system of claim 30, further comprising a metal layer between the tin-chalcogenide layer and the second electrode.
35. The processor system of claim 34, wherein the metal layer comprises silver.
36. A method of forming a memory device, the method comprising the acts of:
  - providing a substrate;
  - forming a first electrode over the substrate;
  - forming a second electrode over the substrate;
  - forming a material layer of a chalcogenide or semi-metal material between the first electrode and the second electrode; and
  - forming a tin-chalcogenide layer between the chalcogenide material layer and the second electrode, the material layer and the tin-chalcogenide layer formed such that a ratio of the thickness of the tin-chalcogenide layer to the thickness of the material layer is less than about 4:3.
37. The method of claim 36, wherein forming the material layer comprises forming a layer comprising a chalcogenide glass.
38. The method of claim 36, wherein forming the material layer comprises forming a layer comprising a crystalline chalcogenide material.

39. The method of claim 36, wherein forming the material layer comprises forming a layer of germanium.
40. The method of claim 36, wherein forming the material layer comprises forming a layer comprising germanium telluride.
41. The method of claim 36, wherein forming the material layer comprises forming a layer comprising  $\text{Ge}_x\text{Se}_{100-x}$ .
42. The method of claim 41, wherein the  $\text{Ge}_x\text{Se}_{100-x}$  is formed having a stoichiometry between about  $\text{Ge}_{33}\text{Se}_{67}$  to about  $\text{Ge}_{60}\text{Se}_{40}$ .
43. The method of claim 36, further comprising forming a metal layer between the tin-chalcogenide layer and the second electrode.
44. The method of claim 36, wherein forming the metal layer comprises forming a silver comprising layer.
45. The method of claim 36, wherein forming the tin-chalcogenide layer comprises forming a layer of  $\text{Sn}_{1+x}\text{Se}$ , where x is between about 1 and about 0.
46. The method of claim 36, wherein forming the tin-chalcogenide layer comprises forming a layer comprising tin-telluride.
47. The method of claim 36, wherein at least one of the first and second electrodes are formed comprising tungsten.
48. The method of claim 36, wherein acts of forming the material layer and the tin-chalcogenide layer comprise forming the material layer and the tin-

chalcogenide layer having thicknesses such that the memory device is programmable a limited number of times.

49. The method of claim 36, wherein acts of forming the material layer and the tin-chalcogenide layer comprise forming the material layer and the tin-chalcogenide layer having thicknesses such that once the memory device is programmed, it cannot be erased.
50. The method of claim 36, wherein the material layer is formed having a thickness of about 300 Å and the tin-chalcogenide layer is formed having a thickness between about 100 Å to about 400 Å.
51. The method of claim 50, further comprising forming a silver layer between the tin-chalcogenide layer and the second electrode, the silver layer formed having a thickness of about 300 Å to about 500 Å.
52. The method of claim 36, wherein the material layer is formed having a thickness between about 100 Å and about 1000 Å.
53. The method of claim 36, wherein the tin-chalcogenide layer and the material layer are formed such that the ratio of the thickness of the tin-chalcogenide layer to the thickness of the material layer is between about 1:3 and about 4:3.
54. The method of claim 36, further comprising providing an address line electrically connected with the first electrode.

55. The method of claim 36, wherein the act of forming the first electrode comprises forming a combined address line/electrode structure.
56. The method of claim 36, wherein the acts of forming the material layer and the tin-chalcogenide layer comprise blanket-depositing the forming the material layer and the tin-chalcogenide layer.
57. The method of claim 56, further comprising the act of etching forming the material layer and the tin-chalcogenide layer to form a vertical stack.
58. The method of claim 36, further comprising forming a via within an insulating layer, wherein the acts of forming the material layer and the tin-chalcogenide layer comprise forming the material layer and the tin-chalcogenide layer within the via.
59. A method of forming a memory element, the method comprising the acts of:
  - providing a substrate;
  - forming a conductive layer over the substrate;
  - forming a first electrode over the substrate;
  - forming a first insulating layer over the conductive layer and the substrate;
  - forming an opening in the first insulating layer to expose a portion of the conductive layer in the opening;

forming a material layer in the opening and over the first electrode, the material layer being a chalcogenide material or germanium;  
forming a tin-chalcogenide layer in the opening and over the material layer, the material layer and the tin-chalcogenide layer formed such that a ratio of the thickness of the tin-chalcogenide layer to the thickness of the material layer is less than about 4:3;  
forming a second electrode layer over the tin-chalcogenide layer;  
providing a mask over the second electrode layer;  
etching the material layer, the tin-chalcogenide layer, and the second electrode to form a stack.

60. The method of claim 59, wherein the act of forming the material layer comprises forming a chalcogenide glass layer.
61. The method of claim 59, wherein the act of forming the material layer comprises forming a crystalline chalcogenide material layer.
62. The method of claim 59, wherein the act of forming the material layer comprises forming a germanium layer.
63. The method of claim 59, wherein acts of forming the material layer and the tin-chalcogenide layer comprise forming the material layer and the tin-chalcogenide layer having thicknesses such that the memory device is programmable a limited number of times.

64. A method of forming a memory device, the method comprising the acts of:
- providing a substrate;
  - forming a first electrode over the substrate;
  - forming a second electrode over the substrate;
  - forming a crystalline chalcogenide material layer between the first electrode and the second electrode;
  - forming a tin-chalcogenide layer between the chalcogenide material layer and the second electrode; and
  - forming a silver layer between the tin-chalcogenide layer and the second electrode.
65. The method of claim 64, wherein the crystalline chalcogenide material layer and the tin-chalcogenide layer are formed having thicknesses such that the memory device is programmable a limited number of times.
66. The method of claim 64, wherein the tin-chalcogenide layer and the crystalline chalcogenide material layer are formed such that the ratio of the thickness of the tin-chalcogenide layer to the thickness of the crystalline chalcogenide material layer is less than about 4:3.
67. A method of forming a memory device, the method comprising the acts of:
- providing a substrate;

- forming a first electrode over the substrate;
- forming a second electrode over the substrate;
- forming a germanium layer between the first electrode and the second electrode;
- forming a tin-chalcogenide layer between the chalcogenide material layer and the second electrode; and
- forming a silver layer between the tin-chalcogenide layer and the second electrode.
68. The method of claim 67, wherein the germanium layer and the tin-chalcogenide layer are formed having thicknesses such that the memory device is programmable a limited number of times.
69. The method of claim 67, wherein the tin-chalcogenide layer and the germanium layer are formed such that the ratio of the thickness of the tin-chalcogenide layer to the thickness of the germanium layer is less than about 4:3.