WHAT IS CLAIMED IS:

1. A wafer comprising:

a substrate including a first region and a second region that do not overlap each other;

a first chip unit and a second chip unit each arranged on the substrate;

a first electrode and a second electrode each electrically connected to the first chip unit; and

a third electrode and a fourth electrode each electrically connected to the second chip unit,

wherein the first electrode and the third electrode are arranged in the first region,

the second electrode and the fourth electrode are arranged in the second region, and

the first region is independent of a region in which the first chip unit and the second chip unit are provided.

2. The wafer according to claim 1, further comprising:

a fifth electrode configured to electrically connect the first electrode and the first chip unit;

a sixth electrode configured to electrically connect the second electrode and the first chip unit;

a seventh electrode configured to electrically connect the third electrode and the second chip unit; and

an eighth electrode configured to electrically connect the fourth electrode and the second chip unit.

3. The wafer according to claim 2, wherein

the first region and the second region are included in a region of the substrate viewed from a first surface side of the substrate.

4. The wafer according to claim 3, further comprising:

a first insulating layer arranged between (i) the first electrode, the second electrode, the third electrode, and the fourth electrode and (ii) the fifth electrode, the sixth electrode, the seventh electrode, and the eighth electrode,

wherein the first insulating layer contains polyimide.

5. The wafer according to claim 2, wherein

the first region is included in a region of the substrate viewed from a first surface side of the substrate, and

the second region is included in a region of the substrate viewed from a second surface side of the substrate opposing the first surface.

6. The wafer according to claim 5, further comprising:

a second insulating layer including a first portion arranged between (i) the first electrode and the third electrode and (ii) the substrate, a second portion arranged between (iii) the second electrode and the fourth electrode and (iv) the fifth electrode, the sixth electrode, the seventh electrode, and the eighth electrode, and a third portion arranged on a side surface of the substrate and connecting the first portion and the second portion to each other,

wherein the second insulating layer contains polyimide.

7. The wafer according to claim 1, wherein

the first electrode, the second electrode, the third electrode, and the fourth electrode each contains conductive carbon, conductive rubber, or mercury.

8. The wafer according to claim 1, wherein

the first electrode, the second electrode, the third electrode, and the fourth electrode each has a plate structure, a wire structure, a ball structure, a spring structure, or a porous structure.

9. The wafer according to claim 1, wherein

the first electrode and the third electrode are for electric power supply, and

the second electrode and the fourth electrode are for signal communication.