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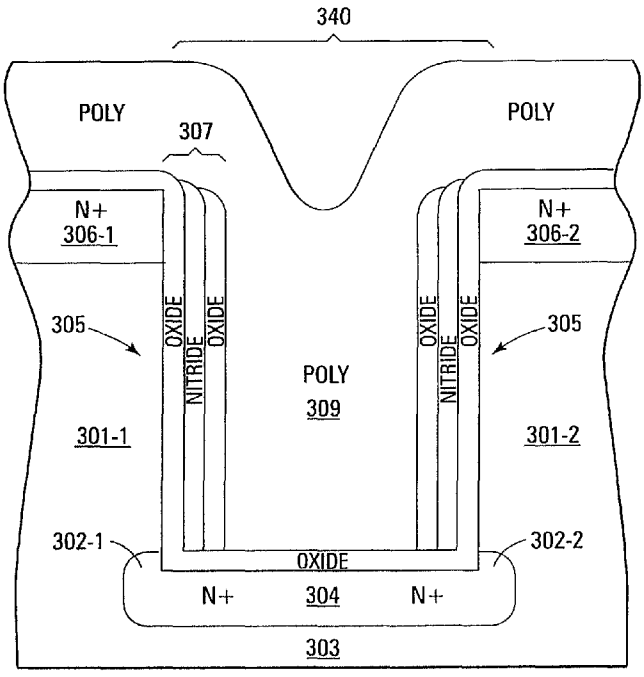
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[Continued on next page]

(54) Title: NROM DEVICE



(57) Abstract: An array of NROM flash memory cells configured to store at least two bits per four F^2. Split vertical channels are generated along each side of adjacent pillars. A single control gate is formed over the pillars and in the trench between the pillars. The split channels can be connected by an n+ region at the bottom of the trench or the channel wrapping around the trench bottom. Each gate insulator is capable of storing a charge that is adequately separated from the other charge storage area due to the increased channel length.

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