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PATENT SPECIFICATION 953,917

DRAWINGS ATTACHED.

953,917

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COMPLETE SPECIFICATION.

Improvements relating to Semiconductor Circuits.

We, TEXAS INSTRUMENTS INCORPORATED, of 6000 Lemmon Avenue, Dallas, Texas, United States of America, a Corporation organized and existing under the laws of the State of Delaware, United States of America, do hereby declare the invention, for which we pray that a patent may be granted to us, and the method by which it is to be performed, to be particularly described in and by the following statement:—

This invention relates to semiconductor circuits.

Many methods and techniques or miniaturizing electron circuits have been proposed in the past. At first, most of the effort was spent upon reducing the size of the components and packing them more closely together. Work directed toward reducing component size is still going on but has nearly reached a limit. Other efforts have been made to reduce the side of electronic circuits such as by eliminating the protective coverings from components, by using more or less conventional techniques to form components of a complete circuit on a single substrate, and by providing the components with a uniform size and shape to permit closer spacings in the circuit packaging therefor.

All of these methods and techniques require a very large number or variety of operations in fabricating a complete circuit. For example, of all circuit components, resistors are usually considered the most simple to form, but when adapted for miniaturization by conventional techniques, fabrication requires at least the following steps:

a. Formation of the substrate.
b. Preparation of the substrate.
c. Application of terminations.
d. Preparation of resistor material.
e. Application of the resistor material.
f. Heat treatment of the resistor material.
g. Protection of stabilization of the resistor.

Capacitors, transistors and diodes when adapted for miniaturization each require at least as many steps in the fabrication thereof. Unfortunately, many of the steps required are not compatible. A treatment that is desirable for the protection of a resistor may damage another element formed on the same substrate, such as a capacitor or a transistor, and as the size of the complete circuit is reduced, such conflicting treatments, or interactions, become of increasing importance. Interactions may be minimized by forming the components separately and then assembling them into a complete package, but the very act of assembly may cause damage to the more sensitive components.

Because of the large number of operations required, control over miniaturized circuit fabrication becomes very difficult. To illustrate, many raw materials must be evaluated and controlled even though they may not be well understood. Further, many testing operations are required and, even though a high yield may be obtained for each operation, so many operations are required that the over-all yield is often quite low. In service, the reliability of a circuit produced by methods of such complexity may also be quite low due to the tremendous number of controls required. Additionally, the separate formation of individual components requires individual terminations for each component. These terminations may eventually become as small as a dot of conductive paint. However, they still account for a large fraction of the usable area or volume of the circuit and may become an additional cause of circuit failure or rejection due to misalignment.

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In contrast to the approaches to miniaturization that have been made in the past, the present invention has resulted from the concept for miniaturization disclosed in the Specification of our co-pending Patent Application No. 3633/60 (Serial No. 945,734).

In the Specification of our co-pending Application aforesaid, a single crystal of semiconductor material exhibiting one type of conductivity, either N-type or P-type has certain regions thereof processed by adding significant impurity materials thereto so as to form certain kinds of circuit components. Other regions of the basic semiconductor crystal may inherently perform functions of certain other circuit components, such as resistors.

It is an object of this invention to provide a miniaturized semiconductor circuit device which can function as one-half of a bistable transistor multivibrator circuit.

The present invention is a semiconductor circuit comprising a substrate, a plurality of semiconductor regions in or on one and the same face and spaced from the opposite face of said substrate, said regions being electrically isolated from one another through said substrate, certain of said regions being adapted to provide the electrical properties of a transistor having a base, emitter and collector, and first, second and third resistors, said first resistor having one end thereof ohmically connected to said collector, said second and third resistors each having one end thereof ohmically connected to said base, and ohmic contacts to said collector and said emitter and to the other ends of said first, second and third resistors.

The present invention is also a bistable circuit comprising two members connected together to form a single circuit and each including a substrate having therein or thereon a plurality of semiconductor regions together providing the electrical properties of a transistor, a capacitive semiconductor diode and a portion of semiconductor material with a substantial resistance.

The present invention is also a bistable circuit including two semiconductor members connected together and built up into a single circuit, each member including a transistor, a capacitive semiconductor diode and a portion of semiconductor material with a substantial resistance.

In the present invention, all components of a bistable circuit subcombination are preferably fabricated within a body of semiconductor material by using the techniques described in the Specification of said co-pending Patent Application together with certain other techniques. All components of this circuit are integrated into the body of semiconductor material and actually constitute portions thereof.

Of importance to this invention is the concept of shaping. As described in detail in the Specification of said co-pending Patent Application, this shaping concept makes it possible in a circuit to obtain the necessary isolation between components and to define the components or, stated differently, to limit the area which is utilized for a given component. Shaping may be accomplished in a given circuit in one or more of several different ways. These various ways include actual removal of portions of the semiconductor material, specialized configurations of the semiconductor material such as rectangular, "L"-shaped, "U"-shaped, etc., selective conversion of intrinsic semiconductor material by diffusion of impurities thereinto to provide low resistivity paths for current flow and selective conversion of semiconductor material of one conductivity type to conductivity of the opposite type wherein the P-N junction thereby formed acts as a barrier to current flow. In any event, the effect of shaping is to direct and/or confine paths for current flow thus permitting the fabrication of circuits which could not otherwise be obtained in a single wafer of semiconductor material. As a result, the final circuit is arranged in essentially planar form. It is possible to shape the wafer during processing and to produce by diffusion the various circuit elements in a desired and proper relationship.

Other and further objects of the present invention will become more readily apparent from the following detailed description of a preferred embodiment of the present invention when taken in conjunction with the accompanying drawings, in which:—

Figure 1 is a conventional schematic line diagram of the bistable multivibrator circuit subcombination which may be fabricated within a body of semiconductor material in accordance with the present invention;

Figure 2 is a pictorial diagram illustrating the miniaturized semiconductor bistable multivibrator circuit subcombination of the present invention;

Figures 3, 4, 5 and 6 are cross sectional views along lines 3—3, 4—4, 5—5 and 6—6, respectively, of Figure 2 of portions of the semiconductor multivibrator circuit subcombination shown in Figure 2.

Referring now to Figure 1, there is shown a conventional schematic diagram of the multivibrator subcombination circuit which is fabricated from semiconductor material. The active element T_1 is an N-P-N transistor whose collector electrode 12 is connected to a positive potential through resistor R_1. Emitter electrode 14 is connected to another source of lesser positive potential, to which is also connected the cathode electrode 24 of diode D_2. Base electrode 16 of transistor T_1 is connected to a source of negative

potential through a resistor R_3. Base electrode 16 is further connected to anode electrode 18 of diode D_1 and to one terminal of resistor R_2. Plate 26 represents distributed capacitance C_1 which is essentially in parallel with all of resistor R_2 and a portion of resistor R_3. Cathode electrode 20 of diode D_1 is connected to one plate 30 of capacitor C_2 and also to anode electrode 22 of diode D_2. Plate 32 of capacitor C_2 is connected to a trigger input terminal I_1.

The circuit shown in Figure 1 represents but one-half of a bistable multivibrator circuit, sometimes called an Eccles-Jordan flip-flop circuit. To form the complete flip-flop circuit, a second circuit exactly like that in Figure 1 is connected to the circuit of Figure 1 in the following manner. The OUT lead from collector electrode 12 in Figure 1 is connected to the CC terminal of the second circuit. The CC terminal of Figure 1 is connected to the OUT lead of the second circuit. In the complete bistable multivibrator circuit, then, the collector of one transistor is cross-coupled to the base of the other transistor through the R-C circuit R_2 and C_1, and vice versa.

The operation of the circuit shown in Figure 1 may best be understood if it is considered to be within a complete flip-flop circuit as described in the preceding paragraph. If transistor T_1 is in its conducting state, a negative pulse at input I_1 coupled through C_2 and buffer diode D_1 causes the base 16 potential to drop below that of emitter 14, thus attempting to cut off T_1. The voltage at collector 12 then begins to rise and thereby causes the cross-coupled base electrode of the non-conducting transistor in the second circuit to rise in potential above that of its associated emitter. This previously non-conducting transistor therefore begins to conduct, while transistor T_1 in Figure 1 becomes completely cut off due to the transmission of the fall in potential of the collector of the previously non-conducting transistor to base 16 of transistor T_1 through resistor R_2 and capacitor C_1. A similar operation would occur in order to again change the state of the bistable multivibrator circuit, except that the trigger pulse would be applied to the other now conducting transistor. Capacitor C_1 functions to increase the switching speed of the circuit.

The present invention is shown in Figure 2 in which the multivibrator subcombination of Figure 1 is fabricated or integrated within associated sections of a single crystal body of semiconductor material. In the preferred form of the present invention, the starting material is a wafer or semiconductor material of N-type conductivity and about 0.2 inch by 0.08 inch by about 0.003 inch thick. This wafer is attached to a ceramic plate which is slightly larger in area and thick enough to provide suitable support for the semiconductor material. The semiconductor material is then subjected to a "form etching" process as described in the Specification of our co-pending Patent Application No. 16066/60 (Serial No. 945,735) entitled "Process for etching semiconductors in the fabrication of miniature semiconductor networks comprising a single semiconductor block", filed on 6th May, 1960.

The "form etching" process results in four associated sections of an N-type semiconductor material in the form of wafer strips 36, 38, 40 and 42 attached to supporting substrate 34 in the configuration as shown in Figure 2. Actually, it is quite often desirable, although not absolutely necessary to perform certain diffusion, material deposition and etching steps before the "form etching" treatment. In fact, although the formation processes for producing the several circuit components within the semiconductor material are described individually for each wafer strip, for the sake of clarity, it has been found most expedient to perform as many of the component formation steps of diffusion, material deposition and etching on the various regions of the single starting wafer before it is divided into the several wafer strips in the "form etching" process. Metal contact strips 44, 46, 48, 50, 52, 54, 56 and 58 are also placed on substrate 34 in the manner also described in the Specification of out aforesaid co-pending Patent Application No. 3633/60 (Serial No. 945,734) for the placing of contacts, and are used to provide input and output terminals for the signal and bias voltages shown in Figure 1. It should be noted that all of the above-identified contact strips, with the exception of 46, extend beneath various regions of wafer strips 36, 38, 40 and 42, as shown by the dashed lines in Figure 2, so as to make ohmic connections thereto. Contact strip 46 does not make a direct ohmic contact to any of the above-identified semiconductor wafers. However, contact strip 46 is connected to one of the fabricated circuit components which is contained within a region of wafer strip 38, which subsequently will be discussed. Contact strips 44 and 54 are not used to introduce or remove signals from the semiconductor circuit on substrate 34. However, they do make ohmic contacts with regions in their associated wafers 36 and 38. Therefore, they may be used as internal terminal posts when connecting the components found within the wafer strips.

The fabrication of circuit components within wafer 42 will now be described, with particular reference to Figure 3. For the purpose of this and subsequent paragraphs, the regions of a wafer strip have been marked in Figure 2 with symbols representative of the circuit element functions that are

performed therein which correspond to the circuit components found in Figure 1. Wafer strip 42 is formed in the shape of an "L" having a vertical and a horizontal leg. The particular dimensions of wafer 42 are designed so that the sum of the effective bulk resistances of the semi-conductor material of the two legs is equal to the desired value of resistor R_1 which is shown in Figure 1. This resistance may be calculated from the following equation:—

$$R = \rho L/A$$

where L is the sum of the active lengths of the two legs in centimetres, A is the cross-sectional area of the wafer, and ρ is the resistivity in ohm-centimetres of the N-type semiconducting material of which wafer 42 is made.

The left-hand region (in the drawing) of the horizontal leg of wafer strip 42 is processed so as to form transistor T_1 therein. Figure 3 shows a cross-sectional view of the said left-hand region which shows how the transistor is fabricated. A P-region 78 is formed within this region of wafer 42 in any well-known manner, such as by the vapour diffusion of significant impurities into the strip so as to form a rectifying P-N junction therein. A second N-region 76 is formed in wafer strip 42 by diffusion over the P-region 78 so as to form a second rectifying P-N junction between regions 76 and 78. The wafer strip 42 is then subjected to an etching treatment, using well known transistor techniques, to remove both diffused layers 76 and 78 from the wafer strip except in the circled area on the left-hand region of the wafer strip. The regions 76, 78 and the left-hand region of wafer 42 which lies beneath them now comprise an N-P-N transistor. In the particular embodiment shown in Figures 2 and 3, region 76 is the emitter of this transistor, the region 78 is the base region, and N-region of wafer 42 underlying region 76 and 78 is the collector of the transistor. A metal emitter electrode or contact 14 is attached to region 76, such as by vacuum deposition and alloying, so as to form an ohmic contact for the emitter, and a metal base electrode 16 is applied in the same manner and alloyed through region 76 so as to provide ohmic contact to base region 78 and rectifying contact to region 76. The junction between contact 16 and region 76 may be etched away if desired as customary in the art in the formation of double diffused transistor such as is constituted by T_1. Contact strips 50 and 58 further contact in ohmic fashion the wafer strip 42 at the regions shown in Figure 2.

The construction of diode D_2 in wafer strip 40 will now be described, with particular reference to Figure 4. A P-region 80 is created in wafer strip 40, preferably in the same manner and at the same time the P-region 78 is formed in wafer strip 42, thus forming a rectifying P-N junction, the junction of D_2. A metal contact 22 is ohmically connected to region 80 just as was contact 14 to T_1. Thus, it is seen that a diode having an anode 80 and a cathode 40 has been fabricated from the original single body crystal of N-type semiconductor material. This diode corresponds to D_2 in Figure 1. Contact strip 56 further ohmically contacts wafer 40 to form cathode electrode 24 as shown in Figure 2.

The construction of the components of wafer strip 36 will now be described, with particular reference to Figure 5. In the particular embodiment as shown in Figure 2, wafer 36 is in the shape of an "L" with a vertical and a horizontal leg. The length and cross-sectional area of the horizontal leg is calculated so as to furnish the desired resistance of resistor R_3 found in Figure 1. The length and cross-sectional area of the vertical leg is such as to provide the desired resistance of resistor R_2. Furthermore, as shown in Figure 1, a distributed capacitance C_1 is connected in parallel with resistor R_3 and a portion of R_2. Figure 5 shows a cross-sectional view of the actual construction of capacitor C_1 in the fabricated circuit of Figure 2 which utilizes the inherent capacitance of a P-N junction. The vertical leg and a portion of the horizontal leg of wafer 36 provide one plate of this capacitor. On these portions of these legs is created a region 62 of P-type semiconductor material so as to form a P-N rectifying junction therebetween. The P-type region 62 may be created by diffusion in the same manner as and preferably simultaneously with, region 80 of wafer strip 40 and region 78 of wafer strip 42. A metallic plate 26 which may be a vapor deposited layer of gold, aluminum or other metal, is alloyed to P-region 62 to make ohmic contact therewith. This technique of fabricating a capacitor on a single body of semiconductor material is described in the Specification of our aforementioned co-pending Patent Application No. 3633/60 (Serial No. 945,734). Contact strip 52 makes contact only with the lowest portion of the vertical leg of wafer 36 as shown by dashed lines in Figure 2, this lower portion being equivalent to the upper terminal of resistor R_2 shown in Figure 1. Thus, the vertical leg and a portion of the horizontal leg of wafer section 36 has been processed so as to form a parallel R-C circuit. It will be noted that the metallic layer 26 of capacitor C1, which is actually the capacitance of the reverse biased P-N junction between P-layer 62 and the N-type region of wafer strip 36, does not appear to be connected directly to the circuit at any

point. However, to those skilled in the art it will be apparent that such construction is equivalent to a capacitance connected in parallel with R_2. Contact strips 44 and 48 are also ohmically connected to wafer 36 at the regions shown in Figure 2.

The construction of the components of wafer strip 38 will now be described with particular reference to Figure 6. Diode D_1, which is shown in Figure 1, is fabricated into the left-hand region of wafer strip 38 in a manner shown by Figure 4, above described. Capacitor C_2 is fabricated into the remaining right-hand region of wafer strip 38 in a manner shown by Figure 6, which is a cross-sectional view. This region of wafer strip 38 provides one plate of this capacitor. Formed onto this region is a layer 60 which provides a dielectric layer for capacitor C_2. As oxide of silicon has been found to be a suitable material for this dielectric layer, as explained in the Specification of our aforementioned co-pending Application No. 3633/60 (Serial No. 945,734). A plate 32 forms the other plate and is provided by evaporating a conductive material onto layer 60. Gold and aluminum have been found to be satisfactory materials for plate 32. Contact strip 54 ohmically contacts wafer strip 38 at its left-hand portion and it serves as an internal connecting point.

It now remains to connect the various circuit components found in each of the above-described wafer strips of sections into the completed circuit diagramed in Figure 1. Wire connectors 64, 66, 68, 70 and 72 perform this function. Base electrode 16 of transistor T_1 is connected by connector 66 to contact strip 44 and thus to the common terminal of resistors R_2 and R_3. Also, the anode electrode 18 of diode D_1 is connected to this latter junction by connector 68. The emitter electrode 14 of the transistor is connected to contact strip 56 by connector 72 and thus to the cathode of diode D_2 which is formed by the wafer strip 40. The anode electrode 22 of diode D_2 is connected to contact strip 54 by the connector 70 and thus to the cathode of diode D_1 which consists of the left-hand region of wafer strip 38. Furthermore, the remaining right-hand region of wafer strip 38 forms one plate 30 (see Figure 7) of capacitor C_2. The other plate 32 of capacitor C_2 is connected by wire 64 to contact strip 46.

A brief explanation of the signal and bias voltage input to the fabricated circuit of Figure 2 will now be given, corresponding to those shown in Figure 1. Positive potential is applied by contact strip 50 to the left-hand region of the horizontal leg of wafer strip 42, corresponding to the collector of transistor T_1, through the vertical and horizontal legs of wafer 42 which correspond to resistor R_1. A satisfactory voltage has been found to be +13V. Contact strip 58 is also connected to the collector region of this transistor and so provides the output at the collector of T_1. A small positive bias is applied to contact strip 56 and thus to the emitter electrode 14 of the transistor in wafer 42. A potential of 1 volt has been found satisfactory. This positive bias is also applied to the cathode of diode D_2 by virtue of contact strip 56 being connected to wafer strip 40. A small negative bias, for example, −2V., is applied by contact strip 48 to the base electrode 12 of the transistor through contact strip 44 and the horizontal leg of wafer strip 36 which corresponds to resistor R_3. This is because contact strip 44 is ohmically connected to the junction of the vertical and horizontal legs of wafer strip 36, and thus it also connects the base electrode to one terminal of resistor R_2. Anode electrode 18 of diode D_1 in wafer strip 38 is also connected to the base electrode 16 of the transistor at contact strip 44, and its cathode, which is the left-hand region of wafer strip 38, is connected by contact strip 54 to the anode electrode 22 of diode D_2 in wafer strip 40. Plate 32 of capacitor C_2 is connected to contact strip 46 which constitutes input terminal I_1 and receives the trigger pulse when two of the solid state circuits of Figure 2 are being used to form a complete bistable multivibrator. The operation of such a semiconductor multivibrator is similar to that described in connection with Figure 1.

The techniques for fabricating various circuit components within a single body of semiconductor material have been described in the Specifications of both of the aforementioned co-pending Patent Applications, which are herein incorporated by reference. For example, the transistor of Figure 3 in the instant Application may be fabricated by producing the P-region 78 and N-region 76 by means of the well-known diffusion process, or otherwise, and then etching away portions of these regions so as to obtain their desired area. Furthermore, in practice the several wafers shown in Figure 2 may be formed individually and then placed on the supporting substrate and interconnected. The exact shape of the various wafer strips or sections are unimportant to the operation of the circuit. The geometrical "L" shape of wafer strip or section 42, for example, merely provides compactness. Also, the wafers or sections of Figure 2 are there shown entirely disconnected from each other, except for the metallic connecting wires 64, 66, etc., in order to prevent short circuits between certain components. However, it is possible to fabricate the circuit of the instant invention into a single body of high resistivity or essentially intrinsic semiconductor material in which there have been produced N-type or

P-type layers which are in the form of wafer strips 36, 38, 40 and 42 and insulated from each other by the "intrinsic" semiconductor material underlying them. A circuit device fabricated in such a manner assumes the same configuration as shown in Figure 2, 3, 4, 5 and 6, except that the substrate 34 represents the supporting layer of intrinsic semiconductor material in such a device and contact tabs 44, 46, 48, 50, 52, 54, 56 and 58 are alloyed completely through the intrinisic layer 34 to form low resistance contacts to the several regions defining the circuit components.

Among the advantages proferred by this invention are that it provides a miniature semi-conductor bistable multivibrator subcombination which can be fabricated from a body of semiconductor material, portions of which are processed so as to form therein a transistor, diode or capacitor, and wherein all or part of all components of the circuit subcombination are completely fabricated within the body of the semiconductor material; that it can provide a miniaturized semiconductor bistable multivibrator subcombination circuit structure which is substantially smaller, more compact, and simpler than circuit packages which heretofore have been developed using known techniques; that it can provide a miniaturized semiconductor bistable multivibrator circuit subcombination comprising a body of semiconductor material wherein a transistor and a load resistor and various input circuits to the transistor are fabricated within the semiconductor body.

Although the invention has been shown and described in terms of a specific embodiment, it will be evident that many changes and modifications are possible within the scope of the appended claims. For example, the bistable multivibrator subcombination circuit may utilize a P-N-P transistor or possibly other forms of transistors. In such a case, the semi-conductor body adjacent the substrate 34 is a P-type semiconductor material.

WHAT WE CLAIM IS:—

1. A semiconductor circuit comprising a substrate, a plurality of semiconductor regions in or on one and the same face and spaced from the opposite face of said substrate, said regions being electrically isolated from one another through said substrate, certain of said regions being adapted to provide the electrical properties of a transistor having a base, emitter and collector, and first, second and third resistors, said first resistor having one end thereof ohmically connected to said collector, said second and third resistors each having one end thereof ohmically connected to said base, and ohmic contacts to said collector and said emitter and to the other ends of said first, second and third resistors.

2. A semiconductor circuit according to Claim 1, wherein another one of said regions is adapted to provide the electrical properties of a P-N junction diode, and one electrode of said diode is ohmically connected to said base.

3. A semiconductor circuit according to Claim 2, wherein a further one of said regions is adapted to provide the electrical properties of a second P-N junction diode, and one of the electrodes of said second diode is ohmically connected to the other electrode of said diode.

4. A semiconductor circuit according to Claim 3, wherein the other electrode of said second diode is ohmically connected to said emitter.

5. A semiconductor circuit according to any preceding claim, including a capacitor having one plate thereof comprised of a portion of semiconductor material of one of said regions, dielectric material overlying said portion and conductive material overlying said dielectric.

6. A semiconductor circuit according to Claims 4 and 5, wherein said portion is ohmically connected to the other electrode of said diode and said one electrode of said second diode.

7. A semiconductor circuit according to any preceding claim, wherein said substrate is semiconductor material.

8. A bistable circuit comprising two members connected together to form a single circuit and each including a substrate having therein or thereon a plurality of semiconductor regions together providing the electrical properties of a transistor, a capacitive semiconductor diode and a portion of semiconductor material with a substantial resistance.

9. A bistable circuit including two semiconductor members connected together and built up into a single circuit, each member including a transistor, a capacitive semiconductor diode and a portion of semiconductor material with a substantial resistance.

10. A bistable circuit according to Claim 8 or 9, wherein the collector of each transistor is connected through one capacitive semiconductor diode to the base of the transistor of the other member.

11. A bistable circuit according to Claim 8, 9 or 10, wherein for each transistor a portion of semiconductor material with a substantial resistance forms a collector resistor.

12. A bistable circuit according to Claim 11, wherein in each member a portion of semiconductor material with a substantial resistance is connected to a terminal of the capacitive diode.

13. A bistable circuit according to any

P-type layers which are in the form of wafer strips 36, 38, 40 and 42 and insulated from each other by the "intrinsic" semiconductor material underlying them. A circuit device fabricated in such a manner assumes the same configuration as shown in Figure 2, 3, 4, 5 and 6, except that the substrate 34 represents the supporting layer of intrinsic semiconductor material in such a device and contact tabs 44, 46, 48, 50, 52, 54, 56 and 58 are alloyed completely through the intrinisic layer 34 to form low resistance contacts to the several regions defining the circuit components.

Among the advantages proferred by this invention are that it provides a miniature semi-conductor bistable multivibrator subcombination which can be fabricated from a body of semiconductor material, portions of which are processed so as to form therein a transistor, diode or capacitor, and wherein all or part of all components of the circuit subcombination are completely fabricated within the body of the semiconductor material; that it can provide a miniaturized semiconductor bistable multivibrator subcombination circuit structure which is substantially smaller, more compact, and simpler than circuit packages which heretofore have been developed using known techniques; that it can provide a miniaturized semiconductor bistable multivibrator circuit subcombination comprising a body of semiconductor material wherein a transistor and a load resistor and various input circuits to the transistor are fabricated within the semiconductor body.

Although the invention has been shown and described in terms of a specific embodiment, it will be evident that many changes and modifications are possible within the scope of the appended claims. For example, the bistable multivibrator subcombination circuit may utilize a P-N-P transistor or possibly other forms of transistors. In such a case, the semi-conductor body adjacent the substrate 34 is a P-type semiconductor material.

WHAT WE CLAIM IS:—

1. A semiconductor circuit comprising a substrate, a plurality of semiconductor regions in or on one and the same face and spaced from the opposite face of said substrate, said regions being electrically isolated from one another through said substrate, certain of said regions being adapted to provide the electrical properties of a transistor having a base, emitter and collector, and first, second and third resistors, said first resistor having one end thereof ohmically connected to said collector, said second and third resistors each having one end thereof ohmically connected to said base, and ohmic contacts to said collector and said emitter and to the other ends of said first, second and third resistors.

2. A semiconductor circuit according to Claim 1, wherein another one of said regions is adapted to provide the electrical properties of a P-N junction diode, and one electrode of said diode is ohmically connected to said base.

3. A semiconductor circuit according to Claim 2, wherein a further one of said regions is adapted to provide the electrical properties of a second P-N junction diode, and one of the electrodes of said second diode is ohmically connected to the other electrode of said diode.

4. A semiconductor circuit according to Claim 3, wherein the other electrode of said second diode is ohmically connected to said emitter.

5. A semiconductor circuit according to any preceding claim, including a capacitor having one plate thereof comprised of a portion of semiconductor material of one of said regions, dielectric material overlying said portion and conductive material overlying said dielectric.

6. A semiconductor circuit according to Claims 4 and 5, wherein said portion is ohmically connected to the other electrode of said diode and said one electrode of said second diode.

7. A semiconductor circuit according to any preceding claim, wherein said substrate is semiconductor material.

8. A bistable circuit comprising two members connected together to form a single circuit and each including a substrate having therein or thereon a plurality of semiconductor regions together providing the electrical properties of a transistor, a capacitive semiconductor diode and a portion of semiconductor material with a substantial resistance.

9. A bistable circuit including two semiconductor members connected together and built up into a single circuit, each member including a transistor, a capacitive semiconductor diode and a portion of semiconductor material with a substantial resistance.

10. A bistable circuit according to Claim 8 or 9, wherein the collector of each transistor is connected through one capacitive semiconductor diode to the base of the transistor of the other member.

11. A bistable circuit according to Claim 8, 9 or 10, wherein for each transistor a portion of semiconductor material with a substantial resistance forms a collector resistor.

12. A bistable circuit according to Claim 11, wherein in each member a portion of semiconductor material with a substantial resistance is connected to a terminal of the capacitive diode.

13. A bistable circuit according to any

* C L M S *

of Claims 8 to 12, wherein the two members are identical to each other.

14. A semiconductor circuit substantially as described herein with reference to Figs. 1 to 6 of the accompanying drawings.

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ERRATA

SPECIFICATION NO. 953,917

Page 1, line 13, *for* "or" *read* "for"

Page 1, line 14, *for* "electron" *read* "electronic"

Page 1, line 21, *for* "side" *read* "size"

Page 1, line 53, *after* "or" *delete* "a"

Page 2, line 14, *after* "components," *insert* "such as diodes and transistors."

Page 3, line 63, In every instance *for* "inch" *read* "inches"

Page 3, line 99, *for* "out" *read* "our"

Page 4, line 17, *for* "semiconducting" *read* "semiconductor"

Page 4, line 43, *after* "emitter" *insert* "region"

Page 4, line 107, *for* "vapor" *read* "vapour"

Page 5, line 20, *for* "As" *read* "An"

Page 5, line 34, *for* "of" *read* "or"

Page 6, lines 11 and 12, *for* "intrinisic" *read* "intrinsic"

Page 6, lines 13 and 14, *for* "circcuit" *read* "circuit"

THE PATENT OFFICE,
12th September 1967

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* C L M S *