

CONTROL METHOD, SEMICONDUCTOR MEMORY, AND ELECTRONIC DEVICE

ABSTRACT

Embodiments of the present disclosure provide a control method, a semiconductor memory, and an electronic device. When the semiconductor memory is in a preset test mode, a first Model Register (MR) and a second MR related to a Data Pin (DQ) are allowed to directly define the impedance of a Data Mask Pin (DM). The DM does not need to add definition of an output driver state and a related control circuit for the preset test mode to ensure that the preset test mode is adapted to the DM. The impedance of the DM may be tested in the preset test mode to avoid circuit processing errors.

[Fig. 1]